IOSR Journal of Applied Physics (IOSR-JAP)
e-ISSN: 2278-4861.Volume 6, Issue 3 Ver. I (May-Jun. 2014), PP 01-07
www.iosrjournals.org

Determination of electron and hole effective masses in thermal oxide utilizing an n-channel silicon MOSFET

Ravi Kumar Chanana
Department of Electrical and Electronics Engineering, Galgotia's College of Engineering and Technology, Affiliated to Uttar Pradesh Technical University, Lucknow, India.
[1,] Institutional Area, Knowledge Park-II, Greater Noida – 201306, India.

Abstract: *The gate tunnelling electron current and the substrate hole current obtained from carrier separation in an n-channel Si MOSFET are used to determine the parabolic electron and hole effective masses in the thermal oxide. The oxide voltages for electron and hole conduction in the n-MOSFET in inversion are formulated, and the carrier effective masses of 0.42m for electron and 0.58m for hole for a free Fermi gas model of carriers at the emitting electrode are determined using the Fowler-Nordheim tunnelling characteristics. These carrier masses are related to the band offsets in SiO_2/Si<100> MOS devices accurately through the MOSFET model for the first time. The carrier effective masses are predicted to be the same for all thickness of oxide. The technique can be extended to other insulating materials as well. Also, the 1/E model of the anode hole injection over the hole barrier of 4.6 eV completely explains the oxide breakdown in thin oxides of 5 to 10nm at high electric fields, and having a slope constant of 516 MV/cm.*

Keywords: *effective mass, FN-tunelling, band offsets, metal-insulator-semiconductor*

I. Introduction

The knowledge of electron and hole effective masses and conduction and valence band offset values in a metal-oxide-semiconductor (MOS) device can facilitate simulation of Fowler-Nordheim (FN) tunnelling currents through a MOS device at high fields. The FN onset field and the dielectric breakdown field can also be determined. The FN onset field can be obtained for a minimum displacement current density of 10^{-8}-10^{-9} A/cm^2, and the dielectric breakdown field can be obtained for a current density of 10^{-4}A/cm^2, with the above knowledge. The onset field is the upper limit to which the oxide can work as a good insulator without injection and trapping of carriers in it. The trapping of carriers causes degradation of the oxide and reduces its reliability. The above knowledge of carrier effective masses and band offsets can also be utilized to determine oxide thickness to within 0.3nmof other physical techniques of thickness measurement [1]. In view of the above, the determination of the electron and hole effective masses and band offset values in a MOS device is of utmost importance. These tunnelling parameters can be determined from the FN tunnelling equation. The equation models the current-voltage characteristics across a MOS device at high fields [2]. The electron effective mass in the thermal oxide as insulator has been determined earlier to be 0.42m, where m is the free electron mass based on the free Fermi gas model for the carriers at the emitting electrode of a MOS device in accumulation [2, 3]. In the present study, the carrier effective masses in the thermal oxide are determined utilizing the gate tunnelling electron current and the substrate hole current versus the oxide voltage characteristics of a MOSFET. These currents are obtained from carrier separation in an n-channel silicon MOSFET device in inversion [2], with the oxide bandgap value taken as 8.9eV [4, 5]. The carrier mass values obtained are 0.42m for the electron effective mass and 0.58m for the hole effective mass for a free Fermi gas model of carriers at the emitting electrode. However, if quantum confinement of carriers is considered at the emitting electrode, where the conduction or valence band edge forms a triangular potential well when biased, then these values have to be corrected. Nearly 70% population of carriers is calculated to be residing at the ground state subband energy level in the potential well [6], which reduces the electron barrier to oxide conduction band by 0.2eV [7], and the hole barrier to oxide valence band by 0.16eV [8] in Si<100> MOS devices. The corrected electron and hole barrier heights due to quantum confinement results in the electron and hole effective masses in the thermal oxide to 0.51m and 0.65m respectively. It needs to be mentioned here that quantum confinement which causes bandgap broadening at the semiconductor-oxide interface and affects the carrier effective mass calculations, is valid for extremely thin channels in the MOSFETs when the peak of the electron concentration lie several angstroms away from the Si/SiO_2 interface and thus reduces the saturation current. To the author's knowledge to date, quantum correction models, such as the triangular potential well model used by Weinberg [7] has not been able to reproduce the reduced saturation current characteristics in the MOSFETs having thin channels.

I. Theory:

FN electron and hole tunnelling has been observed in Si and SiC MOS devices and in organic light emitting diodes [9-12]. The FN equation models the current-voltage characteristics across a MOS device at high fields. It is given by the classical equation [7,10]:

$\frac{J}{E^2} = Aexp\left(\frac{-B}{E}\right)$; (1)

where J is the current density across the MOS device in A/cm^2,E is the oxide electric field in V/cm, and the pre-exponent A and the slope constant B are given by:

$$A = \frac{e^3 m}{16\pi^2 \hbar m_{ox} \varphi_0}$$

$$A = 1.54x10^{-6} \frac{m}{m_{ox}} \frac{1}{\varphi_0} (A/V^2), \qquad (2)$$

$$B = \frac{4}{3} \frac{(2m_{ox})^{1/2}}{e\hbar} \varphi_0^{3/2}$$

$$B = 6.83x10^7 \left(\frac{m_{ox}}{m}\right)^{1/2} \varphi_0^{3/2} (V/cm) \qquad (3)$$

In A and B constants, e is the electronic charge, m is the free electron mass, m_{ox} is the electron or hole mass in the oxide, $2\pi\hbar$ is Planck's constant and φ_0 is the electron or hole barrier height expressed in electron volts. A plot of ln(J/E^2) versus 1/E, called an FN plot, gives the value of the slope constant B, from which $(m_{ox}/m)^{1/2}\varphi_0^{3/2}$product can be obtained. Then, with a known effective mass, φ_0 can be calculated, and with a known φ_0, the effective mass in the oxide can be calculated. The slope constant B is very sensitive to the oxide field as it is in the exponential and therefore precise determination of the oxide field is absolutely critical in the evaluation of the tunnelling parameters. The ln(J/E^2) term is relatively much less sensitive to the oxide field as it is in the natural logarithm.

A. Formulation of the oxide voltage in a n-channel-MOSFET:

In an ideal MOS diode, if the applied voltage across the diode is V, then $-Q_d/C_i$is the voltage across the oxide [13]. For an n-channel MOSFET Q_d is negative, giving a positive voltage across the oxide insulator. The threshold voltage for strong inversion, V_T for a practical MOS device is expressed as:

$V_T = \varphi_{ms} - \left(\frac{Q_i}{C_i}\right) - \left(\frac{Q_d}{C_i}\right) + \psi_s - \psi_{poly}$; (4)

where, $\varphi_{ms}$is the metal-semiconductor work function difference, Q_i is the oxide insulator charge density, C_i is the oxide insulator capacitance per unit area, Q_d is the depletion charge density in the semiconductor, and $\psi_s$is twice the bulk potential in the semiconductor at which strong inversion occurs for the MOS device and $\psi_{poly}$is the polysilicon depletion potential. For an applied voltage V_T across the MOS device, ideally $-Q_d/C_i$ will fall across the oxide. So, the voltage across the oxide $-Q_d/C_i$ can be expressed as:

$V_{ox} = V_T - V_{fb} - \psi_s + \psi_{poly}$; (5)

where$V_{fb} = \varphi_{ms} - (Q_i/C_i)$ is the flatband voltage. Next, if the applied voltage is$V - V_{sb}$, then the expression for the oxide voltage becomes:

$V_{ox} = V - V_{sb} - V_{fb} - \psi_s + \psi_{poly}$. (6)

Here, $V_{sb}$is the reverse bias applied to the substrate of a MOSFET. It is used to control the threshold voltage in a MOSFET. This is the same equation as developed by Depas and co-researchers [14], except that V_{sb} is also part of the equation for a MOSFET. In terms of the threshold voltage V_T, the equation can be written as:

$V_{ox} = V - V_{sb} - V_T - \frac{Q_d}{C_i}$; (7)

For an n-channel MOSFET in inversion, V_{sb} is negative, V_T is positive, and Q_d is negative. Also, Q_d gets modified due to the application of V_{sb}. Therefore, utilizing the absolute voltages for an n-channel MOSFET, the expression for the oxide voltage for electron tunnelling across the ideal oxide that does not contain any positive charges, can be written as:

$V_{ox} = |V| + |V_{sb}| - |V_T| + \left|\frac{Q_d}{C_i}\right|$. (8)

The electron tunnelling across the oxide is represented by the gate current in the n-channel MOSFET [9]. The substrate hole current in the n-channel MOSFET [9] is believed to be due to the back injection of hot holes from the polysilicon anode having the hole barrier of 4.6eV from the valence band of the polysilicon anode to the oxide valence band [15]. Once the hot holes come into the valence band over the barrier [15], the hole current follows the exp(-B/E) dependence of the FN tunnelling equation (1) through the oxide. An n-channel MOSFET having substrate hole conduction is identical to a p-channel MOSFET having hole injection followed by conduction with the ψ_s and ψ_{poly} of p-MOSFET changed as ψ_{poly} and ψ_s of n-MOSFET. This can be observed from Fig.1(a) and (b). Fig. 1(a) shows an n-MOSFET and Fig.1 (b) shows a p-MOSFET. It can be observed that ψ_s and ψ_{poly} of the p-MOSFET can be changed to ψ_{poly} and ψ_s for the n-MOSFET respectively making the n-MOSFET with hole conduction similar to p-MOSFET with hole conduction.

Therefore, the oxide voltage across the n-MOSFET for substrate hole current conduction can be obtained from the oxide voltage across the p-MOSFET. In a p-MOSFET, the threshold voltage equation (4) given above has negative V_T, negative ψ_s and positive Q_d, and

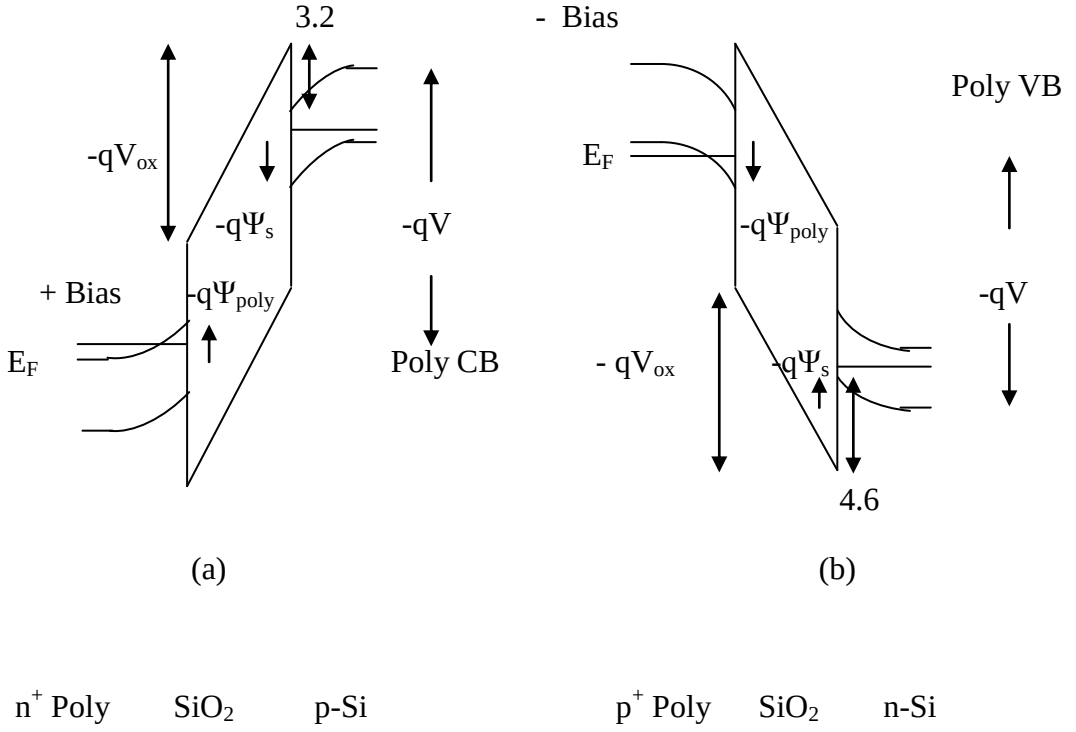

Fig. 1. Energy-band diagram for a (a) n-MOSFET with n^+ polysilicon gate and for a (b) p-MOSFET with p^+ polysilicon gate. Both the devices are biased in inversion.

assuming that the magnitude of V_T for n- and p-MOSFETs is the same. Therefore, for positive oxide charges, the threshold voltage equation (4) for the p-MOSFET can be written as:

$$-|V_T| = -|V_{fb}| - |\psi_s| - \left|\frac{Q_d}{C_i}\right| + |\psi_{poly}|; \qquad (9)$$

Interchanging ψ_s and ψ_{poly} and multiplying throughout by -1, gives:

$$|V_T| = |V_{fb}| - |\psi_s| + \left|\frac{Q_d}{C_i}\right| + |\psi_{poly}|; \qquad (10)$$

Here, for V_T as the applied voltage, Q_d/C_i is the ideal drop across the oxide. This drop in voltage for an applied voltage V_T can be written as V_{ox}. Therefore, for $|V| + |V_{sb}|$ as the applied voltage, the oxide voltage drop across the n-MOSFET with hole conduction can be written as:

$$V_{ox} = |V| + |V_{sb}| - |V_{fb}| + |\psi_s| - |\psi_{poly}|; \qquad (11)$$

For the sake of simplified intermediate steps in formulation of the corrected oxide voltage, the V_{fb} for n- and p-MOSFET is assumed to be the same. Now, from equation (4) for V_T across an n-MOSFET, where Q_d is negative, ψ_s is positive, and with the oxide having positive charges;

$$-|V_{fb}| + |\psi_s| - |\psi_{poly}| = |V_T| - \left|\frac{Q_d}{C_i}\right|; \qquad (12)$$

Substituting equation (12) in equation (11) gives the equation for V_{ox} in n-MOSFET having hole conduction as:

$$V_{ox} = |V| + |V_{sb}| + |V_T| - \left|\frac{Q_d}{C_i}\right|. \qquad (13)$$

Thus, for an n-channel MOSFET device, equation (8) represents the corrected oxide voltage for electron conduction through the oxide, and equation (13) represents corrected oxide voltage for substrate hole conduction through the oxide. The addition of V_T for hole conduction in equation (13) suggests that φ_{ms} for electron conduction becomes φ_{sm} for hole conduction. The oxide voltage for electron conduction is therefore different from the oxide voltage for hole conduction. This point is also discussed in the authors's earlier work [2]. It is shown that the oxide voltage has to be corrected by the flatband voltage for MOS devices in accumulation. In

the present study utilizing an n-channel MOSFET, the oxide voltages are modified by the threshold voltage.

II. Sample Calculations and Results:

A sample calculation for the electron and hole effective masses is performed here, utilizing the current-voltage data on an n^+-polysilicon gated n-channel Si MOSFET. Two points of current and voltage are taken in the FN regime for the gate current representing electron tunnelling current and the substrate hole current from fig. 2 of reference [9], and are presented in Table I below.

Table I. Current-voltage data in the FN region for gate electron current and substrate hole current of the MOSFET.

Current Type	$\lvert V_1\rvert + \lvert V_{sb}\rvert$ (V)	I_1 (A)	$\lvert V_2\rvert + \lvert V_{sb}\rvert$ (V)	I_2 (A)	Uncorrected B (MV/cm)
Gate Electron Current Data	(8.0 + 1)	10^{-8}	(9.5 + 1)	10^{-6}	330
Substrate Hole Current Data	(9.5 + 1)	10^{-9}	(11.0 + 1)	10^{-7}	434

For the calculation of corrected oxide voltages, the threshold voltage V_T is taken as 1.25V. The substrate bias adjusts the threshold voltage of the MOSFET. As the magnitude of the substrate bias V_{sb} increases from 1V to 16V, V_T also increases from 1.25V to 3.25V as presented in fig. 43 of reference [16]. Thus, V_T is 1.25V for the substrate bias of -1V, in the present study. The V_T values presented in the fig.43 of the above reference [16] are considered more accurate because they are calculated experimentally using the MOSFET channel conductance. The other desired parameter values are calculated and presented in Table II below.

Table II. MOSFET parameters for the calculations of corrected oxide voltages.

Substrate doping $N_A = 10^{16}/cm^3$	Intrinsic carrier conc. $n_i = 1.45 \times 10^{10}/cm^3$	Surface potential at strong inversion $\psi_s = 2\psi_B = \frac{2kT}{q}\ln\frac{N_A}{n_i} = 0.7$ V
$\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm	$\varepsilon_r = 3.9$ Oxide thickness $d = 85 \times 10^{-8}$ cm	Oxide capacitance $C_i = \frac{\varepsilon_0\varepsilon_r}{d}$ $= 4.0 \times 10^{-7}$ F/cm^2
$\varepsilon_{Si} = 11.9\,\varepsilon_0$	Depletion charge density $Q_d = \sqrt{2\varepsilon_{Si}qN_A\left(\lvert\psi_s\rvert + \lvert V_{sb}\rvert\right)}$ $= 7.56 \times 10^{-8}$ C/cm^2	$\frac{Q_d}{C_i} = 0.19$ V
n^+ poly Si gate and p-Si work function difference $\phi_{ms} = -1.08$ V	Oxide fixed charge density $Q_i = q.\,2 \times 10^{10}$C/cm^2	Flatband voltage $V_{fb} = \phi_{ms} - \frac{Q_i}{C_i} = -1.1$ V

Utilizing the values of the above parameters, the corrected oxide voltages can be calculated. The corrected slope constant B is determined from the I-V characteristics using equation (1) given above. First, $\Delta ln\,(J/E^2)/\Delta\,(1/E)$is calculated by taking at least two points on the I-V characteristics in the FN regime at high fields given in Table I. For this, the sum of the gate voltage and substrate bias voltage is used for a particular gate current or substrate current in case of the n-channel MOSFET device. This yields the uncorrected B presented in Table I. Next, the corrected B is calculated by dividing $\Delta ln(J/E^2)$ by$\Delta(1/E)$, where $\Delta ln(J/E^2)$ is the same that was used for the calculation of uncorrected B, but the $\Delta(1/E)$employs the corrected oxide voltages. This is because $\Delta ln(J/E^2)$ does not change with the oxide field, as it is in the natural logarithm, and the oxide voltages are corrected for the same current density J as for uncorrected B. The corrected oxide voltages for the gate electron current and the substrate hole current are given in Table III. These values of oxide voltages are obtained by using equation (8) and (13). The oxide voltage divided by the oxide thickness gives the corrected oxide field. Finally, from the corrected B value, m_{ox} or $\varphi_0$can be determined if one of them is known using equation (3). The corrected oxide voltages, the corrected slope constant B, the electron and hole barrier heights used, and the calculated effective masses m_{ox}, for electron and hole are presented in Table III below.

Table III. Corrected oxide voltages and tunnelling parameters for gate electron and substrate hole currents in the MOSFET.

Current Type	Corrected V_{ox1} (V)	Corrected V_{ox2} (V)	Corrected B (MV/cm)	φ_0(eV)	m_{ox}(determined)
Gate Electron Current Data	7.94	9.44	254	3.2	0.42m
Substrate Hole Current Data	11.56	13.06	516	4.6	0.58m

The calculated electron effective mass in the thermal oxide for an electron barrier of 3.2eV from the Si conduction band to oxide conduction band is 0.42m. The hole effective mass in the oxide for an anode hole barrier of 4.6eV is determined to be 0.58m. For quantum confinement at the emitting electrode when biased, the reduced electron and hole barrier heights give electron effective mass in the oxide as 0.51m and the hole effective mass as 0.65m. The carrier effective mass values for a free Fermi gas model for carriers at the emitting electrode are the same as that obtained in a recent study using n- and p-4H-SiC MOS devices in accumulation with SiO_2/4H-SiC devices having vastly different band offsets than SiO_2/Si<100> devices [2]. This reaffirms the values and also suggests that an n-channel Si MOSFET device that allows carrier separation can be used to determine the carrier effective mass values accurately.

III. Discussion

FN tunnelling of carriers occurs in thick oxides greater than 4nm [1,14,17] in which the application of high electric field results in carrier tunnelling as a wave into the oxide conduction or valence band through the triangular barrier and then travels through the insulator as a particle with an effective mass to reach the opposite electrode. In oxides having thickness of 4nm or less, the electron or hole directly tunnels across the trapezoidal barrier of the MOS device to the opposite electrode as a wave without going to the oxide conduction or valence band. Thus, the carrier propagates as a wave-particle dual in FN tunnelling, and as a wave in direct-tunnelling across the MOS device. In either case the propagation is through the oxide. Therefore, the author predicts that the carrier effective masses will remain the same for all the thicknesses of the oxide or insulating materials. A recent report has modelled the direct and FN-tunneling of electrons utilizing a thickness independent tunnel mass of 0.42m [18]. Another report presents the electron effective mass in a thin tunnel oxide of 3.5nm as 0.42m [19], which is the same as that in thick oxides[2,3].

The origin of the substrate current in n-MOSFETs having thin oxide from 5 to 10nm is under debate [9, 15, 20, 21]. Eitan and Kolodny were one of the first to observe substrate hole current in n-channel MOSFET having 8.5nm oxide, and attributed the hole current to the valence electron tunnelling from the Si substrate having a barrier of 4.3eV from the Si valence band to the oxide conduction band [9]. DiMaria et al. proposed later that these holes originate as hot holes from the polysilicon anode. The energy for the hot holes are provided by the FN tunnelling electrons from the cathode, which have a threshold average energy of about 5eV from the bottom of the oxide conduction band. These hot holes are concluded to be back injected from the anode over the hole barrier at the Si anode for thin oxides of 5 to 10nm. In these thin oxides, the electron transport is quasi-ballistic, so that the maximum electron energy at the anode is independent of the oxide thickness giving a thickness independent threshold [15]. More recently, the substrate holes are experimentally shown to be generated by FN-induced photons in the polysilicon gate [20]. A report after the above, refuted this process of hole generation and concluded that the generation efficiency of photons with energy above the Si bandgap energy is 10^{-4} times smaller than that of the electron-hole pairs by impact ionization [21]. The above studies, leads the author to believe that the hot holes from the anode are back injected into the oxide over the barrier [15, 22]. After coming to the oxide valence band, the hole current follows the exp(-B/E) dependence of the FN tunnelling equation (1). The calculated hole effective mass based on this dependence is exactly the same as that determined from the FN tunnelling of holes observed in p-4H-SiC MOS devices in accumulation [2]. This value of hole effective mass is 0.58m for a free Fermi gas model of carriers at the emitting electrode. A value of 0.57m has been used earlier as a fitting parameter in a high frequency tunnel emitter transistor model [23]. The value is also consistent with the evidence of light holes near the top of the oxide valence band [24].

The valence band offset of 4.6eV ($E_{g,oxide}$ - $E_{g,Si}$ - Si CB offset) results in the hole effective mass value of 0.58m in the oxide. This valence band offset has also been reported recently in experimental studies on remote plasma grown dry SiO_2 of 0.9 to 2.2nm, and 2nm dry thermal SiO_2 utilizing soft x-ray photoemission spectroscopy on SiO_2/Si(100) test samples. Table I of the reference [25] presents the valence band offset for the remote plasma SiO_2/Si(100) sample as 4.54 ± 0.06 eV, and the more recent study on 2nm dry thermal SiO_2/Si(100) sample presents the valence band offset as 4.5 ± 0.1 eV [26]. The resulting hole mass of 0.58m is the same as that obtained for p-4H-SiC MOS device in accumulation undergoing FN tunnelling of holes [2], where the Schottky barrier lowering does not change the tunnelling distance. This implies that Schottky barrier lowering in thin oxides of 5 to 10nm, in which the hot holes are injected into the oxide valence band by thermionic emission over the barrier is absent [15, 22]. This is due to the fact that the generated hot holes due to impact ionization at the polysilicon anode of the electrons arriving from the cathode also have a thickness

independent energy. This eliminates any Schottky barrier lowering at the valence band which is field-dependent [22] and therefore thickness-dependent.

The oxide breakdown in thin oxide films of 5 to 10nm is intimately related to the substrate current due to hot holes, which is proportional to exp(-B/E) at high electric fields with the slope constant B of 516 MV/cm presented in Table III. An n-channel silicon MOSFET when biased in inversion as shown in Fig.1a, results in FN tunnelling of electrons from the cathode into the oxide due to the smaller electron barrier to oxide conduction band of 3.2 eV. They then arrive at the polysilicon anode, where they impact ionize and create hot holes. The hot holes inject over the hole barrier of 4.6 eV at the anode [15] and cause the substrate hole current through the oxide. Some holes are trapped in the oxide causing increase in the field at the cathode [2]. This results in larger electron current injection from the cathode into the oxide by FN tunnelling followed by increased substrate current and hole trapping in the oxide. This positive feedback results in the oxide breakdown. The time-to-breakdown is therefore proportional to exp(-B/E) with the slope constant B of 516 MV/cm instead of 350 MV/cm reported earlier [27]. This 1/E model of the anode hole injection [27] completely explains the oxide breakdown in thin oxide films of 5 to 10nm at high electric fields.

Several MOS device configurations can be used to determine electron and hole effective masses or band offsets in thermal oxide and in other viable high-K dielectrics [26, 28, 29]. Six of them are listed below:

1. A p-4H-SiC or p-6H-SiC MOS device can be used in accumulation to determine hole effective mass from the hole current versus voltage characteristics [2].
2. An n-4H-SiC or n-6H-SiC MOS device can be used in accumulation to determine electron effective mass from electron current versus voltage characteristics [2].
3. An n-Si MOS device can be used in accumulation to determine electron effective mass from the electron current versus voltage characteristics.
4. A p-Si MOS device can be used in accumulation to determine hole effective mass from the hole current versus voltage characteristics. Here, all the metals available as gate contact have a lower electron barrier to oxide conduction band as compared to the hole barrier of 4.6eV at the Si anode. Therefore the p-MOS device in accumulation will not have the hole tunnelling current as the dominant current. The choice of gate material should be p+ poly silicon carbide. This will ensure a 6eV valence electron barrier to the oxide conduction band and the dominant FN hole tunnelling from the Si anode having a 4.6eV hole barrier will occur at an onset field of about 14MV/cm.
5. An n-channel n+ polysilicon gated Si MOSFET having a thin oxide of 5 to 10nm can be used to determine electron effective mass from the gate tunnelling current and the hole effective mass from the substrate current. This is demonstrated in the present study.
6. A p-4H-SiC based MOS device in inversion can be used to find electron effective mass from the dominant electron current versus voltage characteristics. This method is complex because strong inversion in SiC does not take place without the application of temperature or shinning UV light. This is due to the fact that the intrinsic carrier concentration in SiC is low because of its wide band gap.

IV. Conclusion:

The parabolic electron and hole effective masses in the thermal oxide are determined to be 0.42m and 0.58m for a free Fermi gas model of carriers at the emitting electrode utilizing a Si n-channel MOSFET device in inversion that allows carrier separation. These carrier masses are related to the band offsets in SiO_2/Si<100> MOS devices accurately though the MOSFET model and is reported for the first time. For quantum confinement of carriers at the emitting electrode when biased, the electron and hole effective masses in the oxide corrects to 0.51m and 0.65m, respectively, keeping in view that quantum correction is valid for extremely thin channels in MOSFETs. The effective masses are predicted to be the same for all thicknesses of the oxide. The device configurations discussed can be utilized with other insulating materials as well for the determination of carrier masses. Also, the 1/E model of the anode hole injection over the hole barrier of 4.6 eV completely explains the oxide breakdown in thin oxides of 5 to 10nm having a slope constant of 516 MV/cm.

References

[1]. H.S.Chang, H.D.Yang, H.Hwang, H.M.Cho, H.J.Lee andD.W.Moon, "Measurement of the physical and electrical thickness of ultrathin gate oxides", J.Vac.Sci.Technol., vol. 20,pp. 1836-1842, Sep. 2002.

[2]. R.K. Chanana, "Determination of hole effective mass in SiO_2 and SiC conduction band offset using Fowler-Nordheim tunneling characteristics across metal-oxide-semiconductor structures after applying oxide field corrections", J. of Applied Physics, vol. 109, pp. 104508-1 to -6, May 2011.

[3]. M. Lenzlinger and E.H. Snow, "Fowler-Nordheim tunneling into thermally grown SiO_2", J. of Applied Physics, vol. 40, pp. 278-283, Jan. 1969.

[4]. R.B. Laughlin, "Optical absorption edge of SiO_2", Physical Review B, vol. 22, pp. 3021-3029, Sep. 1980.

[5]. V.V. Afanasev, "Valence band offset and hole injection at the 4H-, 6H-SiC/SiO_2 interfaces", Applied Physics Letters, vol. 77, pp. 2024-2026, Sep. 2000.

[6]. Y.T. Hou, M.F. Li, Y. Jin, and W.H. Lai, "Direct tunneling hole currents through ultrathin gate oxides in metal-oxide-semiconductor devices", J. of Applied Physics, vol. 91, pp. 258-264, Jan. 2002.

[7]. Z.A. Weinberg, "On tunneling in metal-oxide-silicon structures", J. of Applied Physics, vol. 53, pp. 5052-5056, Jul. 1982.

[8]. S.Rodriguez, J.A.Lopez-Villanueva, I.Melchor andJ.E. Carceller, "Hole confinement and energy subbands in silicon inversion layer using the effective mass theory", J.Appl. Phys., vol. 86, pp. 438-444, Jul. 1999.

[9]. B.Eitan and A.Kolodny, "Two components of tunneling current in metal-oxide-semiconductor structures", Appl. Phys. Lett., vol. 43, pp. 106-108, Jul. 1983.

[10]. R.K.Chanana, K.McDonald, M.Di Ventra, S.T.Pantelides,L.C.Feldman,G.Y.Chung, C.C.Tin, J.R.Williams, R.A.Weller, "Fowler-Nordheim hole tunneling in p-SiC/SiO_2 structures", Appl. Phys. Lett., vol. 77, pp. 2560-2562, Oct. 2000.

[11]. R.Waters and B.Van Zeghbroeck, "Fowler-Nordheim tunneling of holes through thermally grown SiO_2 on p^+ 6H-SiC", Appl. Phys. Lett., vol. 73, pp. 3692-3694, Dec. 1998.

[12]. I.D.Parker, "Carrier tunneling and device characteristics in polymer light-emitting diodes", J.Appl. Phys., vol. 75, pp. 1656-1666, Feb. 1994.

[13]. Ben G. Streetman, Sanjay Banerjee, "Field-Effect transistors", in Solid State ElectronicDevices, 5th edition, New Delhi, India, Prentice-Hall, 2001, pp. 267-277.

[14]. M.Depas, B.Vermeire, P.W.Mertens, R.L. Van Meirhaeghe,andM.M. Heyns, "Determination of tunneling parameters in ultra-thin oxide layer poly-Si/SiO_2/Si structures", Solid-State Electronics, vol. 38, pp. 1465-1471, Aug. 1995.

[15]. D.J. DiMaria, E. Cartier, and D.A. Buchanan, "Anode hole injection and trapping in silicon doxide", J. Appl. Phys., vol. 80, pp. 304-317, Jul. 1996.

[16]. S.M. Sze, "Unipolar Devices', in Semiconductor Devices, Physics and Technology, New York, John Wiley and Sons,1985, pp. 186-221.

[17]. M.L.Green, E.P.Gusev, R.Degraeve, E.L.Garfunkel, "Ultrathin (<4nm) SiO_2 and Si-O-N gate dielectric layers for silicon microelectronics: Understanding the processing, structure, and physical and electrical limits", J.Appl.Phys., vol. 90, pp. 2057-2121, Sep. 2001.

[18]. A. Schenk and G. Heiser, "Modeling and simulation of tunnelling through ultra-thin gate dielectrics", J. Appl. Phys.,vol. 81, pp.7900-7908, Jun. 1997.

[19]. F.A.Noor, M.Abdullah, Sukirno and Khairurrijal, "Analysis of electron direct tunneling current through very-thin gate oxide in MOS capacitors with the parallel-perpendicular kinetic energy components and anisotropic masses", BrazilianJournal of Physics, vol. 40, pp. 404-407, Dec. 2010.

[20]. M.Rasras, I. DeWolf, G. Groeseneken, B. Kaczer, R. Degraeve, and H.E. Maes, "Photo-carrier generation as the origin of Fowler-Nordheim-induced substrate hole current in thin oxides", IEEE, Trans. On Electron Devices, vol. ED-48, pp. 231-238, Feb. 2001.

[21]. A. Dalla Serra, P. Palestri, L. Selmi, "Can photoemission/absorption processes explain the substrate current of tunneling MOS capacitors?", Solid-State Electronics, vol. 46, pp. 1069-1073, Jul. 2002.

[22]. K. Kobayashi, A. Teramoto, M. Hirayama, and Y. Fujita, "Model for the substrate hole current based on thermionic hole emission from the anode during Fowler-Nordheim electron tunnelling in n-channel metal-oxide-semiconductor field-effect transistors", J. Appl. Phys., vol. 77, pp.3277-3282, Apr. 1995.

[23]. E.Aderstedt, Per Lundgren, "High-frequency operation potential of the tunnel emitter transistor, Solid-State Electronics, vol. 46, pp.1033-1037, Jul., 2002.

[24]. V.A. Gritsenko, R.M. Ivanov, Yu. N. Morokov, "Electronic structure of amorphous SiO_2: Experiment and numerical simulation", Journal of Theoretical and Experimental Physics, vol. 81, pp. 1208-1216, Dec. 1995.

[25]. J.W. Keister, J.E. Rowe, J.J. Kolodziej, H. Niimi, T.E. Madey, G. Lucovsky, "Band offsets for ultrathin SiO_2 and Si_3N_4 films on Si(111) and Si(100) from photoemission spectroscopy", J. Vac. Sci. Technol. B. 17, pp.1831-1835, Jul/Aug 1999.

[26]. E. Bersch, S. Rangan, R.A. Bartynski, E. Garfunkel, E.Vescovo, "Band offsets of ultrathin high-K oxide films with Si", Physical Review B, vol. 78, pp.085114-1 to 10, 2008.

[27]. Yee-Chia Yeo, Qiang Lu, and Chenming Hu, "MOSFET gate oxide reliability: Anode hole injection model and its applications", International Journal Of High Speed Electronics and Systems, vol. 11, no.3, pp. 849-886, 2001.

[28]. G.D. Wilk, R.M. Wallace, J.M. Anthony, "High-K gate dielectrics: Current status and materials properties considerations", J. Appl. Phys, vol.89, pp.5243-5275, May 2001.

[29]. J. Robertson, "High dielectric constant oxides", Eur. Phys. J. Appl. Phys., vol. 28, pp.265-291, Dec. 2004.