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Integration of Irreversible Gates in Reversible Circuits Using NCT Library

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Abstract : *The reversible circuit synthesis problem can be reduced to permutation group. This allows Schreier-Sims Algorithm for the strong generating set-finding problem to be used to synthesize reversible circuits using the NCT library. Applying novel optimization rules to minimize the number of gates gives better quantum cost than that shown in the literature. Applications on how to integrate any three irreversible Boolean functions on a single 3-bit reversible circuit will be shown.*
Keywords: *Reversible Circuit, Quantum Cost, Circuit Optimization, Group Theory*

I. INTRODUCTION

Reversible logic [1,2] is an active area of research. It has many applications in quantum computing [3,4], low-power CMOS [5,6] and many more. Synthesis and optimization of Boolean reversible circuits cannot be done using classical methods [7]. Optimization of Boolean systems on non-standard computers that promise to do computation more powerfully [8] than classical computers, such as quantum computers, is essential to explore the novel applications that can be applied on such systems.

The study of reversible logic synthesis problem using group theory is arising rapidly. Investigation on the universality of the basic building blocks of reversible circuits has been done [9,10]. A relation between Young subgroups and the reversible logic synthesis problem has been proposed [11]. A comparison between the decomposition of reversible circuit and quantum circuit using group theory has been shown [12]. GAP-based algorithms that synthesize reversible circuits for various types of gate with various gate costs have been proposed [13]. Tight bounds on the synthesis of 3-bit reversible circuits using NCT library has been shown in [14].

The first aim of the paper is to synthesize 3-bit reversible circuits using NCT library with better quantum cost than that shown in the literature. The second aim is to use the synthesized circuits to design a reversible circuit that simulates the function of irreversible Boolean functions such as $AND, OR, NOT, XOR, NAND$ and NOR in a single zero-garbage reversible circuit by integrating any three Boolean functions as long as this integration keep the reversibility of the circuit.

The paper is organized as follows: Sect. 2 gives a short background on the synthesis of reversible circuit problem and shows the reduction the problem to permutation group. Sect. 3 shows the optimization rules applied on reversible circuits obtained using Schreier-Sims Algorithm for the strong generating set-finding problem [15] to decrease the quantum cost of the circuits. Sect. 4 shows the results of the experiments. Sect. 5 shows the results of integrating irreversible Boolean functions in a single 3-bit reversible circuit. The paper ends up with a summary and conclusion in Sect. 6.

II. BACKGROUND

This section will review the basic definitions of reversible circuits, the definition of quantum cost of reversible circuits and the basic notions for reversible circuit synthesis, the relationship between reversible logic circuits and permutation group theory.

2.1 BASIC DEFINITIONS

Definition 1: Let $X = \{0,1\}$. A Boolean function f with n input variables $x_1,\dots,x_n$ and n output variables $y_1,\dots,y_n$, is a function $f : X^n \to X^n$, where $(x_1,\dots,x_n) \in X^n$ is called the input vector and $(y_1,\dots,y_n) \in X^n$ is called the output vector.

Definition 2: An n-input n-output Boolean function is reversible ($n \times n$ function) if it maps each input vector to a unique output vector, i.e. a one-to-one, onto function (bijection). There are $2^n!$ reversible $n \times n$ Boolean functions. For $n = 3$, there are 40320 3-in/out reversible functions.

Definition 3: An n-input n-output (n-in/out) reversible gate (or circuit) is a gate that realizes a $n \times n$ reversible function.

Definition 4: When an *m*-in/out reversible gate *U* is applied on an *n*-in/out reversible circuit such that $m \leq n$, then *U* will be denoted as $U^n_{i1i2\dots im}$ where $\{i_1, i_2, \dots, i_m\}$ are the *m* wires spanned by *U* in order.

Definition 5: A set of reversible gates that can be used to build a reversible circuit is called a gate library *L*.

Definition 6: A universal reversible gate library L_n is a set of reversible gates such that a cascading of gates in L_n can be used to synthesize any reversible circuit with *n*-in/out.

Definition 7: A universal reversible gate sub library SL_n is a set of reversible gates such that $SL_n \subseteq L_n$ that can be used to build any reversible circuit with *n*-in/out.

Definition 8: Let a finite set $A = \{1, 2, \dots, N\}$ and a bijection $\delta : A \rightarrow A$, then δ can be written as,

$$\begin{pmatrix} 1 & 2 & 3 & \dots & n \\ \delta(1) & \delta(2) & \delta(3) & \dots & \delta(n) \end{pmatrix} \quad (1)$$

i.e. δ is a permutation of A. Let *A* be an ordered set, then the top row can be eliminated and δ can be written as,

$$(\delta(1), \quad \delta(2), \delta(3), \dots, \delta(n)) \quad (2)$$

Any reversible circuit with n-in/out can be considered as a permutation δ and (2) is called the specification of this reversible circuit such that $N = 2^n$.

The set of all permutations on *A* forms a symmetric group on *A* under composition of mappings [16], denoted by S_N [17]. A permutation group *G* is a subgroup of the symmetric group S_N [16]. A universal reversible gate library L_n is called the generators of the group. Another important notation of a permutation is the product of disjoint cycles [17]. For example, $\begin{pmatrix} 1,2,3,4,5,6,7,8 \\ 1,2,4,3,7,6,8,5 \end{pmatrix}$ will be written as $(3, 4)(5, 7, 8)$. The identity mapping "()" is called the unit element in a permutation group. A product $p * q$ of two permutations p and q means applying mapping p then q, which is equivalent to cascading p and q.

2.2 Reversible Circuits

The C^nNOT gate is used as the main reversible gate to build any reversible circuit, since it is proved to be universal for reversible logic synthesis [7]. The C^nNOT gate is defined as shown in Fig.1.

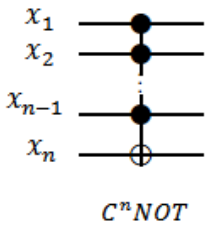

Figure 1: C^nNOT gate. The control bit line is denoted by •, and the target bit line is denoted by ⊕.

The action of C^nNOT gate is defined as follows, if the control bit lines are set to 1 then the target bit line is flipped, otherwise the target bit line is left unchanged. Some special cases of the C^nNOT gate are defined as follows, C^1NOT gate with no control bit is called NOT gate. C^2NOT with one control bit is called $CNOT$ gate. C^3NOT with two control bits is called Toffoli gate. For the sake of readability C^1NOT, C^2NOT and C^3NOT will be written shortly as N, C and T respectively where the control and/or target bits will be shown in the subscript of the gate and the total number of bits will be shown in the superscript. The N, C and T gates can be used to form a universal library for 3-in/out reversible circuits known as NCT library. The main NCT library consists of 12 gates as shown in Fig.2.

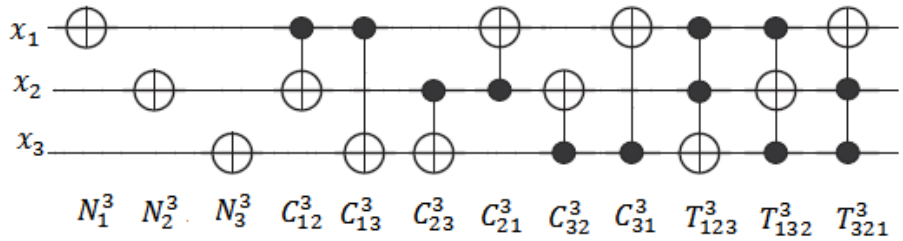

Figure 2: The main NCT library consists of 12 gates

A gate library with N gates is not universal for 3-in/out reversible circuits since it can realize only 8 possible circuits from the 40320 circuits [18]. For n-in/out reversible circuits, there are n possible N gates. There are 3 possible N gates as shown in Fig.3.

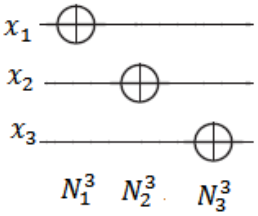

Figure 3: The 3 possible N gates for 3-bit reversible circuits.

$$\begin{aligned} N_1^3:(x_1,x_2,x_3) &\xrightarrow{yields} (x_1 \oplus 1, x_2, x_3) \equiv (1,5)(2,6)(3,7)(4,8), \\ N_2^3:(x_1,x_2,x_3) &\xrightarrow{yields} (x_1, x_2 \oplus 1, x_3) \equiv (1,3)(2,4)(5,7)(6,8), \\ N_3^3:(x_1,x_2,x_3) &\xrightarrow{yields} (x_1, x_2, x_3 \oplus 1) \equiv (1,2)(3,4)(5,6)(7,8). \end{aligned} \tag{3}$$

A gate library with C gates can realize a total of 168 reversible circuits [18]. There are 6 possible C gates for the 3-in/out reversible circuits as shown in Fig.4.

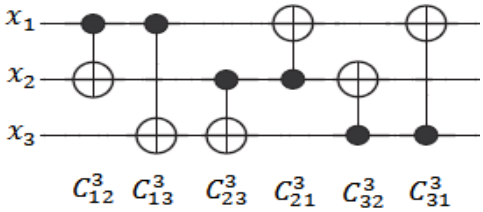

Figure 4: The 6 possible C gates for 3-bit reversible circuits.

$$\begin{aligned} C_{12}^3:(x_1,x_2,x_3) &\xrightarrow{yields} (x_1, x_2 \oplus x_1, x_3) \equiv (5,7)(6,8), \\ C_{13}^3:(x_1,x_2,x_3) &\xrightarrow{yields} (x_1, x_2, x_3 \oplus x_1) \equiv (5,6)(7,8), \\ C_{23}^3:(x_1,x_2,x_3) &\xrightarrow{yields} (x_1, x_2, x_3 \oplus x_2) \equiv (3,4)(7,8), \\ C_{21}^3:(x_1,x_2,x_3) &\xrightarrow{yields} (x_1 \oplus x_2, x_2, x_3) \equiv (3,7)(4,8), \\ C_{32}^3:(x_1,x_2,x_3) &\xrightarrow{yields} (x_1, x_2 \oplus x_3, x_3) \equiv (2,4)(6,8), \\ C_{31}^3:(x_1,x_2,x_3) &\xrightarrow{yields} (x_1 \oplus x_3, x_2, x_3) \equiv (2,6)(4,8). \end{aligned} \tag{4}$$

The T gate is the smallest reversible gate that is proved to be universal for non-reversible computation as it is proved to function as $NAND$ gate by initializing the target bit to 1 [7]. A gate library with T gate is not universal for reversible computation since it can realize only 24 possible 3-in/out reversible circuits [18]. There are three possible T gates for the 3-in/out reversible circuits as shown in Fig.5.

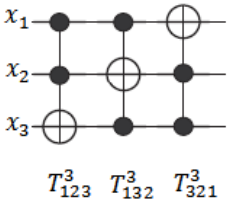

Figure 5: The 3 possible Toffoli (T) gates for 3-bit reversible circuits.

$$\begin{aligned} T^3_{123}:(x_1,x_2,x_3) &\xrightarrow{yields} (x_1,x_2,x_3 \oplus x_1x_2) \equiv (7,8), \\ T^3_{132}:(x_1,x_2,x_3) &\xrightarrow{yields} (x_1,x_2 \oplus x_1x_3,x_3) \equiv (6,8), \\ T^3_{321}:(x_1,x_2,x_3) &\xrightarrow{yields} (x_1 \oplus x_2x_3,x_2,x_3) \equiv (4,8). \end{aligned} \quad (5)$$

For 3-bits reversible circuits, there are 40320 possible 3-in/out reversible circuits. The N gate, the C gate and the T gate (NCT library) can used to synthesize all 40320 possible 3-in/out reversible circuits.

2.3 QUANTUM COST

The quantum cost of a reversible circuit refers to optimization measurement as well as the number of C^nNOT gates used in the circuit. The quantum cost of a reversible circuit is measured by the number of elementary gates required to build the C^nNOT gate [19], i.e. the number of 2-qubit gates used in its implementation as a quantum circuit. In this paper, the cost of N gate is ignored as in [13] to be able to compare results, i.e. the cost of N is equal zero, and the cost of any 2-qubit gate is 1 and the quantum cost of T is equal 5 as shown in Fig.6.

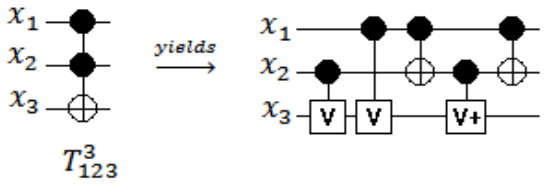

Figure 6: Decomposition of a T gate as 5 elementary gates.

When implementing a reversible circuit, there are four elementary quantum gates that will be used: N gate, C gate, Controlled-V and Controlled-V^+ gates, where $VV^+ = V^+V = I$, $VV = V^+V^+ = N$, and I is the identity gate [19].

III. OPTIMIZATION RULES TO REDUCE QUANTUM COST

Optimization rules will be used to identify and classify similarity of gates among a circuit when decomposed to a sequence of quantum gates. Decomposition of 3-bit reversible circuits can be used to decrease the quantum cost. Optimization is done by removing and/or combining (merging) adjacent gates act on the same qubit lines [20]. For example, the cost of the sequence of reversible gates $[T^3_{123}, C^3_{12}]$ is 4 instead of 6 as shown in Fig.7, the cost of the sequence of reversible gates $[T^3_{123}, C^3_{21}]$ is 5 instead of 6 as shown in Fig.8 and the cost of the sequence of reversible gates $[T^3_{321}, T^3_{132}]$ is 9 instead of 10, because the sequence of gate C^3_{32} and gate V^3_{32} can be combined as one gate $[C^3_{32}V^3_{32}]$ [20] as shown in Fig.9. The optimization rules used in this paper to decrease the quantum cost of the 3-bits reversible circuits are shown in Table 1.

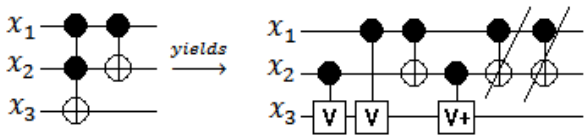

Figure 7: Decomposition of 3-bit reversible circuit $[T^3_{123}, C^3_{12}]$ as 4 elementary gates.

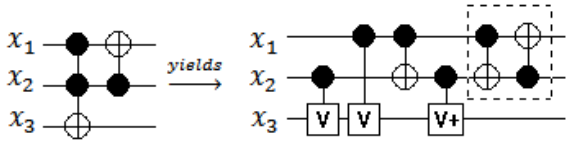

Figure 8: Decomposition of 3-bit reversible circuit $[T^3_{123}, C^3_{21}]$ as 5 elementary gates.

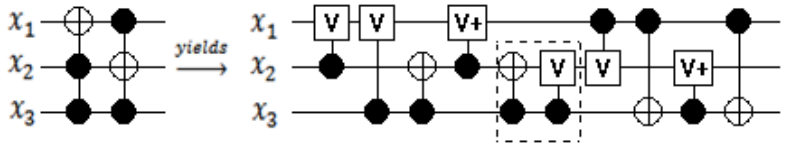

Figure 9: Decomposition of 3-bit reversible circuit $[T^3_{321}, T^3_{132}]$ as 9 elementary gates.

Table 1: Comparison of quantum cost using the proposed optimization rules and the existing work [21].

NCT Circuits	Quantum Cost	
	[21]	Proposed rules
$T^3_{123}C^3_{12}$	6	4
$T^3_{123}C^3_{21}$	6	5
$T^3_{132}C^3_{13}$	6	4
$T^3_{132}C^3_{31}$	6	5
$T^3_{321}C^3_{23}$	6	5
$T^3_{321}C^3_{32}$	6	4
$T^3_{321}T^3_{132}$	10	9
$T^3_{123}T^3_{132}$	10	9
$T^3_{132}T^3_{123}$	10	9

IV. EXPERIMENTAL RESULTS

Experiments on 3-bits reversible circuits' synthesis are presented using the NCT library, the Schreier-Sims algorithm [14] is implemented using the group-theory algebraic software GAP [22]. This algorithm deals with minimal number of generator problems, which is more reasonable in practice because the gates have different costs. Some papers discussed these problems by other methods such as [13] and [14] but the Schreier-Sims algorithm realized in GAP [22] gives the similar minimal length problems result as shown in [13] and [14] and better results to minimize the quantum cost by applying the optimization rules as will be shown later.

Table 2 and Table 3 show the results for the main NCT gate library as a universal reversible library for reversible computation since it can realize the 40320 possible 3-in/out reversible circuits. Table 3 gives the same result as Table 2 with more details on the cost of minimum length. The main NCT gate library synthesizes the best maximum length circuits, where the best maximum length = 8 gates with cost = 21 and maximum cost = 25 with circuit length = 7. Using group-theory algebraic software GAP [22] shows that the average length of a reversible circuit synthesized with NCT library is 5.865 which is similar to that shown in [13] and [14].

Table 4 and Table 5 show the results for the sub-libraries of the main NCT gate library which synthesize the best maximum cost circuits, where the best maximum cost = 17 with circuit length = 7 and maximum length = 12 with cost = 14. Table 5 gives the same result as Table 4 with more details on the length of minimum cost. Using group-theory algebraic software GAP [22] and apply the optimization rules to calculate the quantum cost of reversible circuits show that the average cost of reversible circuits synthesized with NCT library is 11.459.

Table 2: Number of circuits with minimum length

Mini-length	*NCT*-Circuits	*NCT*-Circuits[14]	*NCT*-Circuits[13]
0	1	1	1
1	12	12	12
2	102	102	102
3	625	625	625
4	2780	2780	2780
5	8921	8921	8921
6	17049	17049	17049
7	10253	10253	10253
8	577	577	577
Total	40320	40320	40320
Average	5.865	5.865	5.865

Table 4: Number of circuits with minimum cost.

Mini-Cost	*NCT*-Circuits	*NCT*-Circuits[14]	*NCT*-Circuits[13]
0	8	8	8
1	48	48	48
2	192	192	192
3	408	408	408
4	528	480	480
5	541	288	288
6	1127	592	592
7	2413	1962	2016
8	3566	3887	4128
9	2430	2916	2496
10	2545	1299	672
11	5257	3683	2880
12	6260	7221	7488
13	3983	6059	7488
14	1672	1465	384
15	3389	3562	1600
16	4102	4201	5568
17	1851	2049	3584
Total	40320	40320	40320
Average	11.459	11.769	11.983

Table 3: There are number of circuits with minimum length and cost.

Mini-Length	Cost	#circuits	Mini-Length	Cost	#circuits	Mini-Length	Cost	#circuits	Mini-Length	Cost	#circuits
1	0	3	4	4	78	5	16	285	7	11	789
1	1	6	4	5	101	5	17	29	7	12	1257
1	5	3	4	6	274	5	18	14	7	13	1644
2	0	3	4	7	668	5	19	36	7	14	904
2	1	24	4	8	280	5	20	12	7	15	1104
2	2	24	4	9	96	6	4	45	7	16	1663
2	4	3	4	10	310	6	5	168	7	17	1254
2	5	18	4	11	384	6	6	129	7	18	380
2	6	24	4	12	134	6	7	492	7	19	158
2	9	3	4	13	10	6	8	1347	7	20	66
2	10	3	4	14	56	6	9	1671	7	21	27
3	0	1	4	15	48	6	10	845	7	22	2
3	1	18	4	16	6	6	11	2032	7	23	1
3	2	117	4	18	1	6	12	2986	7	24	4
3	3	51	4	19	1	6	13	2457	7	25	1
3	4	12	5	3	75	6	14	839	8	9	3
3	5	52	5	4	375	6	15	1376	8	10	2
3	6	155	5	5	101	6	16	1588	8	11	17
3	7	105	5	6	326	6	17	752	8	12	25
3	8	1	5	7	835	6	18	88	8	13	19
3	9	25	5	8	1639	6	19	143	8	14	46
3	10	55	5	9	523	6	20	75	8	15	89
3	11	27	5	10	714	6	21	16	8	16	171
3	13	1	5	11	1390	7	6	14	8	17	136
3	14	4	5	12	1413	7	7	78	8	18	46
3	15	1	5	13	383	7	8	147	8	19	20
4	2	51	5	14	273	7	9	465	8	20	2
4	3	282	5	15	496	7	10	295	8	21	1

Table 5: There are number of circuits with minimum cost and length.

Mini-Cost	Length	#circuits	Mini-Cost	Length	#circuits	Mini-Cost	Length	#circuits	Mini-Cost	Length	#circuits
0	1	3	6	7	42	11	4	228	14	9	127
0	2	3	6	8	2	11	5	1020	14	10	60
0	3	1	7	3	69	11	6	2026	14	11	13
1	1	6	7	4	511	11	7	1443	14	12	2
1	2	24	7	5	916	11	8	441	15	3	1
1	3	18	7	6	755	11	9	77	15	4	31
2	2	24	7	7	155	11	10	4	15	5	276
2	3	117	7	8	7	12	4	74	15	6	891
2	4	51	8	3	1	12	5	812	15	7	1184

3	3	51	8	4	174	12	6	2366	15	8	700
3	4	282	8	5	1283	12	7	2018	15	9	273
3	5	75	8	6	1531	12	8	799	15	10	33
4	2	3	8	7	513	12	9	186	16	4	3
4	3	12	8	8	56	12	10	5	16	5	122
4	4	78	8	9	8	13	3	1	16	6	756
4	5	387	9	2	3	13	4	8	16	7	1321
4	6	48	9	3	22	13	5	170	16	8	1110
5	1	3	9	4	74	13	6	1378	16	9	670
5	2	18	9	5	332	13	7	1395	16	10	120
5	3	57	9	6	1318	13	8	618	17	5	11
5	4	120	10	2	3	13	9	292	17	6	203
5	5	140	10	3	43	13	10	109	17	7	424
5	6	202	10	4	228	13	11	12	17	8	323
5	7	1	10	5	618	14	3	4	17	9	369
6	2	18	10	6	908	14	4	42	17	10	353
6	3	123	10	7	579	14	5	180	17	11	155
6	4	298	10	8	153	14	6	445	17	12	13
6	5	429	10	9	13	14	7	545			
6	6	215	11	3	18	14	8	254			

V. INTEGRATION OF IRREVERSIBLE BOOLEAN FUNCTIONS IN A REVERSIBLE CIRCUIT

This section shows that if a set of irreversible Boolean function can be integrated by an even parity permutation that has a cycle representation, then the set of irreversible Boolean functions can be realized by a reversible circuit using NCT library. This provides a concrete realizations for several families of Boolean functions such as $AND(x_1 \wedge x_2)$, $OR(x_1 \vee x_2)$, $NOT(\neg x_1)$, $XOR(x_1 \oplus x_2)$, $NAND(x_1 \uparrow x_2)$, $NOR(x_1 \downarrow x_2)$. For the sake of readability, this will be written shortly as $AND, OR, NOT, XOR, NAND,$ and NOR respectively.

There exist 8 basics combination of three different irreversible Boolean functions which are $\{\{AND, OR, NOT\}, \{AND, NOT, XOR\}, \{AND, NOT, NOR\}, \{OR, NOT, XOR\}, \{OR, NOT, NAND\}, \{NOT, XOR, NAND\}, \{NOT, XOR, NOR\}, \{NOT, NAND, NOR\}\}$. Each basic combination of three different irreversible Boolean functions has 6 possible permutations, and then we have totally 48 possible combinations of three different irreversible Boolean functions. For example, the reversible circuit to implement the set $\{AND, OR, NOT\}$ has six different forms, i.e. (AND, OR, NOT) means that the first output line will be $AND(x_1 \wedge x_2)$, the second output line will be $OR(x_1 \vee x_2)$ and the third line will be $NOT(\neg x_1)$ which is different from (AND, NOT, OR) which means that the first output line will be $AND(x_1 \wedge x_2)$, the second output line be $NOT(\neg x_1)$ and the third output line will be $OR(x_1 \vee x_2)$ as shown in Fig.10.

Setting the input to $(x_1, x_2, 0)$, i.e. the third bit is initialized to 0, all the possible combinations of three different irreversible Boolean functions can be integrated by an even parity permutation that has a cycle representation and can be realized by reversible circuit as will be shown in Table 6. For example, the combination of (AND, OR, NOT) can be integrated by a cyclic permutation equal (1, 2) (3, 4, 5) and can be realized by reversible circuit $[C_{12}^3, C_{13}^3, T_{321}^3, N_3^3, C_{12}^3]$ with best minimum cost equal 8 as shown in Fig.10.

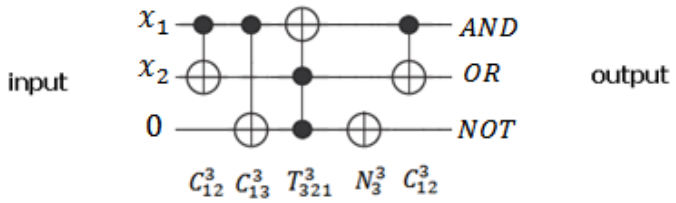

Figure 10: The reversible circuit realizes the combination of (AND, OR, NOT) with the input $(x_1, x_2, 0)$.

Setting the input to $(x_1, x_2, 1)$, i.e. the third bit is initialized to 1, all the possible combinations of three different irreversible Boolean functions can be integrated by an even parity permutation that has a cycle representation and can be realized by reversible circuit as will be shown in Table 7. For example, the combination of three different irreversible Boolean functions (OR, AND, NOT) can be integrated by a cyclic permutation equal (4, 6, 5) (7, 8) and can be realized by reversible circuit $[C_{12}^3, C_{13}^3, T_{321}^3, C_{12}^3]$ with best minimum cost equal 8 as shown in Fig.11.

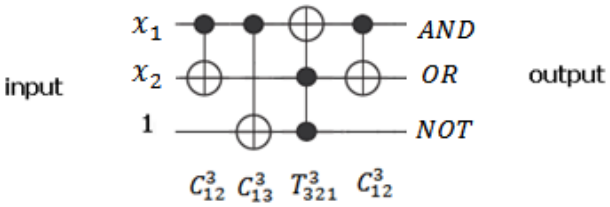

Figure 11: The reversible circuit realizes the combination of (AND, OR, NOT) with the input $(x_1, x_2, 1)$.

All the possible combinations of three different irreversible Boolean functions with the input $(x_1, x_2, 1)$ realize the reversible circuits with best minimum cost and length, while all the possible combinations of three different irreversible Boolean functions with different arrangement with the input $(x_1, x_2, 0)$ realize the reversible circuits with worst cost and length as shown in Table 8, i.e. setting the input vector to $(x_1, x_2, 1)$ gives better results.

Table 6: All the possible Reversible circuits' realizations of Boolean functions combination with input $(x_1, x_2, 0)$.

All possible Combination	Cyclic permutation	Reversible circuit	Quantum cost	Circuit Length
(AND, OR, NOT)	(1,2)(3,4,5)	$[C_{12}^3, C_{13}^3, T_{321}^3, N_3^3, C_{12}^3]$	8	5
(AND, NOT, OR)	(1,3,4)(2,5)(6,7)	$[C_{13}^3, C_{23}^3, C_{32}^3, T_{321}^3, T_{123}^3, N_2^3]$	13	6
(OR, AND, NOT)	(1,2)(3,6)	$[N_3^3, C_{12}^3, T_{123}^3, T_{321}^3, C_{12}^3, C_{23}^3]$	13	6
(OR, NOT, AND)	(1,3,7,6)	$[C_{32}^3, N_3^3, T_{123}^3, T_{321}^3, N_2^3, T_{132}^3, N_3^3]$	16	7
(NOT, AND, OR)	(1,5,2)(3,6)(4,7)	$[N_1^3, C_{12}^3, T_{321}^3, T_{123}^3, C_{32}^3, N_3^3]$	12	6
(NOT, OR, AND)	(1,5,3,7,4)	$[C_{31}^3, N_3^3, T_{123}^3, T_{132}^3, N_1^3, N_3^3]$	10	6
(AND, NOT, XOR)	(1,3,4)(2,7,5)	$[N_2^3, N_3^3, T_{321}^3, N_3^3, C_{13}^3, T_{321}^3, N_3^3, C_{32}^3]$	12	8
(AND, XOR, NOT)	(1,2)(3,4,7,5)	$[C_{13}^3, T_{132}^3, T_{321}^3, N_3^3]$	11	4
(NOT, AND, XOR)	(1,5,2)(3,6,7)	$[N_3^3, C_{31}^3, T_{132}^3, N_3^3, C_{23}^3, T_{132}^3, N_3^3]$	12	7
(NOT, XOR, AND)	(1,5,3,7,2)	$[N_2^3, N_3^3, T_{132}^3, N_3^3, C_{31}^3, T_{123}^3, N_1^3, N_2^3]$	11	8
(XOR, AND, NOT)	(1,2)(3,6,7)	$[N_3^3, T_{321}^3, T_{132}^3, N_3^3, C_{23}^3, T_{132}^3, N_3^3]$	15	7
(XOR, NOT, AND)	(1,3,7,2)	$[N_1^3, N_3^3, T_{321}^3, N_2^3, T_{132}^3, N_3^3, T_{123}^3, N_1^3, N_2^3]$	15	9
(AND, NOT, NOR)	(1,4,7,5)	$[N_1^3, N_3^3, T_{321}^3, T_{132}^3, N_3^3, T_{123}^3, C_{31}^3]$	15	7
(AND, NOR ,NOT)	(1,4,7,5)(2,3)	$[C_{12}^3, C_{13}^3, T_{321}^3, N_2^3, T_{132}^3, N_3^3]$	12	6
(NOT, AND, NOR)	(1,6,7,3,5)	$[N_2^3, N_3^3, C_{31}^3, T_{123}^3, N_2^3, T_{132}^3, N_3^3]$	11	7
(NOT, NOR, AND)	(1,7,2,3,5)	$[N_2^3, C_{12}^3, C_{31}^3, T_{123}^3, T_{132}^3, N_1^3]$	11	6
(NOR, AND, NOT)	(1,6,5)(2,7,3	$[N_1^3, C_{32}^3, T_{123}^3, N_2^3, C_{32}^3, C_{31}^3, T_{123}^3, N_2^3]$	13	8
(NOR, NOT, AND)	(1,7,2,5)	$[N_2^3, N_3^3, C_{21}^3, T_{132}^3, N_3^3, T_{123}^3, T_{321}^3, N_2^3]$	16	8
(OR, NOT, XOR)	(1,3,8)(5,6,7)	$[N_3^3, C_{13}^3, T_{321}^3, T_{123}^3, C_{32}^3, N_3^3]$	12	6
(OR, XOR, NOT)	(1,2)(3,8)(5,7)	$[T_{321}^3, N_3^3, T_{132}^3, C_{13}^3, T_{321}^3]$	14	5
(NOT, OR, XOR)	(1,5,4)(3,8,7)	$[C_{31}^3, N_3^3, T_{132}^3, C_{23}^3, T_{132}^3, N_1^3, N_3^3]$	12	7
(NOT, XOR, OR)	(1,5,4)(2,7)(3,8)	$[N_1^3, C_{12}^3, C_{32}^3, T_{321}^3, N_3^3, T_{123}^3, N_2^3]$	12	7
(XOR, OR, NOT)	(1,2)(3,8,5,7)	$[N_3^3, T_{321}^3, C_{12}^3, C_{23}^3, T_{132}^3]$	12	5
(XOR, NOT, OR)	(1,3,8)(2,7)(5,6)	$[N_1^3, T_{132}^3, N_3^3, C_{21}^3, C_{12}^3, T_{123}^3, N_1^3]$	12	7
(OR, NOT, NAND)	(1,4)(3,8)(5,6,7)	$[N_1^3, C_{21}^3, C_{13}^3, T_{321}^3, C_{32}^3, N_3^3, T_{123}^3, N_1^3]$	13	8
(OR, NAND, NOT)	(1,4)(3,8)(5,7)	$[N_1^3, T_{123}^3, N_2^3, C_{32}^3, T_{321}^3, T_{321}^3, N_1^3]$	16	7
(NOT, OR, NAND)	(1,6)(3,8,7)(4,5)	$[N_1^3, C_{12}^3, N_1^3, T_{321}^3, N_3^3, T_{123}^3, N_1^3, C_{32}^3]$	12	8
(NOT, NAND, OR)	(1,7,2)(3,8)(4,5)	$[N_1^3, N_2^3, T_{321}^3, T_{123}^3, C_{12}^3, C_{32}^3, N_3^3]$	10	7
(NAND, OR, NOT)	(1,6)(3,8,5,7)	$[C_{13}^3, T_{123}^3, N_1^3, C_{31}^3, T_{132}^3, C_{13}^3]$	11	6
(NAND, NOT, OR)	(1,7,2)(3,8)(5,6)	$[N_3^3, C_{21}^3, C_{31}^3, T_{132}^3, T_{123}^3, C_{31}^3]$	12	6
(NOT, XOR, NAND)	(1,6,7)(3,8)(4,5)	$[C_{32}^3, T_{321}^3, N_3^3, T_{123}^3, C_{12}^3, N_1^3]$	10	6
(NOT, NAND, XOR)	(1,7)(3,8)(4,5)	$[N_1^3, T_{123}^3, N_1^3, N_2^3, T_{321}^3, C_{21}^3, T_{123}^3, N_1^3]$	14	8
(XOR, NOT, NAND)	(1,4,7)(3,8)(5,6)	$[N_2^3, N_3^3, C_{21}^3, T_{132}^3, T_{123}^3, N_1^3, N_2^3]$	10	7
(XOR, NAND, NOT)	(1,4,5,7)(3,8)	$[N_1^3, T_{123}^3, C_{21}^3, N_2^3, C_{32}^3, T_{123}^3, N_1^3]$	11	7
(NAND,NOT,XOR)	(1,7)(3,8)(5,6)	$[N_1^3, N_3^3, T_{321}^3, T_{132}^3, N_1^3, C_{13}^3, T_{321}^3, N_3^3]$	15	8
(NAND,XOR,NOT)	(1,6,5,7)(3,8)	$[N_3^3, T_{132}^3, C_{31}^3, C_{13}^3, T_{321}^3, N_3^3]$	11	6
(NOT,XOR,NOR)	(1,6,5,3,7)	$[N_2^3, N_3^3, T_{132}^3, C_{31}^3, N_3^3, T_{123}^3, N_2^3]$	10	7
(NOT, NOR,XOR)	(1,7)(2,5)(3,6)	$[N_2^3, T_{123}^3, N_1^3, N_2^3, C_{32}^3, T_{123}^3, N_2^3, T_{321}^3]$	16	8
(XOR, NOT, NOR)	(1,4,3,7)	$[N_1^3, N_3^3, T_{321}^3, T_{132}^3, N_3^3, T_{123}^3, N_1^3]$	14	7
(XOR, NOR, NOT)	(1,4,7)(3,6)	$[N_2^3, T_{123}^3, N_1^3, T_{321}^3, C_{32}^3, C_{13}^3, T_{321}^3]$	15	7
(NOR, NOT, XOR)	(1,7)(2,5)(3,4)	$[N_2^3, N_3^3, T_{321}^3, N_3^3, C_{13}^3, T_{132}^3, T_{321}^3, N_2^3, N_3^3]$	16	9
(NOR, XOR, NOT)	(1,6,7)(3,4,5)	$[N_1^3, N_2^3, T_{321}^3, C_{13}^3, C_{32}^3, T_{321}^3]$	12	6
(NOT, NAND, NOR)	(1,8,5,3,7)	$[N_1^3, C_{12}^3, C_{31}^3, T_{123}^3, N_2^3, T_{132}^3]$	12	6

(NOT, NOR, NAND)	(1,8,7)(2,5)(3,6)	$[N_2^3, T_{123}^3, N_1^3, C_{32}^3, T_{321}^3, C_{13}^3]$	12	6
(NAND, NOT, NOR)	(1,8,3,7)	$[N_1^3, N_3^3, C_{21}^3, T_{132}^3, N_3^3, T_{123}^3, N_1^3, T_{321}^3]$	16	8
(NAND, NOR, NOT)	(1,8,7)(3,6)	$[N_2^3, T_{123}^3, N_1^3, C_{21}^3, C_{31}^3, C_{13}^3]$	8	6
(NOR, NOT, NAND)	(1,8,7)(2,5)(3,4)	$[C_{23}^3, N_2^3, T_{132}^3, C_{23}^3, C_{21}^3, N_2^3, T_{132}^3]$	13	7
(NOR, NAND, NOT)	(1,8,7)(3,4,5)	$[N_1^3, T_{123}^3, N_2^3, C_{32}^3, C_{31}^3, T_{123}^3]$	12	6

Table 7: All the possible Reversible circuits' realizations of Boolean functions combination with input$(x_1, x_2, 1)$.

All possible Combination	Cyclic permutation	Reversible circuit	Quantum cost	Circuit Length
(AND, OR, NOT)	(3,6)(7,8)	$[C_{23}^3, C_{21}^3, T_{132}^3, T_{123}^3, C_{21}^3]$	11	5
(AND, NOT, OR)	(2,3,8,6)	$[N_1^3, C_{32}^3, T_{123}^3, T_{321}^3, T_{132}^3, N_1^3]$	15	6
(OR, AND, NOT)	(4,6,5)(7,8)	$[C_{12}^3, C_{13}^3, T_{321}^3, C_{12}^3]$	8	4
(OR, NOT, AND)	(2,3)(4,7)(5,8,6)	$[N_1^3, N_3^3, C_{21}^3, C_{32}^3, T_{123}^3, N_1^3, C_{12}^3, T_{321}^3, N_2^3]$	13	7
(NOT, AND, OR)	(2,5,8,4,6)	$[N_2^3, C_{31}^3, T_{123}^3, N_2^3, T_{132}^3]$	11	5
(NOT, OR, AND)	(2,5)(3,6)(4,7,8)	$[N_1^3, C_{12}^3, C_{23}^3, T_{321}^3, T_{123}^3, C_{32}^3, N_3^3]$	13	7
(AND, NOT, XOR)	(2,3,6)(5,8)	$[C_{23}^3, C_{12}^3, T_{321}^3, C_{32}^3, C_{23}^3]$	7	5
(AND, XOR ,NOT)	(3,6)(5,8)	$[N_3^3, T_{321}^3, C_{12}^3, C_{13}^3, T_{321}^3, N_3^3]$	12	6
(NOT, AND, XOR)	(2,5,4,6)(3,8)	$[C_{31}^3, C_{13}^3, C_{23}^3, T_{132}^3, T_{321}^3]$	13	5
(NOT, XOR, AND)	(2,5,4,7,8)(3,6)	$[N_3^3, T_{321}^3, N_2^3, C_{12}^3, T_{321}^3, T_{123}^3, N_1^3, N_2^3]$	16	8
(XOR, AND, NOT)	(3,8)(4,6,5)	$[C_{13}^3, C_{21}^3, T_{132}^3, T_{321}^3, T_{123}^3]$	17	5
(XOR, NOT, AND)	(2,3,4,7,8)(5,6)	$[N_1^3, T_{321}^3, N_2^3, T_{132}^3, N_3^3, T_{123}^3, N_1^3, N_2^3]$	15	8
(AND, NOT, NOR)	(1,6)(2,4,3)(5,8)	$[N_1^3, N_3^3, C_{21}^3, C_{12}^3, C_{32}^3, T_{123}^3, T_{321}^3]$	13	7
(AND, NOR ,NOT)	(1,6)(2,4)(5,8)	$[N_2^3, N_3^3, T_{123}^3, T_{321}^3, N_3^3, C_{32}^3, T_{123}^3, N_2^3]$	16	8
(NOT, AND, NOR)	(1,2,6)(3,8)(4,5)	$[N_1^3, N_3^3, C_{12}^3, T_{321}^3, T_{123}^3, C_{32}^3]$	12	6
(NOT, NOR, AND)	(1,4,2,6)(3,8)	$[N_1^3, N_3^3, T_{123}^3, T_{132}^3, C_{31}^3, C_{13}^3]$	10	6
(NOR, AND, NOT)	(1,6)(2,7,8)(4,5)	$[N_3^3, T_{321}^3, T_{123}^3, N_1^3, C_{12}^3, C_{32}^3]$	12	6
(NOR, NOT, AND)	(1,6)(2,7,8)(3,4)	$[N_3^3, C_{23}^3, T_{132}^3, N_1^3, N_3^3, C_{23}^3, C_{21}^3, T_{132}^3, N_3^3]$	13	9
(OR, NOT, XOR)	(2,3)(4,8,5)	$[C_{23}^3, C_{12}^3, C_{32}^3, C_{23}^3, T_{321}^3]$	9	5
(OR, XOR, NOT)	(4,8,5)(6,7)	$[C_{12}^3, C_{13}^3, T_{321}^3]$	7	3
(NOT, OR, XOR)	(2,5)(3,6,4,8)	$[C_{13}^3, C_{21}^3, C_{31}^3, C_{13}^3, T_{132}^3, T_{321}^3]$	14	6
(NOT, XOR, OR)	(2,5,6,4,8)	$[N_2^3, T_{132}^3, C_{31}^3, T_{123}^3, N_2^3]$	10	5
(XOR, OR, NOT)	(3,4,8)(6,7)	$[T_{321}^3, C_{23}^3, T_{132}^3, T_{123}^3]$	14	4
(XOR, NOT, OR)	(2,3,4,8)	$[N_1^3, T_{321}^3, T_{132}^3, T_{123}^3, N_1^3]$	13	5
(OR, NOT, NAND)	(2,4,8,5)	$[N_2^3, C_{32}^3, T_{123}^3, T_{321}^3, N_2^3, T_{132}^3]$	16	6
(OR, NAND, NOT)	(2,4,8,5)(6,7)	$[N_2^3, C_{13}^3, T_{321}^3, N_2^3, C_{12}^3, T_{321}^3]$	12	6
(NOT, OR, NAND)	(2,6,4,8,3)	$[N_1^3, C_{31}^3, T_{123}^3, T_{132}^3, N_1^3]$	10	5
(NOT, NAND, OR)	(2,7,6,4,8)	$[C_{32}^3, C_{31}^3, T_{123}^3, T_{132}^3]$	11	4
(NAND, OR, NOT)	(2,6,7)(3,4,8)	$[C_{23}^3, T_{132}^3, C_{21}^3, C_{31}^3, T_{123}^3]$	13	5
(NAND, NOT, OR)	(2,7,4,8)	$[C_{32}^3, C_{31}^3, T_{123}^3, T_{321}^3, T_{132}^3]$	16	5
(NOT, XOR, NAND)	(1,2,6,4,8)	$[N_1^3, N_2^3, C_{31}^3, T_{132}^3, T_{123}^3, N_1^3, N_2^3]$	10	7
(NOT, NAND, XOR)	(1,6,4, 8)(2,7)	$[C_{12}^3, N_1^3, C_{23}^3, T_{321}^3, T_{132}^3, N_3^3]$	11	6
(XOR, NOT, NAND)	(1,2,4,8)	$[N_1^3, T_{321}^3, N_1^3, T_{132}^3, T_{123}^3, N_1^3, N_2^3]$	14	7
(XOR, NAND, NOT)	(1,2,4,8)(6,7)	$[T_{321}^3, C_{12}^3, C_{32}^3, C_{23}^3, T_{132}^3, N_3^3]$	13	6
(NAND, NOT, XOR)	(1,4,8)(2,7)	$[N_1^3, C_{21}^3, C_{12}^3, N_1^3, C_{13}^3, T_{321}^3, N_3^3]$	8	7
(NAND, XOR, NOT)	(1,4,8)(2,6,7)	$[N_2^3, N_3^3, T_{321}^3, C_{13}^3, N_1^3, C_{12}^3, T_{321}^3, N_3^3]$	12	8
(NOT, XOR, NOR)	(1,8)(2,6,3)(4,7)	$[N_2^3, C_{31}^3, N_3^3, T_{123}^3, C_{12}^3, T_{321}^3]$	10	6
(NOT, NOR, XOR)	(1,8)(2,7,4,6)	$[N_3^3, C_{12}^3, T_{321}^3, C_{23}^3, T_{132}^3, N_1^3, C_{12}^3]$	12	7
(XOR,NOT, NOR)	(1,8)(2,4,7)(5,6)	$[N_1^3, N_2^3, N_3^3, T_{132}^3, T_{123}^3, C_{21}^3, C_{12}^3]$	10	7
(XOR, NOR, NOT)	(1,8)(2,4,6,5)	$[N_1^3, C_{21}^3, T_{132}^3, C_{31}^3, N_3^3, C_{23}^3, T_{132}^3]$	12	7
(NOR,NOT,XOR)	(1,8)(2,7,6)	$[N_2^3, C_{12}^3, C_{23}^3, C_{21}^3, C_{12}^3, T_{321}^3, N_2^3]$	9	7
(NOR, XOR, NOT)	(1,8)(2,6,3)	$[N_1^3, C_{31}^3, C_{12}^3, C_{13}^3, N_1^3, T_{321}^3]$	8	6
(NOT, NAND, NOR)	(1,2,8)(3,6)(4,7)	$[N_1^3, N_2^3, N_3^3, T_{321}^3, T_{123}^3, C_{12}^3, C_{32}^3]$	10	7
(NOT, NOR, NAND)	(1,4,6,2,8)	$[N_1^3, N_2^3, C_{31}^3, T_{123}^3, C_{32}^3, T_{123}^3, N_1^3, N_2^3]$	12	8
(NAND, NOT, NOR)	(1,2,8)(4,7)(5,6)	$[C_{21}^3, C_{31}^3, T_{132}^3, T_{123}^3, C_{31}^3, N_3^3]$	12	6
(NAND, NOR, NOT)	(1,2,8)(4,6,5)	$[N_2^3, T_{123}^3, N_1^3, C_{32}^3, C_{31}^3, T_{123}^3, N_1^3, N_2^3]$	12	8
(NOR, NOT, NAND)	(1,6,2,8)	$[N_1^3, T_{321}^3, N_2^3, T_{132}^3, T_{123}^3, N_1^3, N_2^3, C_{31}^3]$	15	8
(NOR, NAND, NOT)	(1,2,8)(3,6)	$[N_1^3, T_{123}^3, C_{32}^3, N_3^3, C_{31}^3, C_{13}^3]$	8	6

Table 8: Comparison between the possible combinations of Boolean functions which realize the reversible circuits with best minimum cost and length while the inputs $(x_1, x_2, 0)$ and $(x_1, x_2, 1)$.

Input $(x_1, x_2, 0)$			
Basic Possible Combinations	Reversible Circuits implementation	Mini-Cost	Length
(AND, OR, NOT)	$[C_{12}^3, C_{13}^3, T_{321}^3, N_3^3, C_{12}^3]$	8	5
(AND, XOR ,NOT)	$[C_{13}^3, T_{132}^3, T_{321}^3, N_3^3]$	11	4
(NOT, NOR,AND)	$[N_2^3, C_{12}^3, C_{31}^3, T_{123}^3, T_{132}^3, N_1^3]$	11	6
(XOR, OR, NOT)	$[N_3^3, T_{321}^3, C_{12}^3, C_{23}^3, T_{132}^3]$	12	5
(NOT, NAND,OR)	$[N_1^3, N_2^3, T_{321}^3, T_{123}^3, C_{12}^3, C_{32}^3, N_3^3]$	10	7
(XOR, NOT, NAND)	$[N_2^3, N_3^3, C_{21}^3, T_{132}^3, T_{123}^3, N_1^3, N_2^3]$	10	7
(NOT, XOR, NOR)	$[N_2^3, N_3^3, T_{132}^3, C_{31}^3, N_3^3, T_{123}^3, N_2^3]$	10	7
(NAND, NOR, NOT)	$[N_2^3, T_{123}^3, N_1^3, C_{21}^3, C_{31}^3, C_{13}^3]$	8	6
Input $(x_1, x_2, 1)$			
Basic Possible Combinations	Reversible Circuits implementation	Mini-Cost	Length
(OR, AND, NOT)	$[C_{12}^3, C_{13}^3, T_{321}^3, C_{12}^3]$	8	4
(AND, NOT, XOR)	$[C_{23}^3, C_{12}^3, T_{321}^3, C_{32}^3, C_{23}^3]$	7	5
(NOT, NOR, AND)	$[N_1^3, N_3^3, T_{123}^3, T_{132}^3, C_{31}^3, C_{13}^3]$	10	6
(OR, XOR, NOT)	$[C_{12}^3, C_{13}^3, T_{321}^3]$	7	3
(NOT, OR, NAND)	$[N_1^3, C_{31}^3, T_{123}^3, T_{132}^3, N_1^3]$	10	5
(NAND ,NOT, XOR)	$[N_1^3, C_{21}^3, C_{12}^3, N_1^3, C_{13}^3, T_{321}^3, N_3^3]$	8	7
(NOR, XOR, NOT)	$[N_1^3, C_{31}^3, C_{12}^3, C_{13}^3, N_1^3, T_{321}^3]$	8	6
(NOR, NAND, NOT)	$[N_1^3, T_{123}^3, C_{32}^3, N_3^3, C_{31}^3, C_{13}^3]$	8	6

VI. CONCLUSION

By reducing the representation of the reversible circuit synthesis problem to permutation group, Schreier-Sims Algorithm for the strong generating set-finding problem is used to synthesize reversible circuits with minimal length. Applying the proposed optimization rules on the synthesized circuits gives better quantum cost to be 11.459 better than other results shown in the literature. The minimal length of a reversible circuit is obtained by using the main NCT library which the minimal quantum cost is obtained from using a sub library from the main NCT library.

Digital logic design is a well established area of research where classical Boolean functions in used in the construction process. Classical Boolean functions are mainly irreversible and cannot be used directly in the reversible circuits' synthesis. It was shown how to integrate any three Boolean functions in a single reversible circuit using the NCT library. It was shown that the order of the Boolean function in the output vector affects the efficiency of the circuit. There are two ways to initialize the input vector, $(x_1, x_2, 0)$ and $(x_1, x_2, 1)$. It was shown that initializing the input vector to $(x_1, x_2, 1)$ gives better results with respect to the length and the quantum cost of the circuit.

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