IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)
e-ISSN: 2278-2834,p- ISSN: 2278-8735. Volume 7, Issue 2 (Jul. - Aug. 2013), PP 05-12
www.iosrjournals.org

Performance Analysis of Minimum Hop Source Routing Algorithm for Two Dimensional Torus Topology NOC Architecture under CBR Traffic

Dinesh Lekariya[1], Dr.M.A.Gaikwad[2]
[1,2]*Department of Mtech (Electronics), BDCOE/R.T.M.N.U University, INDIA*

Abstract: *Network on Chip has emerged as new paradigm for the system designers to design an on chip interconnection network. However, NOC presents a large amount of array of design parameters and decision that are sometimes difficult to tackle. Apart from these issues NOC presents a framework of communication for complex SOC and has been widely accepted by the industries and academia's. Today all the complex VLSI circuitry which requires an on chip communication between them are the part of NOC. The mature concepts of communication network such as routing algorithm, switching technique, flow and congestion control etc in the NOC are the important features on which the performance of NOC depends. This paper introduces the efficient source routing algorithm which generates the minimum hop from source to destination. Performance of NOC network in terms of latency and throughput for minimum hop source routing algorithm is also evaluated.*
Keywords: *Network on chip, routing algorithm, topology, traffic.*

I. Introduction

With the feature size of semiconductor technology reducing and intellectual properties (IP) cores increasing, on chip communication architectures have a great influence on the performance and area of System-on- Chip (SoC) design. Network-on-chip have been considered as a most promising candidate for the problem of on chip networks communication and widely accepted by many academician and designers. In NoC paradigm the processing elements are connected to each other through a network of interconnected routers or switches and they communicate among themselves using a wormhole switching technique. The topology, routing algorithm, switching technique, traffic patterns are important features that describes the behaviour of NoC. Topology suggests how the routers are interconnected to one another. Different interconnections have been described such as Mesh, Torus, Octagon, Hypercube, binary tree, butterfly etc. But the most commonly used and most widely accepted topologies are Mesh and Torus. Switching techniques determines that how the information flows through routers in the networks. Circuit switching, virtual cut through, packet switching and wormhole switching are various types of switching mechanism proposed in the literature. The most desirable technique is the wormhole switching in which packet is divided into small units known as flits. Flits stands for flow control units. Routing algorithm gives the idea about the path or the route followed by the flits. There are various ways in which the routing algorithms are classified. One of the methods suggests two classes of routing i.e source routing and distributed routing. In source routing, a source core precomputes the information about the whole path from the source to the destination; selects this information for a desired communication and provides it in packet header. In distributed routing, the header contains destination address only and the path is computed dynamically by participation of routers on the path. Design of a router also depends upon the type of routing. For example, router design for source routing will be simpler as compared to the router designed to handle distributed routing algorithm.

In order to route a packet through the network using source routing, a sender resource consults its routing table to get a complete path to the required destination. This path is then written in the dedicated field in the packet header. The packet is transferred to the network through network interface. The packet must follow the path while traversing through the network towards its destination. Each router that receives this packet reads the path field in the packet header and forwards it to the destined output port. Unlike a router used in distributed routing, this router does not require any extra computation for making routing decisions because the packets already contain pre-computed decisions. The various distributed routing algorithms are XY, odd-even, west first, negative first, north last etc. Some of algorithms mentioned above are either fully adaptive or partially adaptive. In adaptive routing multiple paths from source to destinations are possible. There also exists a partially adaptive routing algorithm which restricts a certain paths for communication. They are simple and easy to implement compared to adaptive routing algorithms.

This paper analyzes the torus NOC network under new routing strategy which is a combination of already existing routing algorithms. In section II analysis of work already done is presented. Section III describes our proposed routing algorithm while section IV concludes the paper.

II. Literature Review

Authors have proposed so many routing algorithms and implemented these routing strategies on both regular and irregular NOC topologies. But the most common and well known type of routing algorithm is XY also known as dimension order routing. Apart from these other routing algorithms such as odd-even, negative first, north last, west first types of partially adaptive and fully adaptive routing algorithms have been proposed in the literature. Wang Zhang and Ligang Hou [1] have proposed the most popular routing algorithm that is XY routing. Ge-Ming Chiu [2] has proposed in his paper a model for designing adaptive wormhole routing algorithms for meshes without virtual channels. The performance of the odd even turn model is evaluated under three traffic patterns namely uniform, transpose and hotspot. Maurizio Palesi et al. [3] have proposed in this paper a region based routing algorithm mechanism for 2-D mesh topology of NOC architecture. Region based routing is the mechanism which groups destinations into network region allowing an efficient implementations with logic blocks. Haibo Zhu et al. [4] have described in their paper, the performance of NOC networks for mesh topology using Negative-First routing algorithm. Wei Luo and Dong Xiang [5] have proposed in their paper an efficient adaptive deadlock free routing algorithm for torus network. Ran Manevich et al. [6] have proposed in their paper a centralized adaptive routing for NOC architecture. In this paper they introduce a novel paradigm of NOC centralized adaptive routing, and a specific design for mesh topology. The authors introduced Adaptive Toggle Dimension Order Routing (ATDOR). In ATDOR, for every source destination pairs the paths are adaptively switched between XY and YX. Jose Flich and Jose Duato [7] have proposed a logic based distributed routing for NOCs. They propose a new circuit that removes the need for using routing tables. Using this scheme any routing algorithm can be used on both regular and irregular topologies. Mr. Latit Arora et al. [8] have proposed, a framework for mesh interconnection network is designed to analyze the packet loss during the link is failed. M. Mirza-Aghatabar et al. [9] have discussed and compared two popular NOC topologies i.e., mesh and torus, in terms of different figures of merit e.g., latency, power consumption, and power/throughput ratio under different routing algorithms and two common traffic models, uniform and hotspot. XY routing is employed as an example of deterministic, Odd-Even and Negative First Turn models as examples of partially adaptive, and Duato as an example of fully adaptive routing algorithms.

All these NOC models with a combination of different topologies and routing algorithms with different parameters have been simulated and tested using different simulators. Various simulators have been developed in the past years which are able to design the NOC for various topologies and routing algorithms using different traffic patterns. Most of the simulators are design in SystemC. Noxim, Omnet++, Opnet, NIRGAM, NS2 etc. are some of the tools available for simulating NOC architectures. We have also developed a new routing strategy which is the combination of already existing routing algorithms. The description of our routing algorithm has been given in section III.

III. Minimum Hop Source Routing Algorithm

As already discussed in section II, the authors have proposed in the literature different routing algorithms out of which some are fully adaptive while others are partially adaptive. Source routing is deterministic type of algorithm where the entire path from source to destination is pre-computed and enclosed in the packet header. To find this path we have developed a strategy by using already existing routing algorithm.

We have designed this strategy to generate the minimum hops or shortest path for 2-D torus NOC network. We have taken some good points from these partially adaptive and fully adaptive routing algorithms and tried to blend these algorithms to form a new product. Here the network is first divided into odd and even columns. For even column we follow YX routing algorithm while for odd column we follow the XY routing algorithm. Thus every path is computed from above strategy and the logic is build to select the minimum distance or minimum hops route from source to Destination. The flow chart of above algorithm is as presented below:

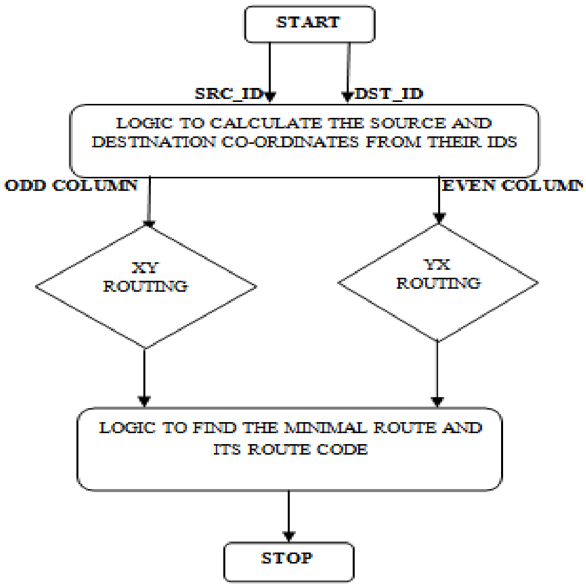

figure: 1

The logic for calculating the minimal distance is divided into three modules. In the first module logic is build for all corners nodes or tiles. In the second module the logic is build for border nodes or tiles while in the third module the logic is developed for intermediate nodes other than corner nodes and border nodes. Each node whether corner or border or intermediate has to satisfy four different conditions to move the packet in four different directions. These conditions are necessary and must be satisfied by the nodes so that the packets must follow the minimal path from source to destination. The logic to evaluate the minimal path is presented in the form of flow charts below.

1. Flow Chart of Corner Node

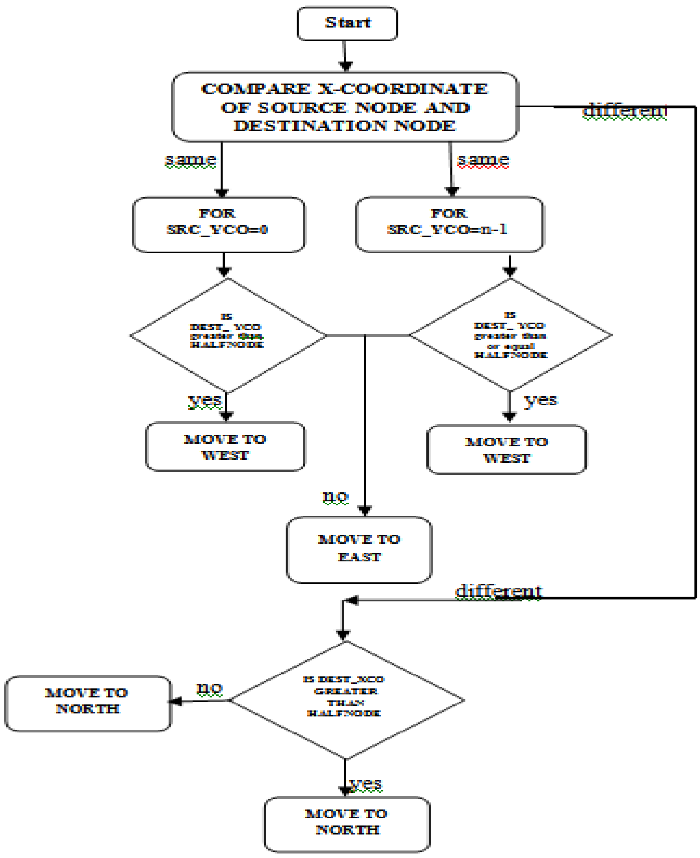

Figure: 2

2. Flow Charts of Border Nodes

a. For North and South Border

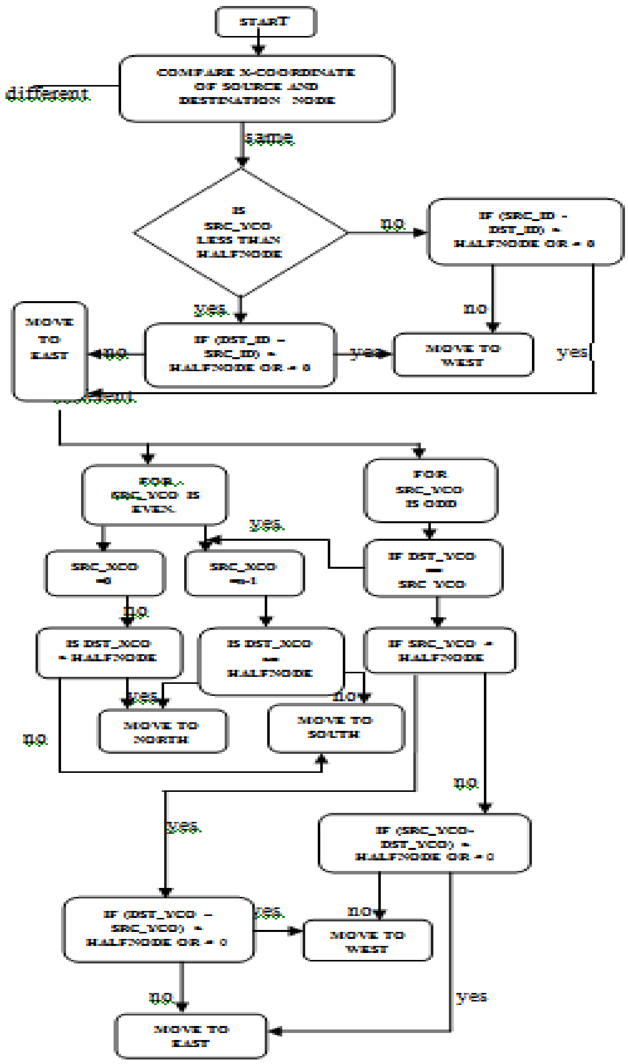

Figure: 3

b. For East and West Border

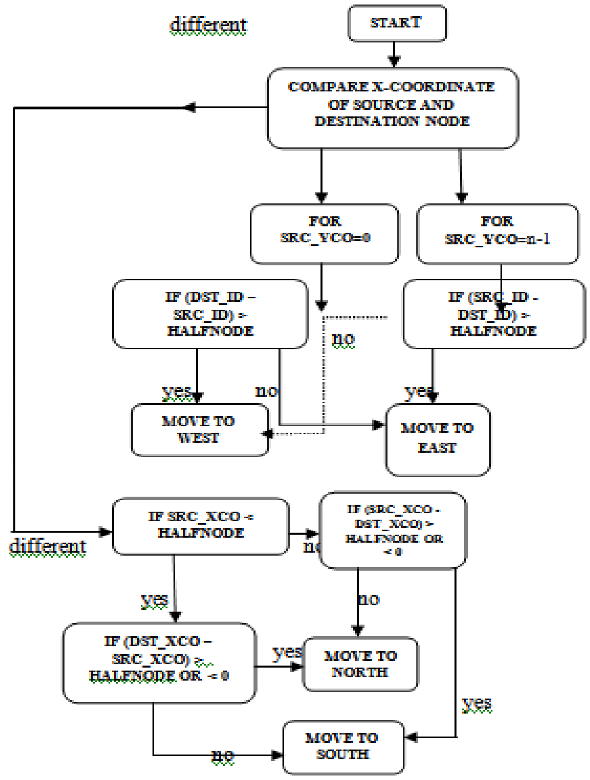

Figure: 4

3. Flow Chart of Intermediates Nodes

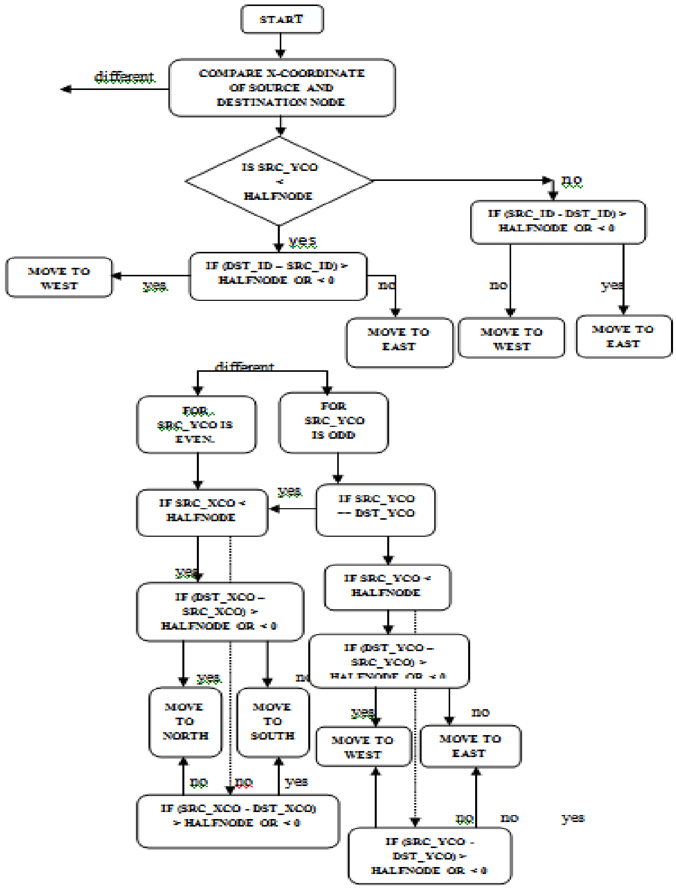

figure: 5

Where, SRC_XCO = Source x-coordinate
SRC_YCO = Source y-coordinate
DST_XCO = Destination x-coordinate
DST_YCO = Destination y-coordinate
SRC_ID = Source ID
DST_ID = Destination ID

HALF_NODE = $\frac{(n-1)}{2}$

Where n is the network size.

The above algorithm has designed for odd sizes of torus network only. For example the torus network of sizes 3x3, 5x5, and 7x7 and so on. Since in torus topology the corner and border nodes are horizontally and vertically connected our algorithm defines the best shortest route between source and destination. To simulate this routing algorithm we are using NIRGAM simulator. To implement the source routing algorithm the simulator requires a parameter called route code. In every direction i.e. north, south east, west and core has been allotted a unique number from 0 to 4. Depending upon the direction the packets are taking while traversing from source to destination the route code is calculated. For better illustration of above concept we explains the calculation of

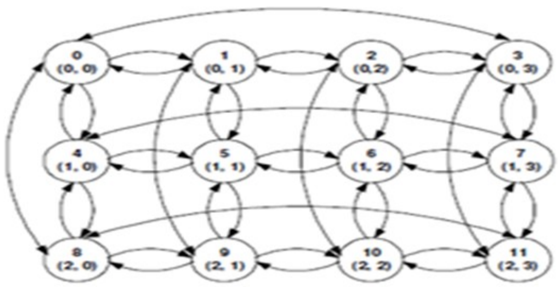

figure: 6 3x4 Torus network

Route code for sending packet from tile-9 to tile-1. Let say the path is calculated and is represented by the direction sequence W-> N-> E- > C. Route code can be obtained by writing the direction codes for these direction in the reverse order while maintaining the order of 3 bits in each direction codes. Thus, we have W(011)->N(000)->E(010)->C(100) =100 010 000 011 = 2179. This route code is used to route the packet from source to destination. In the above manner code has been written for four border nodes and intermediate nodes.

This strategy of routing not only provides the minimal path but also reduces the packet loss ratio. To implement the above routing algorithm the parameters are configured into a NIRGAM simulator. NIRGAM allows to experiment with various options available at every stage of design be it topology, virtual channels, switching technique, buffers parameters, routing mechanism or traffic generation application. The performance can be measured in terms of latency and throughput for the given set of choices. At an initial level a network size of 3x3 is taken. The parameters such as warm-up (defines the number of clock cycles before which the traffic generation begins) is set to be 5 clock cycles. The parameter TG-NUM (defines the clock cycles until which traffic is generated) is set initially at 300 and is varied at a step size of 300, so that the performance of algorithm can be measured in heavy traffic environment. The parameter SIM_NUM (defines the clock cycles for which simulation runs) is kept 10000 cycles. CBR traffic pattern application is attached to each tile. Packet size of 8 bytes and flit interval of 2 cycles is set. The bandwidth of channel i.e. load parameter is kept 50.

Number of virtual channels is four. The configuration files are simulated and following graphs and results are obtained.

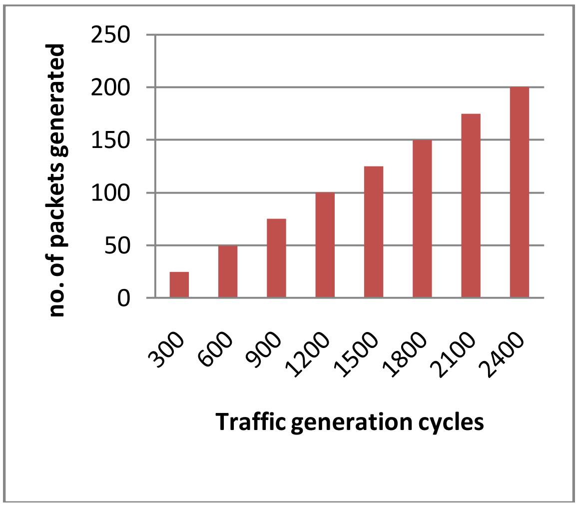

Figure: 7

Thus from the above graph it is clear that as we increase the traffic generation cycles in a step size of 300 the packets are increased by 25. Here when we increase the traffic on the network then also the packet loss is zero. Thus total number of flits generated is equal to the total number of flits received.

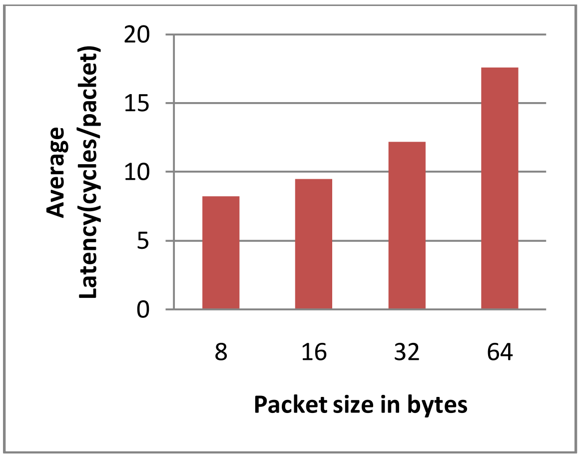

Figure: 8 Average Latency

The above graph is plotted between packet size and Latency per packet. Latency is the average delay required to transfer the packet from source to the required destination. In NOC, there are many factors that add to the latency including routing delay, channel occupancy, contention delay and overheads due to packetization and depacketization, flitization and deflitization, and synchronization among routers. It shows that as packet size increases latency increases. The maximum latency of 17.4547 clock cycles is obtained for a packet size of 64 bytes.

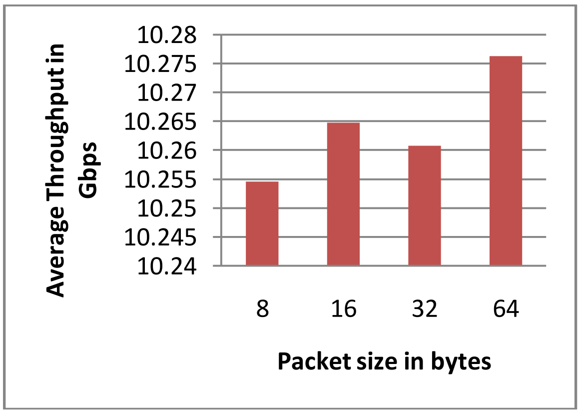

Figure: 9 Average throughput

Throughput gives the total number of packets reaching their destination per unit time. It is calculated as

$$T = \frac{Totalmessagecompleted \times Messagelength}{NumbersofIPcores \times Times}$$

Thus from the above graph it is clear that as we increase the packet size the latency is also increases which in turn increases the throughput.

IV. Conclusion

An efficient routing algorithm which generates minimum hop from source to destination for 2-d torus NOC architecture is presented in this paper. Performance analysis of this routing algorithm in terms of latency and throughput is also presented. Our algorithm has designed by using the concept of already existing routing algorithms but with a constrained of generating the minimum hop between source and destination and its analysis shows that it gives the better result for 3x3 torus network. The packet loss in a network is zero is the best feature of this routing algorithm. In our future work we will analysed this routing strategy for higher order of network sizes.

References

[1] Wang Zhang, Ligang Hou, Jinhui Wang, Shuqin Geng, Wuchen Wu in “Comparison Research between XY and Odd-Even Routing Algorithm of a 2-D 3X3 Mesh topology Network-on-Chip.

[2] Ge-Ming Chiu “The Odd Even Turn Model for Adaptive Routing” in IEEE Transaction on Parallel and Distributed System, Vol.11 No.7, July 2012.

[3] Andres Mejia, Maurizio Palesi, Jose Flich, Shashi Kumar “Region Based Routing: A Mechanism to Support Efficient Routing Algorithms in NOCs” in IEEE Transactions on VLSI System, Vol.17, No.3, March 2009.

[4] Haibo Zhu,Partha Pratim Pande, Cristian Grecu in “Performance Evaluation of Adaptive Routing Algorithms for achieving Fault Tolerance in NoC Fabrics” in IEEE transaction 2007.

[5] Wei Luo and Dong Xiang “An Efficient Adaptive Deadlock Free Routing Algorithm for Torus Networks”, in IEEE Transaction on Parallel And Distributed System, Vol. 23 No.5,May 2012.

[6] Ran Manevich et al. in “Centralized Adaptive Routing for NoCs” IEEE Computer Architecture Letters, Vol. 9, NO. 2, July-December 2010.

[7] Jose Flich and Jose Duato in “Logic Based Distributed Routing for NoCs” in IEEE Computer Architecture Letter, Vol.7, No. 1, January-June 2008.

[8] Lalit Kishore Arora, Rajkumar “Simulation and Analysis of Packet loss in Mesh Interconnection Networks” National Conference on Development of Reliable Information Systems, Techniques and Related Issues (DRISTI) 2012 Proceedings published in International Journal of Computer Applications® (IJCA) .

[9] M. Mirza-Aghatabar+,S.Koohi+, S. Hessabi*, M. Pedram†An “Empirical Investigation of Mesh and Torus NoC Topologies Under Different Routing Algorithms and Traffic Models” *Sharif University of Technology, Tehran, Iran,*

[10] Kanchan Manna, Santanu Chattopadhayay and Indranil Sen Gupta “Energy and Performance Evaluation of a Dimension Order Routing Algorithm for Mesh-of-Tree based Networks-on –Chip Architecture” in Annual IEEE India Conference 2010.

[11] Partha Pratim Pande, Cristian Grecu, Michael Jones, André Ivanov, Resve A. Saleh, “Performance Evaluation and Design Trade-Offs for Network-on-Chip Interconnect Architectures,” IEEE Trans. Computers, vol. 54, no. 8, pp 1025-1040, 2005.

[12] Yang Xiaoqiang, Li Junmin, Du Huimin and Han Jungang “A Node Encoding of Torus Topology and Its Improved Routing Algorithm” in JOURNAL OF COMMUNICATIONS, VOL. 3, NO. 6, NOVEMBER 2008.

[13] Naveen Choudhary “Bursty Communication Performance Analysis of Network-on-Chip with Diverse Traffic Permutations” International Journal of Soft Computing and Engineering (IJSCE) ISSN: 2231-2307, Volume-1, Issue-6, January 2012.

[14] J. Duato, ªA Theory of Fault-Tolerant Routing in Wormhole Networks,º IEEE Trans. Parallel and Distributed Systems, vol. 8, no. 8, pp. 790±802, Aug. 1997.

[15] J. Upadhyay, V. Varavithya, and P. Mohapatra, ªA Traffic- Balanced Adaptive Wormhole Routing Scheme for Two-Dimensional Meshes,º IEEE Trans. Computers, vol. 46, no. 2, pp. 190±197, Feb. 1997.

[16] Sun. Y. M., Yang. C. H., Chung Y. C and Hang. T. Y. 2004. An efficient deadlock-free tree-based routing algorithm for irregular wormhole-routed networks based on turn model. In proceedings of International Conference on Parallel Processing, vol. 1, 343-352.

[17] L. Benini and D. Bertozzi, “Xpipes: A Network-on-Chip Architecture for Gigascale Systems-on-Chip,” IEEE Circuits and Systems Magazine, vol. 4, no. 2, pp. 18-31, 2004.

[18] Saad Mubeen “Evaluation of Source Routing For Mesh Topology Network on Chip Platforms” Jonkoping Institute Of Technology 2009.

[19] Ahmad Patooghy and Seyed Ghassem Miremadi “XYX: A Power & Performance Efficient Fault-Tolerant Routing Algorithm for Network on Chip

[20] Ahmad M. Shafiee, Mehrdad Montazeri, and Mahdi Nikdast ,” An Innovational Intermittent Algorithm in Networks-On-Chip (NOC)”.

.