Amplitudo Modulation Data Rate Coherence To Ease Clock Regeneration For Underwater Data Communication

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Abstract: *Clock regeneration in synchronized data communication system has a very important role to extract the transmitted data correctly. According to very low bit rate with long zero and high signal distortion due to underwater propagation, the recovery would be very difficult, so that a certain technique must be applied to regenerate the clock easily. In this paper will be discussed a simply technical method to regenerate the clock. At the transmitter, amplitude modulator uses carrier frequency coherent with the data rate in the system. It is done by generating clock pulses as a fraction of the carrier wave. In addition to the coherency, modulation index of generated AM to supply underwater acoustic transducer is adjusted to be less than hundred percent. At the receiver, the weak signal is amplified by a frequency selective amplifier for carrier wave signal only. The output contains other weak signal and noise. To find the clear clock pulses, the signal is used as a frequency reference. A Voltage Controlled Oscillator, where its phase and frequency automatically controlled by frequency reference will generate a phase locked wave with the frequency as same as frequency clock at the transmitter side.*
Keywords: *Coherence, Clock Regeneration, underwater data communication.*

I. INTRODUCTION

Underwater communication system is an acoustic wave transmission system using water as propagation medium. The acoustic wave contains information to be delivered to receiver [1]. The information is either analog or digital. The digital form can be asynchronous or synchronous data. Regarding underwater data communication system, the no return to zero of asynchronous data is more difficult to be applied due to several factors, such as variation on acoustic power dumping caused by underwater dynamic, environmental noise [2], reverberation [3], etc. Thus, the return to zero form of synchronous or asynchronous data can be an option. While asynchronous system is using time slot of original data as a start and end with stop data, in synchronous data communication system, synchronization bits are used. Therefore, clock pulses are needed in transmitter and clock regeneration must be available in receiver [4].

The working frequency of underwater communication system with acoustic vibration usually ranges between tens of KHz to hundreds of KHz. On those low working frequency, the applicable data rate in underwater data communication system is also low. In order to recognize data that appropriate to the one from transmitter, it will need clock that coherent to transmitter's clock. The coherence between receiver's and transmitter's clocks is gained by continuously sending clock, which is using carrier frequency that is the multiple of clock frequency of transmitter. In addition, index of AM modulation is not made to 100%, which is several percent of carrier signal residual are still exist when data equal to zero.

II. Basic Configuration

Underwater data communication system with modulation amplitude consists of data processor, frequency carrier generator (f_c), the clock is generated by dividing frequency carrier f_c and acoustic transducer ultrasonic power amplifier in transmitter side. Whilst, in receiver, it consists of acoustic-electric conversion, selective low noise amplifier (LNA), demodulator, carrier separator, clock regenerator, and receiver's data processor. Figure 1 is a block diagram of underwater data communication system [5.2].

In transmitter's data processor, input data is analog signal from sensor signals called data channel. These analog signals are converted to digital signals by analog digital converter (ADC). ADC is putting every sensor data in a given time slot, determining transmit mode and data status, etc. In this process, the data is converted to line code, such as using pulse code modulation (PCM) system.
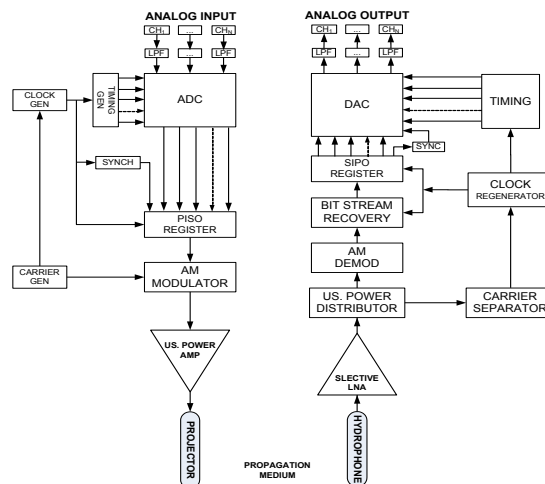
Fig. 1 Block Diagram of underwater AM data communication system [5,2].

To simplify the delivery process, those data are sent in serial format. The shift register of parallel in-serial out (PISO) is used to get serial data format. All clock pulses in the systems, also in data processor, are supplied by clock frequency which is derived from carrier generator. These digital data streams as the input of amplitude modulator, AM. The output level of AM modulator is low power, in the order of tens milliwatt. An ultrasonic power amplifier increases the ultrasonic power with level appropriate to projector requirement [5].

The data-modulated acoustic wave is projected to the water by a projector. After propagated, the wave touches a hydrophone at receiver side [5]. This modulated signal has undergone an attenuation due to distribution and absorption by water medium and distortion [3]. The hydrophone converts the acoustic wave into electrical signals. This weak signal is amplified by Low Noise Selective Amplifier. Further, the amplitude modulation signal will be distributed to two lines. The first line goes to data processor of receiver and the other goes to clock regenerator. In signal processor, of the receiver, the AM-signal is demodulated to extract data which is sent by the transmitter. The synchronized clock is needed for this process, so the clock regeneration must be done to generate clock receiver in phase with the incoming data rate.

III.   Data Communications Systems

Data communication for this application is AM modulation system. In this case, the carrier wave frequency is made coherent with the data rate in the system. The clock frequency to generate data rate is generated by dividing the carrier wave and the dividing factor is integer. The clocks frequency is shown in equation 1[16]:

$$f_{clock} = \frac{f_c}{N} \text{……………………………..…} (1)$$

Where:

f_{clock} *is* clock frequency
f_c *is* carrier wave frequency
N *is* divider frequency, integer.

In order to yield a maximum spectrum clock frequency, the waveform with duty cycle of 50%, so N should be an even number. Modulation index (m) of the AM signal to supply the underwater acoustic transducer is made 90% instead of 100%. Therefore, when data is equal to zero, 10% residual carrier signal is remained. Figure 2 shows AM signal with m < 100%.
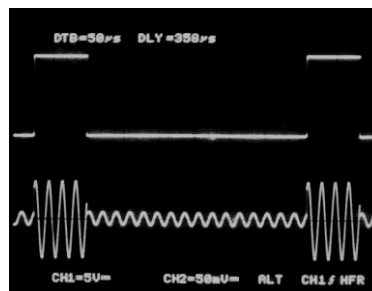

Fig. 2 AM signal with m < 100%

After wave shape processing, the carrier frequency is used as reference signal in the clock regeneration process in the receiver side. The amount of modulation index is calculated using equation 2[6]:

$$m = \frac{V_m}{V_c} \times 100\% \ldots\ldots\ldots\ldots\ldots\ldots\ldots(2)$$

Where:

m *is* modulation index

V_m *is* amplitude of modulated/information signal

V_c *is* carrier signal amplitude

In the receiver side, the acoustic AM signal is received by hydrophone and then amplified by a Selective Low Noise Amplifier, or SLNA, as front end circuit in the receiver. The output of the SLNA is connected to power distribution amplifier, and the signal distributed onto two lines. The first line enters the data processor, and the second line enters the clock regenerator in receiver. Before entering the data processor in receiver, demodulation process of AM signal yields data signal. The signal from AM-demodulation usually weak, distorted and noisy, the signal processor circuit will overcome the problems, and the output of the processor is recovery bit-stream as close as the sent data signal from the transmitter. The bit stream data has serial data format, similar to the one sent by transmitter side. S*erial in–parallel out* (SIPO) shift register converts the serial to parallel data format. This register also produces synchronize bit to be supplied to digital analog converter (DAC). DAC converts data in time slot to the analog signals in channel(s) as sent by the transmitter. All systems in input data processor need clock used as timer and counter. To obtain the right data conversion result, the clock should have the same frequency and locked with transmitter clock frequency. This clock signal is produced by clock regenerator circuit.

The circuit of carrier separator consists of selective signal amplifier circuit with bandwidth about 15Hz. The purpose of this circuit is to obtain the carrier signal within AM 90%. The output signal from selective amplifier is supplied to amplifier circuit with the operating point approaching saturation region. This circuit also called pulse shaper. This amplifier output signal has almost stabile square signal form. Figure 3 shows a block diagram of carrier separator circuit.
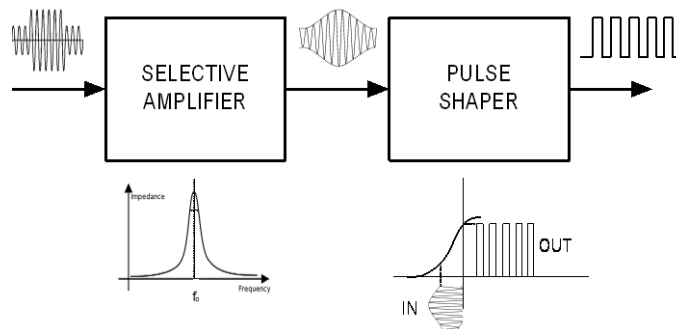

Fig. 3 A block diagram of carrier separator circuit

The pulse shaping circuit consists of logarithmic amplifier and saturation signal amplifier. Log amplifier is used to get amplitude compression, in which weak signal is strengthened more than strong signal. Therefore, by this amplifier the dynamic range, which is the different between weak and strong signals become lower [6]. The amplifier yields an unevenly amplitude signal; therefore a nonlinear amplifier is needed in form of saturation signal amplifier, or an amplitude comparator circuit. For the saturation amplifier, the transistor is made using the principle of switch, where the transistor is situated in cut off or saturation conditions. In cut off condition, the value of $V_{BE} = 0V$, so $I_B = 0V$ and $I_C = 0V$; therefore, no current flows from collector to emitter and ($I_C = 0$) and $V_{CE} = V_{CC}$, this situation is similar to switch in open condition (off). Whereas, saturation condition is obtained by arranging $V_{BE} \neq 0$ or $I_B > I_C/\beta$; therefore, current will flow from collector to emitter and $V_{CE} = 0$. This condition is similar to switch in closed condition (on) [6]. In determining base resistance (R_B) to obtain saturation base current, equation 3[3] is used:

$$R_B = \frac{(V_{in} - V_{BE.SAT})\beta}{I_{B.SAT}} \ldots\ldots\ldots\ldots\ldots\ldots..(3)$$

Where:

R_B *is* front base resistance

V_i *is* input voltage

$V_{BE.SAT}$	*is*	saturation base-*emitter* voltage
β	*is*	transistor amplification factor
$I_{B.SAT}$	*is*	saturation base current

This circuit uses silicon type transistor having saturation base-emitter ($V_{BE\ sat}$) ≈ 0.7 V. Figure 4 is working principle of transistor switch as saturation signal amplifier.
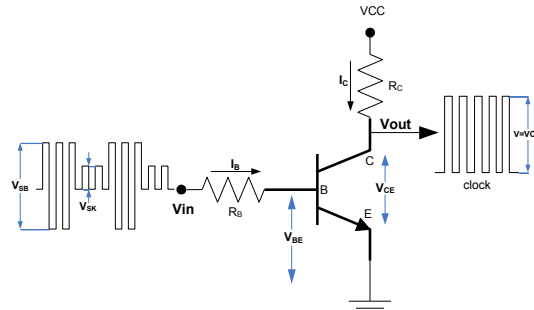

Fig. 4 Transistor as saturation signal amplifier

The transistor input voltage (V_{in}) originates from carrier signal. This signal still consists of signals with high (V_{SB}) and lower (V_{SK}) amplitudes, and the both level are high state of the signal. When V_{SB} or V_{SK} = 0V, then V_{BE} = 0V, this condition makes transistor in cut off condition; thus, the value of V_{output} = V_{CE} = VCC. If V_{SK} ≥$V_{BE\ sat}$, then, transistor is in saturation condition causing V_{output} = 0V. With the above process, clock signal with flat or almost stabile amplitude will be obtained; in which, the level of the signal amplitude can be adjusted by arranging VCC value.

Clock regenerator circuit acquires input signal from clock separator. Clock frequency of receiver should be locked with clock frequency of the transmitter; therefore, the frequency divider against its carrier frequency is N. Figure 5 shows a block diagram of clock regenerator for underwater AM-data communication system.
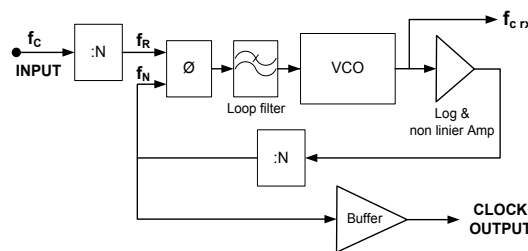

Fig. 5 A block diagram of underwater AM-data communication system

A clean carrier signal with frequency *fc* is formed into square wave. The circuit of frequency divider with denominator = N is used to obtained clearer signal; from here, it will gained reference frequency (f_R). Later, this f_R frequency is connected into phase detector circuits, as a reference signal, to be compared against frequency f_N which is derived from voltage control oscillator (VCO). If frequency of VCO is equal to carrier wave frequency, then divider frequency for phase detector is N. Phase detector compares signal phase of f_R and f_N, in initial condition f_R *is* not equal to f_N because frequency of *VCO* is free running oscillator. Due to frequency and phase difference between f_R and f_N, the circuit of phase detector yields error voltage. Then, the error voltage in form of pulse sequence is passed on to loop filter circuit in form of low pass filter, which always following every change on carrier frequency of transmitter (f_c). Next, this DC voltage is used to control VCO frequency so that VCO circuit is oscillated on the same frequency as fc, which is carrier frequency of receiver (f_{cRX}). In this condition, phase difference f_R and f_{cRX} divided with N or f$_N$ is 90^0, this condition is called locked.

Before comparing with reference frequency (f_R) in phase comparator circuit, the VCO output frequency ($f_{c\ RX}$) divided with denominator N. When the system is in locked condition, then $f_R = f_{c\ RX} / N$ or in other words will meet equation 4[3]:

$f_{c\ RX} = f_R \times N$ ……………………..…..(4)

Where:

$f_{c\ RX}$	*is*	carrier frequency of receiver
f_R	*is*	reference frequency
N	*is*	denominator

Based on the equation, f_{cRX} will be easy to be made as variable by changing the amount of N number, where N is integer and f_R is the lowest unit of f_{cRX} change. This lowest unit often called step. The above process will raised locked phase wave with the same frequency as clock frequency in receiver side. In clock regenerator in Figure 4, VCO is oscillated in carrier wave frequency f_c, while clock frequency is f_{cRX} divided with N factor. The output of divider frequency is branched for phase detector and output clock through buffer circuit. This clock signal is used to supply system in data processor of receiver, such as bit system recovery, SIPO register and timing for DAC.

IV.   Conclusion

In synchronous data communication system, clock signal in receiver side should be locked with clock in transmitter side. The locked status for clock regenerator with low bit as in underwater communication system, data will be hard to achieve if using bit stream as reference. With AM signal 90% using carrier frequency coherent to bit stream as modulated signal, clock regenerator can refer to carrier wave that always exist, so that regeneration will be easier.

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