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DESIGN OF 4 BIT BINARY ARITHMETIC CIRCUIT USING 2'S COMPLEMENT METHOD

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Abstract: *This paper presents a technique to design a 4bit binary arithmetic circuit capable of doing addition and subtraction operation using 2's complement method. As the 2's complement method is more advantageous than 1's complement method, the explored method of the circuit of 2's complement method along with the conventional 4 bit adder-subtractor composite unit achieves the design to get perfect result. By this circuit we can add or subtract any two numbers with any sign in an efficient way without employing the human brain.*
Keywords: *Control inverter, Control sign input, Composite unit, Sign magnitude bit output, Full adders.*

I. Introduction:

The adder-subtractor composite unit has a vast application in binary arithmetic operations in digital technology. The addition of multiple bit numbers can be accomplished using several full adders [3]. Composite unit simplifies the complexity by adding two circuits in a single one. This circuit is capable of adding and/or subtracting two 4bit numbers resulting in a 5bit result with an additional bit representing the sign of the output. The subtraction of two binary numbers may be accomplished by taking the 2's complement of the subtrahend and adding to the minuend [1]. Control sign input in the present study controls the sign of the inputs as per requirement and thus can control the addition and subtraction using 2's complement method in parallel binary full adder circuit. This circuit have inputs i.e. X (X_3, X_2, X_1, X_0) & Y (Y_3, Y_2, Y_1, Y_0) and capable of performing arithmetic operation like X+Y, -X+Y, X-Y, & -X-Y.

II. Theory:

This circuit(Fugure-1) have total ten inputs i.e. X_3,X_2,X_1,X_0 as to represent 1st 4 bit input A; Y_3,Y_2,Y_1,Y_0 as to represent 2nd 4 bit input B, C_A (Control sign input of A) and C_B (Control sign input of Y). Control sign input is 0 when number is positive and 1 when number is negative. We are using parallel 4 bit adder circuit by cascading 4 full adders, xor gates as control inverter and other simple logic gates [5, 6]. Here T (C_A XOR C_B) is 1st parallel adder's complement controller factor. In 1st parallel adder two 4 stage xor gate are used to complement the binary values of X and Y according to the requirement [4]. T is connected with 1st parallel adder's carry input to implement the 2's complement method. C_A* is the complement controller of X and C_B* is the complement controller of Y. Cout1 is the final carry output from the 1st parallel adder. The sum outputs of 1st parallel adder are connected with another 4 stage xor gates as controlled inverter [3]. K is the 2nd parallel adder's complement controller factor. The output of xor gates are connected with the B_3, B_2, B_1, & B_0 of the 2nd parallel adder [2]. In 2nd parallel adder A_3, A_2, A_1 are connected with ground and A_0 is connected with K to implement the 2's complement of the output when required. From 2nd parallel adder we get the outputs S_3, S_2, S_1 & S_0. The 5th output Cout (T XOR C_{out1} XOR K) shows the extra output to represent the high ranges data. The 6th output bit (MSB) SM (C_A C_B + TC_{out1}^) is the sign magnitude bit to represent the sign of the outputs. For SM, C_AC_B=1when $C_A \neq C_B$, TC_{out1}^=1 when T=1 as well as C_{out1}^=1. C_{out1}^=1 when C_{out1}=1 and T=1 when C_A=C_B. Examples are shown below in the tables.

This circuit has three very important indicators named as T, K, & C_{out1}. T controls the C_A* and C_B* to complement the values of X and Y when needed. K controls the 2nd parallel adder to implement the complement of the output when needed and thus controls the total operation.

Figure-1

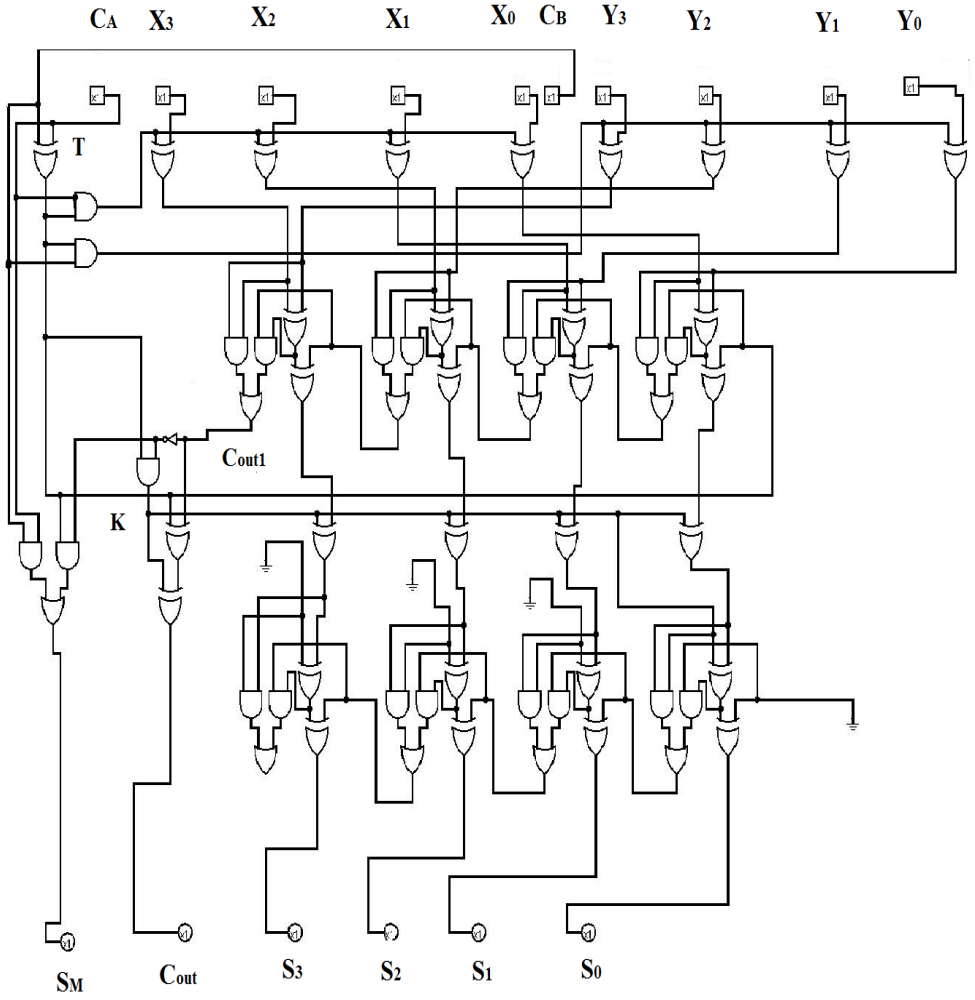

Table-1

C_A	X_3	X_2	X_1	X_0	C_B	Y_3	Y_2	Y_1	Y_0	S_m	C_{out}	S_3	S_2	S_1	S_0
0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0

Table-2

C_A	X_3	X_2	X_1	X_0	C_B	Y_3	Y_2	Y_1	Y_0	S_m	C_{out}	S_3	S_2	S_1	S_0
1	1	0	0	0	1	1	0	0	0	1	1	0	0	0	0

Table-3

C_A	X_3	X_2	X_1	X_0	C_B	Y_3	Y_2	Y_1	Y_0	S_m	C_{out}	S_3	S_2	S_1	S_0
0	0	1	1	1	0	0	1	0	1	0	0	1	1	0	0

Table-4

C_A	X_3	X_2	X_1	X_0	C_B	Y_3	Y_2	Y_1	Y_0	S_m	C_{out}	S_3	S_2	S_1	S_0
1	0	1	1	1	1	0	1	0	1	1	0	1	1	0	0

Table-5

C_A	X3	X2	X1	X0	C_B	Y3	Y2	Y1	Y0	Sm	Cout	S3	S2	S1	S0
1	1	0	0	0	0	0	0	1	1	1	0	0	1	0	1

Table-6

C_A	X3	X2	X1	X0	C_B	Y3	Y2	Y1	Y0	Sm	Cout	S3	S2	S1	S0
0	1	0	0	0	1	0	0	1	1	0	0	0	1	0	1

III. Result and analysis:

By using logisim software I am constructing the circuit diagram used in Fig-1. The simulation results are showing in Table-1, Table-2, Table-3, Table-4, Table-5 and Table-6. The results are explained below.

Table-1 shows the result when X=+8(X3=1,X2=0,X1=0, X0=0),Y=+8(Y3=1,Y2=0,Y1=0,Y0=0), So CA=0(representing X as positive),CB=0(representing Y as positive). At the output port Sm=0(representing output as positive),& Cout=1,S3=0,S2=0,S1=0,S0=0 represent the output as +16.

Table-2 shows the result when X=-8(X3=1,X2=0,X1=0, X0=0),Y=-8(Y3=1,Y2=0,Y1=0,Y0=0), So CA=1(representing X as negative),CB=1(representing Y as negative). At the output port Sm=1(representing output as negative),& Cout=1,S3=0,S2=0,S1=0,S0=0 represent the output as -16.

Table-3 shows the result when X=+7(X3=0,X2=1,X1=1, X0=1),Y=+5(Y3=0,Y2=1,Y1=0,Y0=1), So CA=0(representing X as positive),CB=0(representing Y as positive). At the output port Sm=0(representing output as positive),& Cout=0,S3=1,S2=1,S1=0,S0=0 represent the output as +12.

Table-4 shows the result when X=-7(X3=0,X2=1,X1=1, X0=1),Y=-5(Y3=0,Y2=1,Y1=0,Y0=1), So CA=0(representing X as positive),CB=0(representing Y as positive). At the output port Sm=1(representing output as negative),& Cout=0,S3=1,S2=1,S1=0,S0=0 represent the output as -12.

Table-5 shows the result when X=-8(X3=1,X2=0,X1=0, X0=0),Y=+3(Y3=0,Y2=0,Y1=1,Y0=1), So CA=1(representing X as negative),CB=0(representing Y as positive). At the output port Sm=1(representing output as negative),& Cout=0,S3=0,S2=1,S1=0,S0=1 represent the output as -5.

Table-6 shows the result when X=+8(X3=1,X2=0,X1=0, X0=0),Y=-3(Y3=0,Y2=0,Y1=1,Y0=1), So CA=0(representing X as positive),CB=1(representing Y as negative). At the output port Sm=0(representing output as positive), & Cout=0,S3=0,S2=1,S1=0,S0=1 represent the output as +5.

IV. Conclusion:

The present circuit represents 6 output bit. 6^{th} (MSB) output bit is the sign magnitude bit to represent the sign of the output. 5^{th} output, C_{out}, is the extra output representing as C_{out}=0, when the result lies in between 0 to 15 and as C_{out}= 1 when the result exceed the range. The last four outputs S_3, S_2, S_1 & S_0 are the normal output to represent the data. By this Process desired and accurate result may be obtained depending on the value and sign of the inputs. Moreover, the present endeavour encompasses the use of the simple logic gates and costing to a minimum range enable to use in an economic manner in practical applicable field. By using this circuit we can perform 4 bit operation only, but we can implement the same logic over higher number of bits also. In future I want to design an arithmetic circuit which is capable of using BCD and Excess-3 codes.

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References:

[1] D. Sangwan and M. K. Yadav, "Design and Implementation of Adder/Subtractor and Multiplication Units for Floating-Point Arithmetic", International journal of ElectronicsEngneeing,2(1), 2010,pp.197-203.(8)
[2] D. Ghosh,"Design of 4-Bit Adder Subtractor Composite Unit Using 2's Complement Method"http://www.academia.edu/4020322/DESIGN_OF_4BIT_ADDER_SUBTRACTOR_COMPOSITE_UNIT_USING_2S_COMPLEMENT_METHOD
[3] Goggle search, Digital adder circuit,http://mindcraft.gamepedia.com/Tutorials/Advanced_redstone_circuit
[4] Google search,digital logic circuit design, http://ozark.hendrix.edu/~burch/logisim/
[5] U. Kulisch, "Advanced Arithmetic for the Digital
[6] Wikipedia,adder-subtractor composite unit, http://en.wikipedia.org/wiki/Adder%E2%80%93subtractor

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