

A Hierarchical Standard Cell Placement Method Based On a New Cluster Placement Model

¹Poovendran R, ²Mohan A, ³Vigneshsingh B

^{1,2,3}Department of Electronics and Communication Engineering Adhiyamaan College of Engineering

Abstract: In this paper, we propose a new hierarchical timing-driven standard-cell placement method, in which a new cluster placement model is introduced. The proposed method is divided into three phases, clustering cells, global placement and detailed placement. After clustering cells, in the global placement phase, we determine and improve cluster placement by a simulated annealing based method. In most of previous methods, the shape of any cluster was restricted to a square. In the proposed method, however, we remove this restriction, and propose a new placement model, called the Amoeba model, in which the shape of a cluster can be a collection of connected squares. Since the flexibility of cluster placement is increased by the amoeba model, we can obtain a high quality placement satisfying timing constraints. In the detailed placement phase, we assign cells to cell rows under the non-overlapping constraint of cells with a constructive approach. Experimental results show the effectiveness of the proposed method with the new cluster placement model.

I. Introduction

With the rapid progress of semiconductor technology, standard-cell placement has become a quite difficult task, since it must handle circuits containing more than 10^6 cells under strict timing constraints. A well-known approach to this difficult problem is to introduce clustering of cells so that the problem size is effectively reduced. In particular, when a simulated annealing based placement algorithm is used, clustering is indispensable to get a good placement in a practical computation time. There have been many clustering methods proposed so far

Any placement method combining clustering and simulated annealing typically consists of three phases, i.e., clustering cells, global placement, and detailed placement. Global placement is to determine a placement of clusters, and detailed placement is to get a final standard cell placement. In the global placement phase, the shape of any cluster is generally assumed as a square, or sometimes, a circle. However, it may not be appropriate to restrict the shape of a cluster to a square or a circle, since, in the final cell placement, cells in a cluster would not form a square or a circle. Thus, in global placement can be flexibly changed, a better final placement would be obtained. This is our basic idea of the proposed method.

In this paper, we propose a clustering based standard cell placement method, which consists of three phases mentioned above. In the first clustering phase, we perform a connectivity-based clustering algorithm to form clusters of cells for the given netlist. In the global placement phase, we determine and improve cluster placement by simulated annealing. We propose a new cluster placement model, called the Amoeba model. In the amoeba model, the shape of any cluster can be flexibly changed under some constraints.

Since the flexibility of cluster placement is increased, it is expected that a high quality placement satisfying timing constraints is easily obtained. Finally, in the detailed placement phase, we assign cells to cell rows under the nonoverlapping constraint of cells with a constructive approach considering the minimization of estimated total wire length of all nets to get a final legal cell placement. Experimental results show that the proposed placement method produced better placements, compared with the placement method, in which the shape of any cluster is restricted to a square. The remainder of this paper is organized as follows. In Section 2, we explain the interconnect delay model, and formulate the timing-driven standard-cell placement problem. In Section 3, we propose a timing-driven standard-cell placement method based on a new cluster placement model. Finally, in Section 5, we address some conclusions and discuss future researches.

II. Preliminaries

2.1. Layout Model

The layout model we assume in this paper is the row based standard cell model. A standard cell layout consists of rectangular modules with the same height called cells. The functionality and the electrical characteristics of each predefined cell are tested, analyzed, and specified in advance. Cells are placed in rows called cell rows, and none of them should overlap each other. I/O pads are placed around the chip area. The space between two cell rows is called a channel, which is used to realize interconnection between cells.

2.2. Delay Model

In the proposed algorithm, timing constraints are taken into account, and thus an appropriate wire delay model is required. In this paper, the Elmore delay model is adopted as the interconnect delay model.

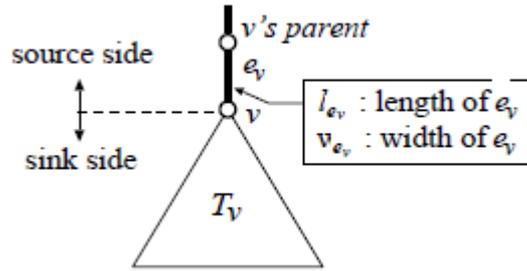


Figure 1: Elmore delay of wire e_v .

For wire e , let l_e , w_e , c_e and r_e denote its length, width, capacitance, and resistance, respectively. Further, let e_v denote the wire entering node v from its parent, as shown in Figure 1. We use the following model for interconnect delay of e_v , denoted $D_{wire}(e_v)$.

$$c_e = (c_a \cdot w_e + c_f) \cdot l_e$$

$$r_e = r_0 \cdot l_e / w_e$$

$$D_{wire}(e_v) = r_{ev} \cdot (c_{ev} / 2 + c(T_v))$$

where c_a , c_f , and r_0 are area capacitance, fringing capacitance, and resistance for unit-width, unit-length wire, respectively. T_v is the subtree rooted at v , and $c(T_v)$ is the capacitance of directed connected subtree in T_v from T_v 's root v . The total Elmore delay DE_{lmore} from source s_0 to sink t_i is given as follows.

$$DE_{lmore}(s_0, t_i) = \sum_{e_v \in \text{path}(s_0, t_i)} D_{wire}(e_v)$$

2.3. Problem Formulation

Let $L = (M, N)$ be a logic circuit, where $M = \{m_1, m_2, \dots, m_M\}$ is a set of cells and $N = \{n_1, n_2, \dots, n_N\}$ is a set of nets. Any net n_i can be represented as a subset of M . Assume that a net n_j is a set of cells, $n_j = \{m_{nj0}, m_{nj1}, \dots, m_{nj_k}\} \subset M$, $k = |n_j| - 1$, where m_{nj0} is the source cell and others are sink cells. For each net n_j , the required arrival time T_{req_j} is given. Let d_j denote the largest delay time from the source to a sink of a net n_j . Then, the timing constraint violation V_j of a net n_j is defined as follows.

$$V_j = \begin{cases} 0 & (d_j \leq T_{req_j}) \\ d_j - T_{req_j} & (d_j > T_{req_j}) \end{cases}$$

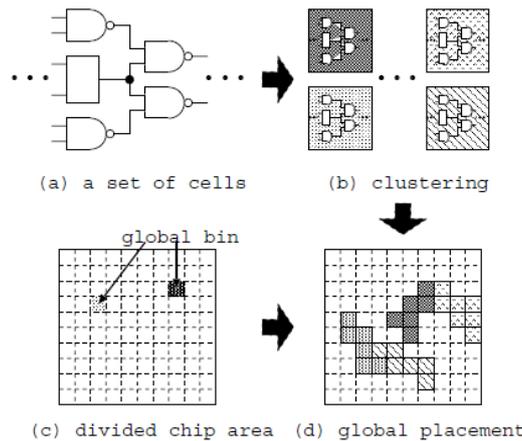


Figure 2: Global placement in the proposed method.

This equation means that, for each net n_j , if the largest sink delay d_j is smaller than the required arrival time T_{req_j} , the timing constraint is satisfied, otherwise the timing constraint is violated. The placement problem discussed in this paper is to find a standard cell placement minimizing the total wire length of all nets under the condition that all timing constraints are satisfied.

III. The Proposed Algorithm

3.1. Overview

The proposed method is divided into three phases, i.e., clustering of cells, global placement and detailed placement. After clustering cells, in the global placement phase, cluster placement is determined and improved with a simulated annealing based algorithm. Then, in the detailed placement phase, cells are assigned to cell rows under the nonoverlapping constraint of cells. In the following, we give the overview of each phase.

First, clustering of cells is performed to reduce the size of the problem so as to shorten the computation time of the simulated annealing based global placement method in the global placement phase (Fig.2(b)). In most of previous clustering-based placement methods, in the global placement phase, the shape of each cluster is assumed to be a square, and each cluster is placed in the chip area, allowing the overlaps among clusters. However, it may be difficult to obtain a high quality cell placement, since cells in a cluster will not necessarily form a square in the final cell placement. Making the size of a cluster small

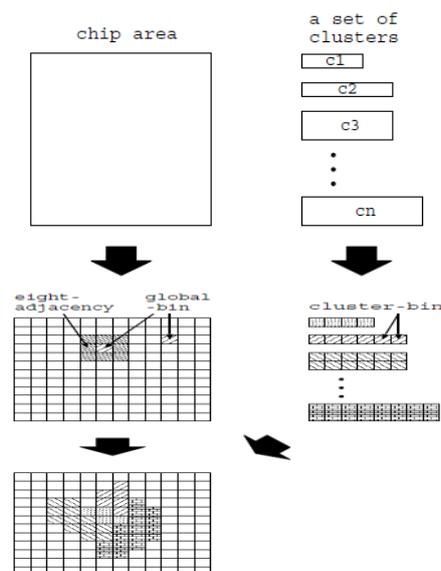


Figure 3: Global placement based on the amoeba model.

would lead to a better placement, but it would also incur the large increase of computation time if the placement method was based on simulated annealing. To resolve this difficulty, we propose a new cluster placement method. In the global placement phase of the proposed method, the chip area is divided into a number of global bins (Fig. 2(c)). Then, all clusters are placed on global bins by a simulated annealing(SA) based method (Fig. 2(d)), allowing the overlaps among clusters. The area of each cluster is k times as large as the area of a global bin, where k is an integer with $5 \leq k < 20$. When determining the cluster placement in the chip area, the shape of any cluster is not restricted to a square, but can be a collection of connected global bins (Fig. 2(d)). We call this cluster placement model the Amoeba model.

In the detailed placement, each cluster is decomposed contained in global bins on which the cluster including them are placed. Finally, the cell assignment is performed with a constructive method minimizing the half perimeter length of all nets to obtain a final legal cell placement.

3.2. Phase 1: Clustering

A clustering of a standard-cell netlist groups cells into disjoint clusters. The objective of clustering in the proposed method is to reduce the problem size so as to improve the performance of the global placement phase, which is based on simulated annealing. Let K be a number of clusters after clustering cells. In the current implementation, we set K to 100 ~ 500, and a simple connectivity-based, greedy clustering algorithm is used to form clusters. In this algorithm, first, K cells are randomly selected as initial clusters.

Then, a pair of a cell and a cluster, denoted c_i and C_j respectively, is selected so that c_i is not an element of any current cluster, and the fractions of nets absorbed by the clusters is maximum if c_i is merged with C_j . We repeat this procedure to form clusters. We also introduce the upper and lower bounds of the cluster size, and the clustering result must satisfy those bounds. For the lack of space, we omit the details of cell clustering. For details, refer to [6].

3.3. The Amoeba Model

We introduce some terminologies to define the amoeba model. The chip area is a rectangle, on which all cells are placed. The global bin is a grid, which is obtained by dividing the chip area equally in x- and y-directions. We divide the chip area into a set of global bins so that the number of global bins is about k times as many as the number of clusters, where k is a positive integer less than 20 (in the current implementation, we set k=10). Let C be a set of all clusters, $C = \{c_1, c_2, \dots, c_C\}$, and let B be a set of all global bins, $B = \{b_1, b_2, \dots, b_B\}$. Each cluster is placed on more than one global bins (Figure 3). Therefore, let A_i be the size of a cluster c_i and let A_{bin} be the size of a global bin, then a cluster c_i is placed on N_i global bins, where $N_i = \lfloor A_i / A_{bin} \rfloor$. We call N_i global bins composing a cluster c_i the cluster bins of c_i . And for a set of global bins, B, two global bins $b_s \in B$ and $b_t \in B$ is said to be 8-adjacent, if they share a common vertex. Moreover, if the reflexive transitive closure of the 8-adjacent relation on B is equal to the universal relation of B, we say that B is 8-connected. We formally define the amoeba cluster placement model as follows.

Amoeba Model For any cluster $c \in C$, c is placed on a set of 8-connected global bins in the chip area.

3.4. Phase 2: Global Placement

As described in Section 3.1, in the global placement phase of the proposed method, the set of all clusters in C is placed in the chip area with the simulated annealing based placement method with the amoeba model. Outline of the global placement phase is shown in Figure 4. Initial placement of clusters is generated randomly under the condition that the shape of any cluster is a square and overlaps among clusters are permitted. We define the shape of a cluster as a rectilinear polygon by eliminating bins from the top-right corner of a square if the cluster can't be placed in a square shape. We give some notations to explain the detail of the proposed algorithm in the following. When a cluster $c_i \in C$ was placed with the amoeba model, a set of global bins on which cluster bins of c_i have been placed is represented as $P(c_i) \subset B$. Moreover, a set of clusters placed on global bin b_j is represented as $Q(b_j)$, that is, $Q(b_j) = \{c_i \mid b_j \in P(c_i), c_i \in C\}$. In the following, we explain the detail of the proposed algorithm.

3.4.1. Moving clusters

In this section, we describe how to change the cluster placement in the proposed method when the cluster placement is improved with simulated annealing. There are two cases. One is to move one cluster, and the other is to interchange locations of two clusters. But, the latter can be realized as an extension of the former. Therefore, we mainly explain how to move a cluster using an example shown in Figure 5.

3.4.2. Determining the shape of a cluster

We explain how to determine the shape of a cluster when moving it. As described in Section 3.4.1, for the cluster c_i to be moved, first, one global bin is randomly selected as the destination of move of one cluster bin of c_i , and then, remaining cluster bins are moved one by one so that the shape of cluster c_i is determined. The following is the procedure to determine the shape of a cluster.

Step 1 Let $P(c_i) = \{bs\}$.

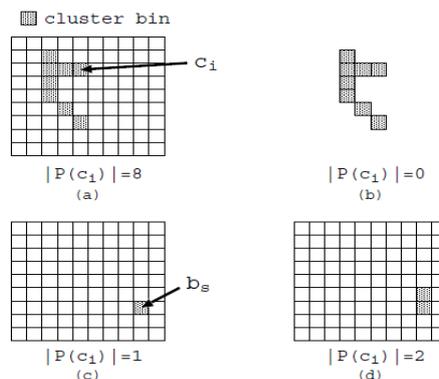
Step 2 Let $B_8(c_i) \in B$ be a set of global bins which are 8-adjacent with $P(c_i)$.

Step 3 Evaluate the cost of each $b \in B_8(c_i)$.

Step 4 Add $b_{min} \in B_8(c_i)$ with the minimum cost to $P(c_i)$, that is, $P(c_i) = P(c_i) \cup \{b_{min}\}$.

Step 5 Repeat Step 2 \in Step 4 until $|P(c_i)| = N_i$.

The objective of determining the shape of c_i is to minimize the total delay considering the number of overlaps among clusters. Therefore, we should use the sum of delay.



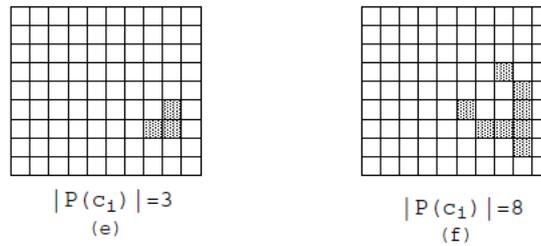


Figure 5: An example of moving a cluster.

Of all interconnections connecting to b as the cost in Step 3. However, we can hardly estimate the accurate delay to evaluate the shape of a cluster, because precisely estimating the delay of interconnections might require an unacceptable large time in this phase. So, we use the quadratic sum of total estimated wire length since the delay of a wire is quadratically proportional to the wire length. We define the estimated wire length of a net as follows. A set of nets connecting to $c_i \in C$ is represented by $\text{Net}(c_i)$. Note that a net $n \in \text{Net}(c_i)$ is a set of clusters. Moreover, the distance between $c_i \in C$ and $c_j \in C$, denoted $l(c_i, c_j)$, is defined as follows.

$$l(c_i, c_j) = \min\{l_M(b, b') \mid b \in P(c_i), b' \in P(c_j)\}$$

where $l_M(b, b')$ is the Manhattan distance between the centers of b and b' . And then, the estimated wire length of $n \in \text{Net}(c)$, denoted $L(c, n)$, is defined as follows.

$$L(c, n) = \min\{l(c, c') \mid c' \in n, c' \neq c\}$$

3.4.3. Cost function

A current solution in simulated annealing (SA) is perturbed by the methods presented in Sections 3.4.1 and 3.4.2. Then, a neighborhood solution is generated. We define the cost function to evaluate a neighborhood solution as follows.

$$f_{\text{cost}} = L_{\text{wire}} + \beta N_{\text{overlap}} + \gamma T_{\text{vio}}$$

3.4.4. Routing Estimation

To evaluate interconnections among clusters by Equation (6), we need to assign the pins of a net on each cluster

and generate routing patterns of interconnections. We determine them by an extension of the SERT algorithm [3]. In the proposed method, we assign the pin positions for each cluster and determine global routes among clusters, simultaneously. First, we must assign the pin position of the source to the source cluster. We assign the pin position of the source to the cluster bin which is the nearest to the center of a net. The center of a net is determined by calculating the arithmetic mean of locations of all clusters connecting to the net. Next, instead of seeking terminals in each step of adding a new edge, we seek cluster bins which haven't been added to a Steiner tree. And then, the pin of the cluster connecting to a net is assigned to a cluster bin included in the cluster. For the lack of space, the details are omitted. For details, refer to [6].

3.5. Phase 3: Detailed Placement

In the detailed placement, a final standard cell placement is determined from the global placement of clusters.

The cell placement is done with the step-by-step refinement procedure as follows. This procedure consists of three steps. In the first step, cluster bins in each cluster are assigned to global bins in the chip area without any overlaps among clusters, considering the minimization of total wire length.

For each cluster, the corresponding global bins in the chip area thus determined in this step are called target global bins. In the second step, each cluster is decomposed into a set of original cells, and each cell is assigned to one of target global bins, which were determined in the first step, considering the minimization of total wire length. Finally, in the third step, each cell in the global bins are assigned to cell rows, also considering the minimization of total wire length. For the lack of space, the details are omitted. For details, refer to [6].

IV. Conclusion

In this paper, we have proposed a clustering based, timingdriven standard-cell placement method with a new cluster placement model, called the amoeba model. In the proposed method, the shape of any cluster, which was used to be a square in the previous method, can be flexibly changed. Since the flexibility of cluster placement is increased, we can obtain a high quality placement satisfying timing constraints. Experimental

results were quite promising. There are several future works. First, in the clustering phase, some timing influenced clustering method like is sought, since in the current implementation, no timing constraints are considered in cell clustering. Second, in the global placement phase, some effective mechanism to remove overlaps among clusters is required, since, in the current implementation, a considerable amount of overlaps exists in general. Also, an efficient algorithm to determine global routes among clusters is needed to reduce the computation time. Finally, in the detailed placement, a timingdriven cell assignment method to cell rows is sought.

References

- [1] C.J.Alpert and A.B.Kahng, "A general framework for vertex orderings, with applications to netlist clustering", Proc.ICCAD'94, pp.63–67, 1994.
- [2] C.J.Alpert, "The ISPD98 circuit benchmark suite,"Proc. International Symposium on Physical Design,pp.18-25, 1998.
- [3] K.D.Boese, A.B.Kahng and G.Robins, "High-performance routing trees with identified critical sinks,"Proc. 30th ACM/IEEE Design Automation Conference, pp.182-187, 1993.
- [4] J.Cong and D.Xu, "Exploiting signal flow and logic dependency in standard cell placement", Proc.ASPDAC' 95, pp.399–404, 1995.
- [5] W. C. Elmore, "The transient response of damped linearnetworks with particular regard to wideband amplifiers," J. Applied Physics, 19, pp.55–63, 1948.
- [6] N.Iwauchi, "A timing-driven standard-cell placement method based on a new clustering placement model," Master thesis, Graduate School of Engineering, Hiroshima University, 2002.
- [7] W.-J Sun and C.Sechen, "Efficient and effective placement for very large circuits," Proc.ICCAD'93, pp.170– 177, 1993.
- [8] H.Vaishnav and M.Pedram, "Delay-optimal clustering targeting low-power VLSI circuits", IEEE Trans.CAD,18, 6, pp.799–812, 1999.