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Design and Analysis of Carry Look Ahead Adder Using CMOS Technique

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Abstract:*Addition is a fundamental operation for any digital system, digital signal processing or control system. In this paper we have designed a carry look adder circuit using CMOS technique. The propagation delay is one of most important problem in the adder circuits. So the delay problem of Ripple carry adder is analyzed by CLA adder. The adder circuits are designed using Tanner EDA tool and simulation is done by T-Spice 180nm technology. The ripple carry adder and Carry look ahead adder is compared in terms of power and delay. By the analysis of adder circuits using tanner tool found that the delay of proposed carry look ahead adder is reduced 34%.Hence it gives better performance that ripple carry adder.*

Keywords:*Carry Look Ahead Adder, CMOS technique, Ripple Carry Adder, Propagation Delay, Power dissipation*

I. Introduction

ALU is the fundamental building block in central processing unit. ALU needs adder circuit for addition and multiplication. In the past major challenges for VLSI designer to reduce the area of chip . Now three major performance parameters i.e. Power, area and speed are focused by VLSI designer.A carry look ahead adder is a type of adder used in digital logic. It improves speed by reducing the amount of time required to determine carry bits. It can be contrasted with the simpler, but usually slower, ripple carry adder for which the carry bit is calculated alongside the sum bit, and each bit must wait until the previous carry has been calculated to begin calculating its own result and carry bits. In this paper Carry look ahead adder is designed and analyzed using standard CMOS technique.Tanner simulation has been done for 180 nm technology to determine power dissipation and delay. Carry look ahead adder is compared with ripple carry adder.

II. Design Of Carry Look Ahead Adder and Ripple Carry Adder

Carry look ahead adder:

The basic block diagram of carry look ahead adder is discussed in this. The carry look ahead adder using the concept of propagating and generating the carry bit. It calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits.

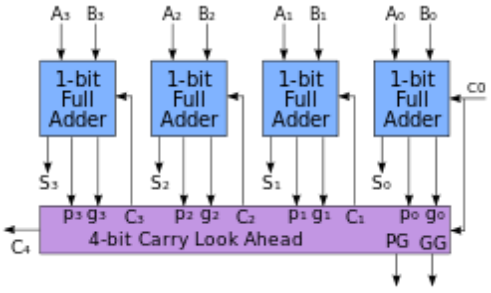

Fig 1: Block diagram of 4 bit carry look ahead adder

The expression for Carry propagate,Pi = Ai xor Bi
Carry generate, Gi = Ai . Bi
Sum expression, Si = Pi xor Ci
Carry out, Ci+1 = Gi + Pi Ci

Ripple carry adder :

A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs.

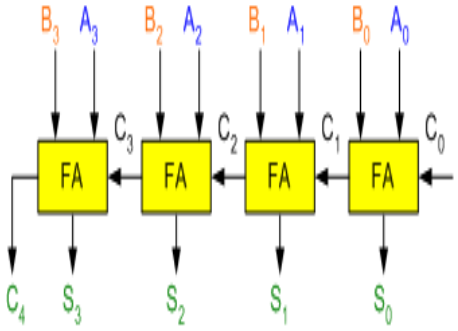

Fig 2 Block diagram of ripple carry adder

III. Technique Used

The most widely used logic style is standard CMOS. Complementary metal oxide semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS circuitry dissipates less power than other logic families with resistive loads. Since this advantage has increased and grown more important.

IV. Performance Parameters Of Design

a) Power dissipation:

Power dissipation is a measure of the power consumed by the logic gate when fully driven by all its input. The D.C or average power dissipation is the product of D.C supply voltage and the mean current taken from the supply.We can compute the whole power dissipation through the following equation-

P total = P static + P dynamic + P short cir

P = α CL Vdd2 fclk(Isc + I leakage)Vdd

b) Propagation delay:

The propagation delay can be defined as time required to reach 0.5 V_{dd} of output from the 0.5 V_{dd} of input.The propagation delays of Carry look ahead adders are measured in orders of nanometers.This is the important factor in CLA design. The propagation delay of carry bit is calculated. The speed of adder is depending upon propagation delay how fast circuit is work.

V. Simulation And Results Of CLA And RCA

All the simulated circuits of carry look ahead adder and ripple carry adder are given. The comparisons of 2 bit carry look ahead adder and ripple carry adder are done by channel length 180nm technology. Power dissipation, Propagation delay are calculated and compared**.**

Carry look ahead adder:

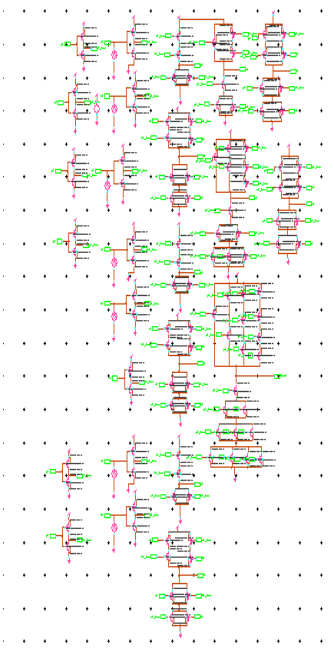

Fig 3 Schematic of carry look ahead adder

WAVEFORM:

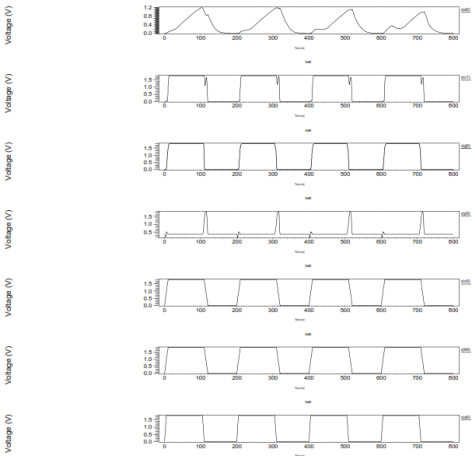

Fig 4 Waveform of carry look ahead adder

Ripple carry adder:

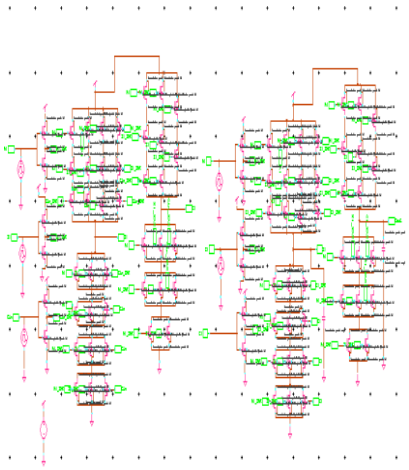

Fig 5 Schematic of ripple carry adder

WAVEFORM:

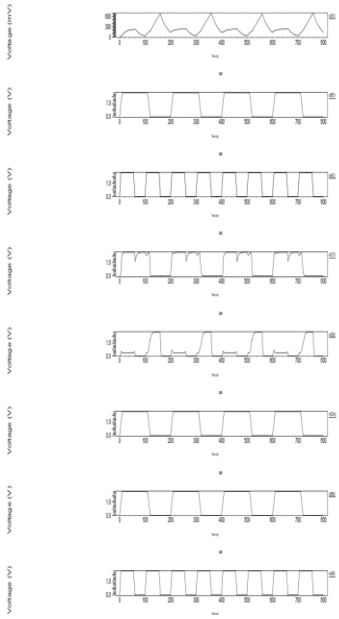

Fig 6 Output waveform of ripple carry adder

Simulation results of carry look ahead adder and ripple carry adder using 180nm technology

DESIGN	AVERAGE POWER(watt)	DELAY(sec)
CARRY LOOK AHEAD	1.369*10^-3	3.187*10^-8
RIPPLE CARRY ADDER	4.871*10^-4	4.857*10^-8

Table1

VI. Conclusion

The proposed carry look ahead Adder is designed using CMOS technique and it performed with 34% less propagation delay as compared to ripple carry adder. The no of transistor count increases but gives less delay and high speed. The carry look ahead adder is used as propagation adder in various multipliers and gives less delay. For future work these high speed adders are used in multiplier circuits.

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