IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676, p-ISSN: 2320-3331, Volume 17, Issue 3 Ser. I (May. – June. 2022), PP 10-19
www.iosrjournals.org

Hybrid Two Quasi Z Source Boost Dc-Dc Converter

JOSE FILIPE ZINGA TOMAS*, YU TANG (Senior Member, IEEE)

Corresponding Author: Dept. of Electrical and Electronic Engineering, Hebei University of Technology, China.(alveszinga@gmail.com)
Dept. of Electrical and Electronic Engineering, Hebei University of Technology, China (2018040@hebut.edu.cn)
** Corresponding author.*

Abstract
The article is about a new family Z-source boost DC-DC converter for the PV solar application, for boosting high voltage gain, which is required to amplify a weak source voltage to a predetermined grid voltage. The proposed converter incorporates a conventional Z-source network to enhance the boost capability of the conventional Z-source network. The hybrid dual quasi-Z-source boost DC-DC converter is a revised version of the proposed Z source network converter which is combined with the traditional, and advantages of Z-source networks with greater boost capability for AC and DC power conversion. All the graphics results of the converter are represented and the converter presents better performance and comparison with other converters, the proposed converter was simulated by PSIM Software.

Keywords: *DC-DC converters, photovoltaic (PV), Z source inverters.*

Date of Submission: 20-05-2022 Date of Acceptance: 03-06-2022

I. Introduction

In the global shortage of fossil fuels, renewable energy power systems, based mostly on photovoltaic (PV) power systems, have exploded in popularity in recent years. The output voltages of PV panels, in a PV power system, are typically low and vary greatly due to weather and environmental effects, thus a step-up stage is frequently required. Especially well-suited for PV power systems, which frequently require a dc-dc converter with strong step-up capability. The suggested hybrid Z-source networks, like the standard Z-source network, may be used for dc–ac, ac–ac, and ac–dc power conversions [1] – [2]. The two-stage systems are shown in Fig. 1 which are made up of inverters and step-up dc-dc converters. The uncontrolled PV panels' low dc voltage, which cannot be supplied by inverters, must be increased and controlled using a high-gain inverter converter. The output of the step-up converters was then controlled to a high level, grid-connected inverters with dc voltage. As a result, the design of step-up dc-dc converters is critical in PV power systems. Various voltage-boost methods, such as the voltage multiplier. [3] – [4]. However, by doing so, the component's leakage inductance increases, resulting in large switching losses and voltage spikes, jeopardizing the converter's efficiency. [5], switched capacitor [6], linked inductor [7]. Currently, research on Z-source networks is mostly focused on dc–ac power conversion, with applications in other fields being considered. There is still a gap in the use of Z-source networks in dc-dc power conversion must be filled as a result; the Z-source networks are used in this article. To enhance e capabilities of dc-dc converters, and presents a type of Z-source boost dc-dc converter with a hybrid Z-source by merging the standard Z-source and the quasi-Z-source networks in many ways [8]. Voltage lift, and cascaded boost, have been extensively investigated thus far. These approaches, on the other hand, are all complicated, with low efficiency and large prices [9].

Peng was the first to suggest the notion of a Z-source network. [10]. As a consequence, the Z-source quasi-Z-source network integrations improve the boost abilities of the produced hybrid Z-source networks while retaining all of the conventional Z-source quasi-Z-source network benefits. The suggested converters are attractive because of the aforementioned benefits [11]. The Z-source network is an X-shaped impedance network that may be used in dc–ac, dc-dc, in dc-dc applications [12]. Z-source inverter (ZSI) can use the shoot-through condition, which is not allowed in standard voltage-source inverters [13]. The remedy to this problem, in addition to improving voltage gain, is to increase the number of switches, as proposed in [14].

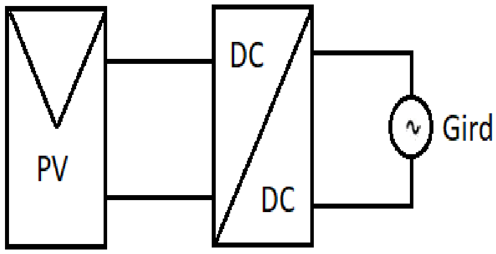

Figure 1: The proposed converter is applied for a PV solar system

Has quickly become a research hotspot. Despite its benefits, the original ZSI has some flaws [15]. The Z-source Inverter solves the problems associated with traditional Voltage Source and Current Source Inverters, such as restricted output voltage and dependability [16-17]. Including a discontinuous input current, high-voltage stresses, and a boost factor of 1/(1-2DS) that is restricted (DS is the shoot-through duty cycle). In addition, with the dc voltage source, there is no common ground between the inverter bridge [18]. Various new impedance-source network topologies have been developed in multiple research to address the constraints of the original ZSI. The quasi-Z-source network is a basic yet effective solution among the modified Z-source network topologies [19]. There are two types of Quasi Z-source inverters (QZSI): continuous current QZSI and discontinuous current QZSI Their impedance networks are referred to as such for ease of reference [20-21]. Quasi-Z-source network I and Quasi-Z-source network II are two types of Quasi-Z-source networks. The two suggested quasi-Z-source networks have the same boost factors as the standard Z-source network, which are 1/(1-2DS). They do, however, have some benefits over standard Z-sources [22]. Constant input current, common ground between the voltage source and the inverter bridge, and decreased network complexity voltage stress on the capacitor [23].

II. Principle of Operation

The following assumptions were made to characterize the operating principle: The converter is in a steady state; the capacitors are large enough that their voltage may be deemed constant during a single switching period; the gray components are turned Off. The operation of the suggested converter was separated into two stages in continuous-conduction mode (CCM) and three stages in discontinuous-conduction mode (DCM) during one switching period, as shown in Figure 2 and Figure 3. The suggested converter is based on Z-source operation principles or is similar to the new Z-source dc-dc converter.
Displays the hybrid Z-source networks' main waveforms. The All of the suggested converters' operation states may be split into state 0 and state 1 is the two states.
1) State 0: The suggested converter's equivalent circuit works in state 0 as depicted in Figure 2. The switch S is on in this condition, while the diodes D1-D3 are off. T0 = DT denotes the interval of state 0 in a switch cycle T, where D is the duty cycle. The energy is discharged to the inductor L1 by the voltage source Vin and capacitor C2. Capacitors C1, C3, and C4 charge inductors L2 and L3 as well as C4.
2) State 1: The suggested converter's equivalent circuit Figure 1 shows how it works in state 1 (b) figure 3. During this time, Switch S is turned off, but diodes D1-D3 are turned on. Assume T1 = (1 - D)T is the interval between states one and two, and T is a switching cycle. Capacitors C1–C4 store energy, whereas capacitors C1–C4 store information. The voltage source Vin, as well as the inductors L1–L3, discharge the capacitors, and energy to the load R.

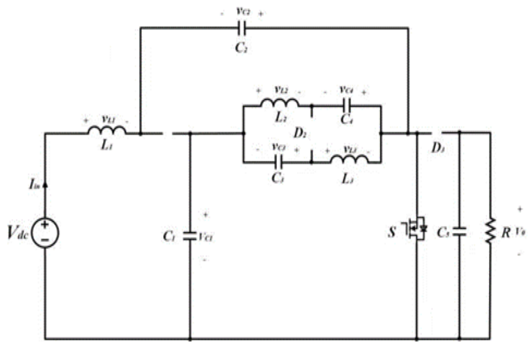

Figure 2: The proposed converter equivalent circuit at state 0

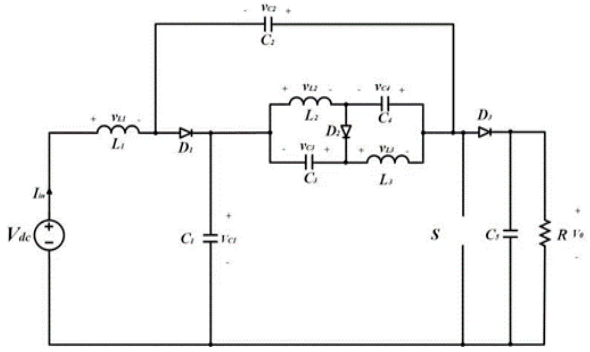

Figure 3: The proposed converter equivalent circuit state one

This section examines the working principles of the suggested converters. The following conditions are assumed for analytical reasons:
1)There are no flaws in any of the components.
2) Because all capacitors are so big, the capacitor voltages can be rather high and be regarded as though it were continuous.
3) All of the converters proposed work in CCM.

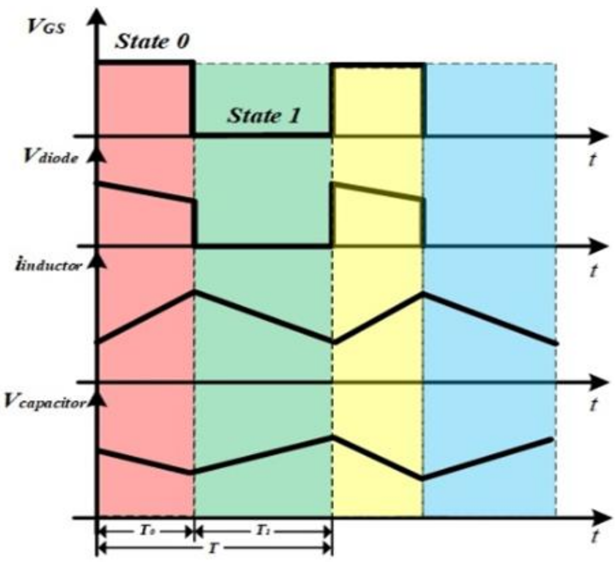

Figure 4 Key waveforms of the proposed converter

Kirchhoff's Voltage Law (KVL) states that voltages are proportional to the square of L1-L3 across inductors can be represented as:

$$V_{L1} = V_{in} + V_{C2}, V_{L2} = V_{C1} + V_{C4}, V_{L3} = V_{C1} + V_{C3}$$
(1)

Due to the symmetry of the quasi-Z-source network II (L2 = L3, C3 = C4) and we can obtain:

$$V_{L2} = V_{L3}, V_{C3} = V_{C4}$$
(2)

2) State 1: The suggested converter's equivalent circuit works in state 1 as depicted in Fig. 6. (b). Switch S is 0ff in this state, while diodes D1-D3 are On. Assume T1 = (1-D) T is the interval between states 1 in a switch cycle T. The voltage source Vin and inductors L1–L3 store energy, while capacitors C1–C4 discharge it to the load R, from State 1, we can obtain:

$$VL_1 = V_{in} - V_{c1}, VL_2 + VL_3 = -V_{C2}$$

$$V_{C3} + V_{C4} = V_{C2}, V_0 = V_{C1} = V_{C2}$$
(3)

The inductors L1 and L2 (or L3) from (1)-(3) can be balanced using the voltage–second balancing method.

$$V_{C1} = \frac{1-2D}{1-3D} V_{in}, V_{C2} = \frac{2D}{1-3D} V_{in}$$

$$V_{C3} = V_{C4} = \frac{D}{1-3D} V_{in}, V_0 = \frac{1}{1-3D} V_{in}$$

(4)

As a result, the suggested converter's voltage gain M can be formulated as:

$$M = \frac{V_0}{V_{in}} = \frac{1}{1-3D}$$

(5)

We know from voltage gain (5) that the suggested has the capacity to move up the hybrid Z-source network has a larger capacity than the standard Z-source network the switched-inductor network and the Z-source/quasi-Z-source network.

Network with a quasi-Z-source the suggested hybrid Z-source network has a higher step-up capability than the standard Z-source/quasi-Z-source network and the switched-inductor quasi-Z-source network. The two-quasi-Z-source boost dc-dc converter uses a hybrid two-quasi-Z-source boost dc-dc converter.

For the hybrid two-quasi-Z-source boost dc-dc converter, the output voltage, Vo, may be written as:

$$V_0 = \frac{1}{1-3D} V_{in} - \frac{1-D-2D^2-2D^3}{1-5D+6D^2} I_{in} r_L$$

$$-\frac{3-9D^2}{1-5D+6D^2} I_{in} r_S - \frac{2-9D+11D^2-4D^3}{1-5D+6D^2} V_D \quad (6)$$

2.1 CCM Voltage Gain Derivation

To determine the proposed converter's static gain, first of all, the inductors are balanced using the volts-second method, as indicated:

$$\int_{t_0}^{t_2} v_{L_1} dt + \int_{t_0}^{t_2} v_{L_2} dt = 0$$

(7)

In stages one and two, knowledge of the voltage across the inductors from stage one and stage two, adequate simplifications are the fowling equation, that can use the capacitor voltage (VC1 and VC2) of the voltage multiplier cell:

$$v_{C1} = v_{C2} = \frac{1+D}{1-D} V_i$$

(8)

As regards the switched capacitor cell, VC3 and VC4 can be obtained through the analysis of the Kirchhoff law in Stage one:

$$v_{C3} = v_{C4} = \frac{3+D}{1-D} V_i$$

(9)

Finally, by assessing Stage II, the static gain (M) may be determined, where Vo=VC3+VC4-VC2. As a result, M is equal to:

$$M = \frac{V_0}{V_I} = \frac{1}{1-3D}$$

(10)

The suggested converter's non-ideal voltage gain is dependent on parasitic factors. In CCM, the non-ideal gain (M’) may be calculated. The component resistances are taken into account in this evaluation as follows: windings of inductors (rL1 = rL2 = rL); capacitors (rC1 = rC2 = rC3 = rC4 = rCo = rC); switches (rDS(on)1 = rDS(on)2 = rDS); diodes (rD1 = rD2 = rD3 = rD4 = rDo = rD) in addition to their forward voltages (vf1 = vf2 = vf3 = vf4 = vf5 = uf) When parasitic components are taken into account, (5) may be rewritten as:

$$D = [V_i - \frac{Ii}{2}(r_L + r_{DS})$$

$$+D'[V_i - V_{C1} - Uf - I_i(2r_L + \frac{r_C + r_D}{2})]$$
(11)
where D' = 1 – D
The input current may be calculated as follows:

$$I_i \approx \frac{5+D}{1-D} I_0 \approx \frac{5+D}{1-D}\frac{V_0}{R_0}$$
(12)
In the first and second stages, the KVL rule states that VC3 and Vo are given by:

$$V_{C3} = 2V_{C1} + V_i - uf - 3kr_C I_i$$
(13)

$$V_0 = 2V_{C3} - V_{C1} - 2uf - 4r_C I_0$$
(14)
The constant proportion of the input current that passes through the SC cell is k. Knowing that VC1 = VC2, VC3 = VC4 after performing the appropriate simplifications, the suggested converter's non-ideal voltage gains (M') is given by:

$$M' = \frac{V_0}{V_i} = \frac{\frac{5-D}{1-D}V_i - 7uf}{V_i(1+\rho(\omega + l))}$$
Where ρ is:

$$= -3\frac{5+D}{R_0(1-D)^2}, \omega = 2r_L - \frac{3D}{2}r_L + \frac{D}{2}r_{DS} + \frac{1-D}{2}r_{D},$$

$$l = (3k\frac{5+D}{1-D} + \frac{8-D}{2})r_C$$
(15)

The suggested converter's voltage gain was verified while parasites (M') were taken into account. Parasites, and experimental voltage gain. Notably, the models accurately replicate the experimental data.

2.2 Maximum Voltage Stress

In general, the component voltage and current stresses, which are described in Tables I and II, determine the parameters design of a dc–dc converter. To demonstrate the parameter design, we use a hybrid two-quasi Z-source boost dc–dc converter as an example.

Table 1: Maximum Voltage Stress

Parameter	Voltage Stress
C1	$\frac{1-2D}{1-3D}v_{in}$
C2	$\frac{2D}{1-3D}v_{in}$
C3, C4	$\frac{D}{1-3D}v_{in}$
D1,D2,D3	$\frac{1}{1-3D}v_{in}$
S	$\frac{1}{1-3D}v_{in}$

2.3 Maximum Current Stress

The present stresses of the components may be calculated using CCM's steady-state analysis, where dtL = DT denotes the time interval between states 0 and 1, diL = xL percent IL denotes the inductor's current ripple at state 0, and f = 1/T denotes the switching frequency. The inductances of L1-L3 may be written as by substituting the expressions of VL and IL. can be:

Table 2: Current Stress

Parameter	Current Stress
$L_1 - L_3$	I_{in}
D_1	$\frac{I_{in}}{1-D}$
D_2	$\frac{I_{in}}{(1-D)^2}$
D_3	$\frac{1-3D}{1-D} I_{in}$
S	$3I_{in}$

2.4 Estimated Efficiency

Initially, the topology can be considered to function within the specifications given in Table III based on the expected losses of the proposed converter. The expected losses of the components were evaluated using the current stress reported in the preceding section as well as the digital simulation supplied by PSIM simulation software. The expected losses may be determined by using the approach outlined in [1]. Switching and conduction losses are the causes of switch losses.
They may be calculated in the following way:

$$P_s = [I_{s(rms)^2} R_{DS(on)} + \frac{1}{2} f_s V_S I_S (t_{off} + t_{on})]$$

(16)
where Is(rms) is the RMS current flowing through the switches given by RDS(on) is the datasheet-specified MOSFET on-state resistance; ton and off are determined by the device's static characteristic as described in the manufacture datasheet; fs is the frequency of switching Vs is the frequency of switching and Is is the current flowing through the switches during the switching process.
Because the diodes employed are Scotty, their conduction losses are calculated as follows:

$$P_D = 3[I_{D(avg)} u_F]$$

(17)
Where ID(rm) is the sum of the diodes' average currents, where vF is the diode forward voltage, which is calculated based on the datasheet's specifications.
The manufacturer gives the following technique for estimating losses for inductors (L1 and L2) In reality, each component's losses may have an impact on the step-up. the suggested converters' performance we believe that the inductors' dc resistances are rL, and the forward voltage decreases. The on-resistance of the switch is rs, and the diodes are VD. I in is the average input current. The suggested converters' power loss distributions, Hybrid boost dc-dc converter with two quasi-Z sources. below. This computation can also be verified using the applications listed below:

$$P_L = 3[r_L I_{L(rms)^2} + (aB_{pk^b} f_s^c) Aele]$$

(18)
where IL(rms) is the inductor's RMS current, rL is copper resistance; Bpk is the magnetic device core's AC magnetic flux density, a, b, c are constants derived from the core's curve fitting le is the core medium path length (MPL) and Ae the transversal core area.
The following formula may be used to calculate the expected capacitor losses:

$$P_C = 4(I_{C(rms)} ESR)$$

(19)
Where IC(rms) is the RMS current of the capacitor and ESR is the measured resistance. The efficiency (n) The following formula may be used to calculate the converter's efficiency:

$$n = \frac{P_i - (P_{scon} + P_{Sw} + P_D + P_L + P_C)}{P_i}$$

(20)
The suggested converter's estimated efficiency, may be used to calculate the distribution of losses as can be seen in fig 7. As may be observed, diode failures are common. One alternative option is to employ diodes with a low forward voltage value to ameliorate the issue.

2.5 Inductor Parameter Design

Assume that the inductor's maximum allowed current ripple is xL percent. When the suggested converter is in use, it will be following equation may be obtained from state 0:

$$L = \frac{v_L dt_L}{di_L} = \frac{V_L D T}{x_L \% I_L} = \frac{V_L D}{x_L \% I_L f}$$

(21)

Where dtL = DT is the time gap between state 0 and 1. diL = xL%IL while state 0 is the inductor's current ripple, and f = 1/T is the frequency of switching. The inductances of L1-L3 may be represented in the next formula as by plugging the expressions of vL and IL into (19).

$$L_1 = L_2 = L_3 = \frac{D(1-D)V_{in}}{(1-4D)x_L \% I_{in} f}$$

(22)

2.6 The Capacitor Parameter Design

Assume that the capacitor's maximum allowed voltage ripple is xC percent. The following equation may be obtained while the proposed converter is in state 0:

$$C = \frac{i_C dt_c}{dv_c} = \frac{i_c D T}{x_c \% V_c} = \frac{i_c D}{x_c \% V_c f}$$

(23)

where dtC = DT , interval between states 0 and dvC = xC percent VC, the capacitor's voltage ripple during state 0.The capacitances of C1-C4 may be calculated by substituting the formulas of iC and VC into:

$$C_1 = \frac{2D(1-3D)I_{in}}{(1-2D)x_c \% V_{in} f}, C_2 = \frac{(1-3D)I_{in}}{2x_c \% V_{\text{in}} f}$$

$$C_3 = C_4 = \frac{(1-3D)I_{in}}{x_c \% V_E f}.$$

(24)

III. Comparison of the Converters

Table 3: Specification and Components of the Converter

Converter	Gain (M)	Switches Count	Diodes Count	Inductor Count	Capacitor Count	Common Grounded
Proposed	$\frac{1}{1-3D}$	1	3	1	4	Yes
(2)	$\frac{5+D}{1-D}$	2	5	2	5	No
(4)	$\frac{3-D}{1-D}$	2	3	2	3	No
(5)	$\frac{1+3D}{1-D}$	2	7	4	1	No
(6)	$\frac{1+D}{1-D}$	2	1	2	1	No

3.1 Performance Comparison

Table 3 compares similar converters in order to emphasize the benefits of the proposed converter. The first comparison is based on voltage gain, for the whole duty cycle range, the suggested converter has a larger voltage gain. In addition, maximum voltage strains on the switch and diode, respectively. In both of these tests, the suggested converter had less voltage stress than the other converters. As a result, semiconductors with lower voltage levels and inherent resistances can be employed, preserving the converter's efficiency.

IV. Simulation and Experimental

The Hybrid two-quasi-Z-source boost DC-DC converter is simulated and the working principle is based on a cycle of two stages illustrated in Figure 2 and figure 3. The circuit's build according to the parameters as shown in table IV.

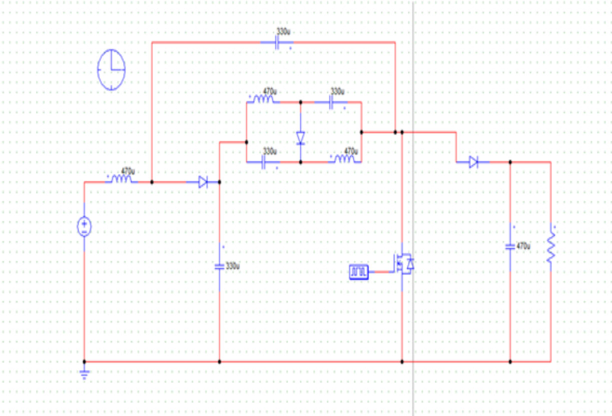

Figure 5: The proposed converter Simulation

4.1 Specification and Components of the Converter

The value of which component of the converter all are showing in the table four, all of them potting working in this project give the great result for in circuit graphics.

Parameter	Value/ Part Number
Input Voltage	20 V
Output Voltage	200 V
Z-source capacitors	300 uF
Z-source inductors	470 uH
Output capacitor	470 uF
Full load	100 W
Switching frequency	30 kHz

4.3 Experiment Results of the Converter

Hybrid two-quasi-Z-source boost dc–dc convert simulation results, when D=0.3. Vin=20V and input current 10 A.

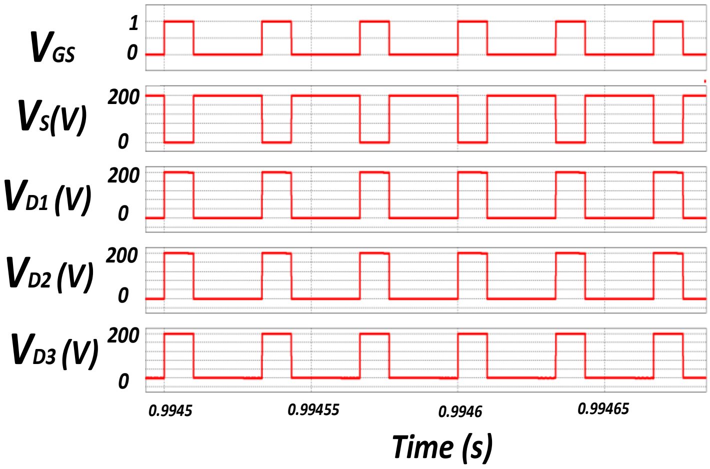

Figure 6: The proposed converter simulation results, graphic of VGS, VS and voltage on diodes VD1 VD2 and VD3.

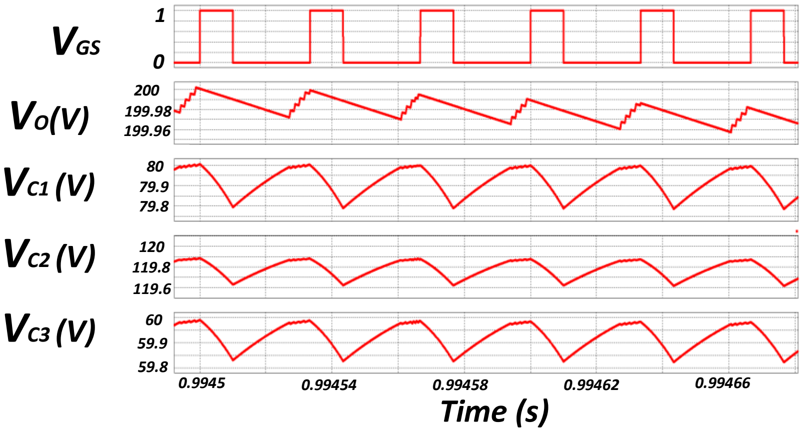

Figure 7: The proposed converter simulation results, graphic Vo, VC1, VC2 and VC3

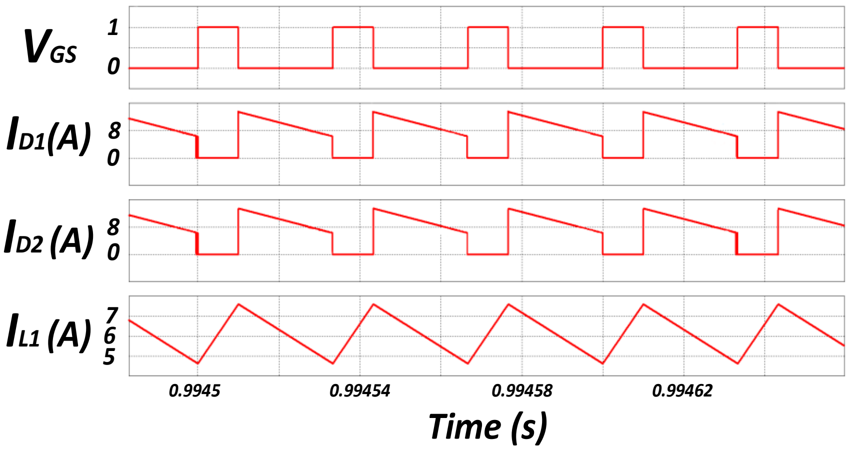

Figure 8: The proposed converter simulation results, graphic of the current on diodes. ID1, ID2 and ID3.

4.4 The Performance of the Proposer

The proposed converter result was run on PISM Simulink software and all the graphics are present in this section, the input voltage 12V DC and current 10A. In figure 6 shows VS, VD1, VD2 as well a VD3 reaching out to 200V. Figure 7 in tutorial Vo is 200V, VC1 to 80V, VC2 to 120V at last VC3 to 60V. In figure 8 the ID1, and ID2 reached out to 8A, and the last one was IL1 to 7A. I rhetorical is 200 V output, output current is 1A output power is 200W.

In addition, and shows a maximum on switch and diode, respectively in the results of the test, the volt strain suggested converter had less voltage stress than the other converters. As a result, semiconductors with low volt levels and inherent resistances may be employed, preserving converter efficiency such as:

High productivity
Gain is significant
Powerful applications
Bucket-boosting procedures
It is possible to get a high output voltage
Complete stability
size is tiny

V. Conclusion

The hybrid Z source converter is designed; the issue of circuit systems is explored in this article. In converters, a hybrid two Quasi-Z source network is built by the combination of the traditional Z-source. The proposed converter preserves all of the benefits, in addition to its superior step-up capabilities. Always input current, decreased capacitor volt stress, the common features among volt source and ground, and the flip bridge.

All graphs and waveforms have been acquired in the simulation section; clearly, the calculated parameters and simulation results are consistent. In the description section, the waveform generated as a consequence of the simulation was discussed.

A hybrid two quasi-z-source boosts DC-DC converter, it presents a small size, very lower cost, batter efficiency, high gain, it presents longer durability. Those parameters qualify the hybrid two quasi-z-source boosts DC-DC converter as one of the best converters in power electronic applications. The converter examined the volt gain. The circuit has demonstrated high performance and efficiency, the proposed provides a high gain for solar PV applications.

Acknowledgments

I kindly want to thank my lovely family, my friends, to give me personal support, and for their patience and kindness. I emit my supervisor Prof. Dr. Yu Tang for wisdom and guidance and my laboratory partners and friends, for being there at every moment to help this project.

Biographical notes: Yu Tang (Senior Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics (NUAA), China, in 2003 and 2008, respectively. He joined the Electrical Engineering Department, NUAA, in 2008. Since 2018, he has been with the State Key Laboratory of Reliability and Intelligence of Electrical Equipment, Hebei University of Technology. He has published more than 80 papers in journals and conference proceedings. His research areas include power electronics in renewable energy generation.

Biographical notes: JOSE FILIPE ZINGA TOMAS was born in Cabinda, Angola. He received his BSC. Degree from the Hebei University of Technology in 2019, and now is currently pursuing his MCS degree from Hebei University of Technology, China. His main areas of research focus on Power Electronics Control and system.

References

[1]. Veerachary, M., and Kumar P., Analysis and Design of Quasi-Z-Source Equivalent DC-DC Boost Converters. 2020. 56(6): p. 6642-6656.
[2]. Salvador, M. A., et al., Nonisolated high-step-up dc-dc converter derived from switched inductors and switched-capacitors. 2020. 67(10): p.8506–8516.
[3]. Shiluveru, K., Singh, A., Ahmad A., and Singh, R. K., Hybrid buck-boost multioutput quasi-Z-source converter with dual DC and single AC outputs. 2019. 35(7): p7246-7260.
[4]. Tang, Y., et al., Hybrid switched-inductor converters for high step-up conversion. 2019. 62(3): p.1480–1490.
[5]. Maroti, P. K., et al., New tri-switching state non-isolated high gain dc-dc boost converter for microgrid application. 2019. 12: p. 2741–2750.
[6]. Tang, Y., Sun, H., and Wang, S., (2020) A Family of High Step-Up Quasi Z-source Inverters with Coupled Inductor. 2020. 13: p. 5667.
[7]. Haji-Esmaeili, M, M., Babaei, E., and Sabahi, M., High step-up quasi-Z source DC-DC converter. 2018. 33(12): p. 10563-10571.
[8]. Torkan, A., and Ehsani, M., A novel nonisolated Z-source DC-DC converter for photovoltaic applications. 2018. 54(5): p. 4574-4583.
[9]. Zhu, X., and Zhang, B., High step-up quasi-Z-source DC-DC converters with single switched capacitor branch. 2015. 5(4): p. 537-547.
[10]. Liu, C., et al., Novel hybrid LLC resonant and DAB linear DC-DC converter: Average model and experimental verification. IEEE Transactions on Industrial Electronics 64(9): p. 6970-6978.
[11]. Bussa, V. K., et al., Single-phase high-voltage gain switched LC Z-source inverters. IET Power Electronics 2018. 11(5): p.796-807.
[12]. Zeng J., et al., A quasi-resonant switched-capacitor multilevel inverter with self-voltage balancing for single-phase high-frequency AC microgrids. 2017. 13(5): p. 2669-2679.
[13]. Vetriselvi, G., Selvaraj, P., and Baskaran, J., Designing of high voltage gain Z-sources DC-DC converter with soft switching in modified PMSG wind-PV module in 2017 International Conference on Computation of Power Energy Information and Communication (ICCPEIC) IEEE 2017.p. 722-725.
[14]. Jeyasudha, S., and Geethalakshmi, B., Steady-State Analysis in Continuous Conduction Mode of a Novel Z-Source Boost Hybrid Converter in 2018 International Conference on Recent Trends in Electrical, Control, and Communication (RTECC) 2018
[15]. Kumari, L., and Jain, A., Slip power recovery drive using Z-source inverter in 2019 International Conference on Smart Systems and Inventive Technology (ICSSIT). 2019.p: 304-308
[16]. Rahul, J., R., Kirubakaran, A., and Das, C. K., A Novel Hybrid Quasi Z-source Based T-Type Seven-Level Inverter in 2018 8th IEEE India International Conference on Power Electronics (IICPE) 2018.
[17]. Kim, B., and Lavrova, O., Quasi-Z-Source Resonant Full-Bridge Converter for Wireless Power Transfer with Sliding Mode Model Predictive Control in 2020 IEEE Power and Energy Conference at Illinois (PECI) 2020.
[18]. Shen, H., et al., (2016) A common grounded Z-source DC-DC converter with a high voltage gain. 2016. 63(5): p. 2925-2935.
[19]. González-Santini, N., et al., Z-source resonant converter with power factor correction for wireless power transfer applications. 2017. 31(11): p.7691-7700.
[20]. Lee S S and Heng Y E (2016) Improved single-phase split-source inverter with hybrid quasi-sinusoidal and constant PWM. IEEE Transactions on industrial electronics 64, 2024-2031
[21]. Veerachary, M., and Kumar, P., Analysis and design of fourth-order quasi-Z-source equivalent DC-DC boost converter in 2019 IEEE Transportation Electrification Conference (ITEC-India). 2019.
[22]. Ajaykumar, T., and Patne, N. R., Hybrid Multi-Cell Single-Stage Reduced Switch Multilevel Inverter in 2020 IEEE International Conference on Power Electronics. Smart Grid and Renewable Energy (PESGRE2020). 2020.
[23]. Rostami. S., Abbasi. V., and Blaabjerg, F., Implementation of a common grounded Z-source DC-DC converter with improved operation factors. 2019. 12(9): p. 2245-2255.