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# Impact of RC Snubber on Switching Oscillation Damping of Cascode GaN Transistors

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***Abstract:***
*Currently, the Cascode structure is widely used for high voltage normally-on GaN devices. Due to the rapid switching speed of GaN transistors, switching oscillations and electromagnetic interference (EMI) become more severe. It is possible for the device to be destroyed by divergent oscillation if it is turned off at a high current. To suppress such unwanted oscillations, adding RC snubber branches was considered an effective method. This paper studies the characteristics and operation principles of a 600 V cascade GaN HEMT. In addition, the effect of using a snubber circuit on the dynamic performance of GaN cascade is investigated. The device is simulated using LTspice simulation. The results show that using RC snubber circuit improves the device's dynamic performance and significantly reduces the high-frequency oscillations under high-current turn-on and -off conditions.*

***Keywords****: Cascode GaN, Dynamic Response, LTspice, Oscillation, RC snubber Circuit, Double-Pulse Tester (DPT).*

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## I. Introduction

Nowadays, silicon (Si) based power devices have reached their possible material limits, e.g. temperature operation, maximum switching frequency, and blocking voltage. Silicon carbide (SiC) and gallium nitride (GaN)-based power devices are attractive candidates for high-power and high-frequency switching. Both technologies are commercially available from different manufacturers. Although these technologies are improving rapidly [1,2]. Compared to Si devices and due to their higher breakdown field and the thinner drift region, the on-state resistance and parasitic capacitances of wideband gap semiconductor (WBG) semiconductors are lower [3]. SiC power devices with a range of 650 V-1.7 kV are available from several manufacturers in different packages. SiC MOSFETs ranging 2.2 kV, 3 kV, 3.3 kV, 10 kV and 15 kV can be found in the literature [4–7]. Further, the GaN switch with enhancement mode (E-mode) is still limited to the 650 V range. A Cascode GaN switch rated 900 V has recently become available by Transphorm. A 1200 V E-mode from GaNPower International is recently introduced [8,9].

Most of the research on false turn-on focuses on the enhancement-mode GaN devices, whereas there is still little published research on GaN devices in cascode configuration due to the package parasitic component and comparatively complicated structure. In the depletion mode GaN devices, a low-voltage Si-MOSFET is typically connected in series to control the on-off state of high-voltage GaN devices, which is well known as cascode structure. In the cascode configuration, the interaction between two devices may result in instability due to the package parasitic inductance [10,11]. Further, junction capacitances of two devices also play an important role in the dynamic performance of the cascode device. The capacitance charge of a high-voltage GaN device is typically larger than the low-voltage silicon MOSFET [12]. The common source inductance shared by the power loop and the gate drive loop can worsen the false turn-on problem, because of the voltage drop on this inductance, which is induced by the fast-changing displacement current in the power loop. However, a comprehensive and in-depth overview is still lacking on this topic.During dynamic switching, however, fast switching is accompanied by oscillation phenomena. Inductance and capacitance in gate and power loops are more affecting the switching. It is, therefore, necessary to develop an accurate model in order to optimize and predict WBG device switching behavior. Under different operating conditions, the mathematical model can determine the limitations factor of the WBG, such as thermal and switching frequency limits.In [13], a piecewise linear model is presented without parasitic inductances and capacitances. According to some references, the SiC MOSFET model can be derived using conventional modelling methods of a Si MOSFET [14]. PSpice simulator is used to simulate the WBG [15].

In this paper, the dynamic switching performance of available commercial SiC and GaN devices is investigated. The study includes static and dynamic characteristics for different gate resistances, different load

currents, and at various temperatures. The simulations have been performed in LTspice using the standard double-pulse tester (DPT). The power losses are calculated by considering the parasitic elements of the gate and power circuits in DPT.

## II. Cascode Configuration

The cascode configuration of the integrated GaN FET in series with a low-voltage Si-MOSFET is shown in Figure 1. Several parasitic inductances are included in a cascode package due to the interconnections between the GaN and Si-MOSFET chips and the outer terminals. The mutual effects between these parasitic inductances become more important at high switching currents. As a result, undesirable switching oscillations and hence high switching losses occur which in turn limit the dynamic performance.

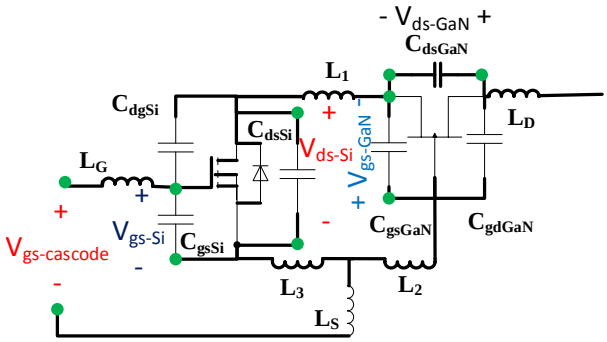


**Figure 1:** Schematic of cascodeGaN normally-off operation

## III. Dynamic Performance of Cascode GaN Transistor

In this work, the standard DPT circuit with inductive load, see Figure 2, is used to evaluate the switching performance. The gate-source voltage ($V_{gs}$), drain-source voltage ($V_{ds}$), and the drain-source current ($I_{ds}$) at the end of the first pulse and at the beginning of the second pulse are recorded. This gives the dynamic turn-off and turn-on processes, respectively.The dynamic characterization is done at different input voltages ($V_{dc}$), load currents ($I_{load}$), external gate resistances ($R_g$), and case temperatures.

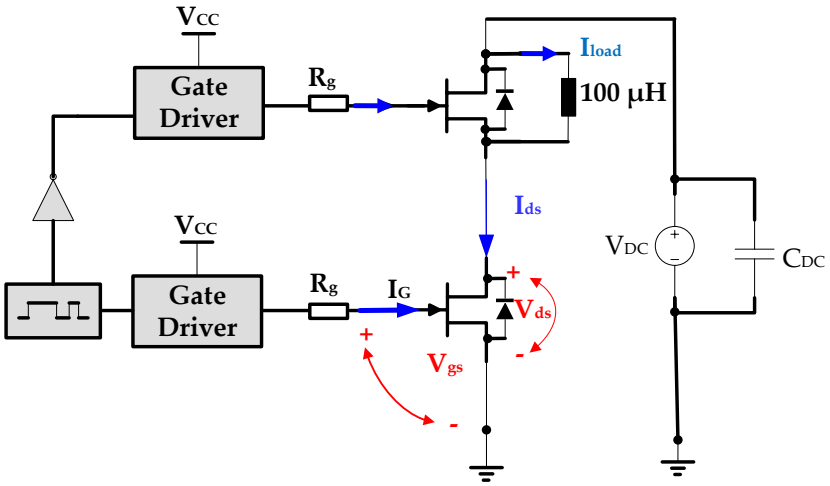


**Figure 2:** schematic of standard DPT.

The switching characteristics of the devices are simulated by LTSpice-IV using the model delivered by the manufacturer. The switching simulation are conducted up to 600 V with different load current and different gate resistances. The main parameters of the device under test (DUT) used in this work are listed in Table-I.

**Table 1:** Main parameters of DUT

| Parameters | TP65H015G5WS (based on datasheet) |
|---|---|
| Drain-Source Voltage, $V_{ds}$ | 650 V |
| Drain-Source Current, $I_{ds}$(100°C) | 60 A |
| On-State Resistance, $R_{on}$(25 °C/ 150 °C) | 15/ 30 Ω |
| Gate-Source Voltage, $V_{gs}$(Turn off/ Turn on) | 0 / 12 V |
| Input capacitance, $C_{iss}$ | 5218 pF |
| Output capacitance, $C_{oss}$ | 307 pF |
| Reverse transfer capacitance, $C_{rss}$ | 4.5 pF |

Figure 3 shows the impact of the gate resistance on the switching using the internal body diode of the cascodeGaN. When a small gate resistance is used, the fast switching speed produces high ringing in the gate waveforms, which may cause the device to turn on or off unintentionally. The gate resistance should be chosen to ensure that ringing at the gate drive signal is sufficiently damped, and the parasitic inductance must be minimized by minimizing the gate driver loop and power circuit loop.

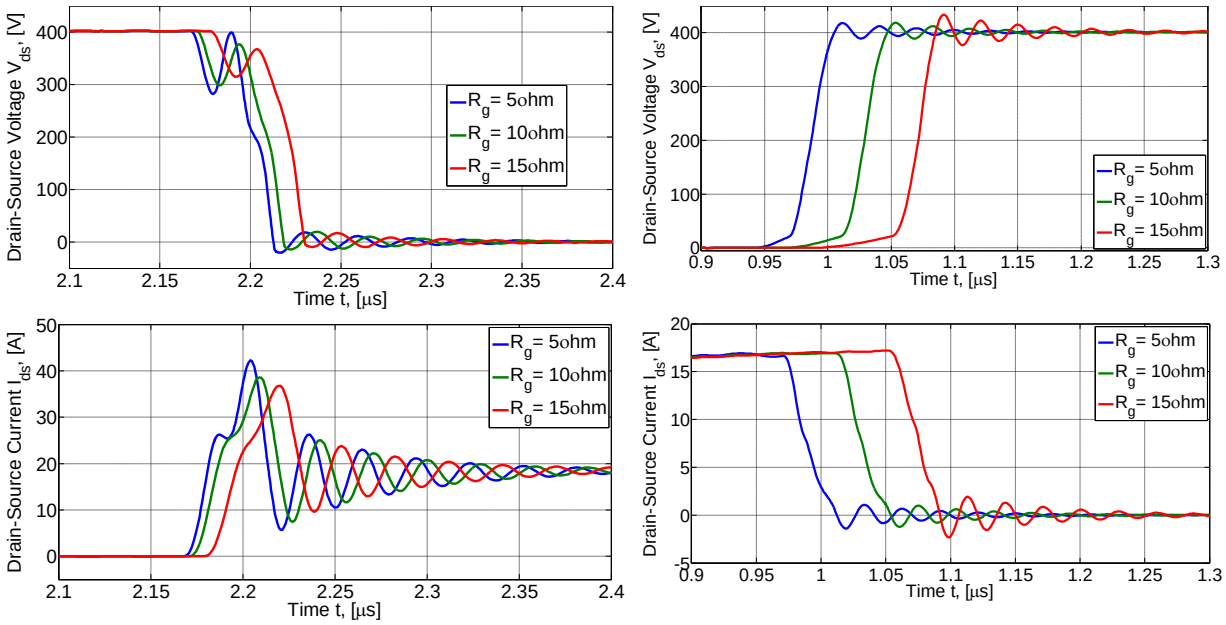


**Figure 3:** Dynamic response with different $R_g$ and $V_{ds}$= 400 V and $I_{load}$of 18 A: (a) Turn-on and (b) Turn-off

Further, the effect of using different input DC voltages is simulated. Figure 4 depicts this influence with a constant load current of 18 A and variable $V_{ds}$ between 200V and 600V.As shown in Figure 4, as the input voltage increase, the reverse recovery increases, because the capacitive charge increases with the applied voltage.

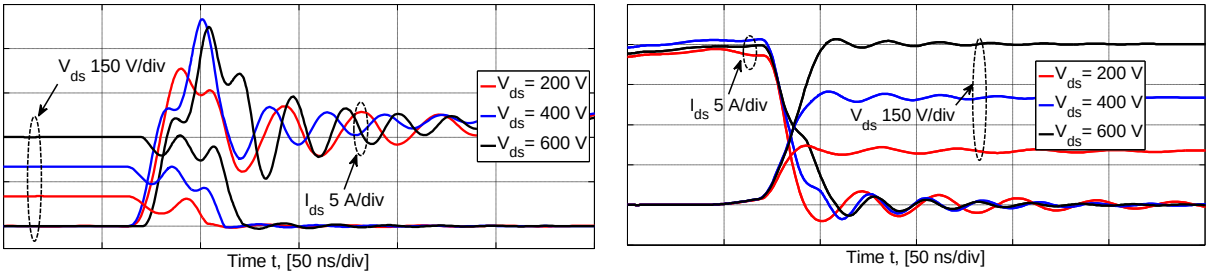


**Figure 4:** Dynamic response with different $V_{ds}$ and $R_g$= 5Ω and $I_{load}$of 18 A: (a) Turn-on and (b) Turn-off

Further, the influence of the different load currents is also investigated. Figure 5 depicts the effect of using different Ids. As shown, the oscillation has become more dangerous as the load current increase.This could lead to false turn-on of the devices and hence destroy these devices.

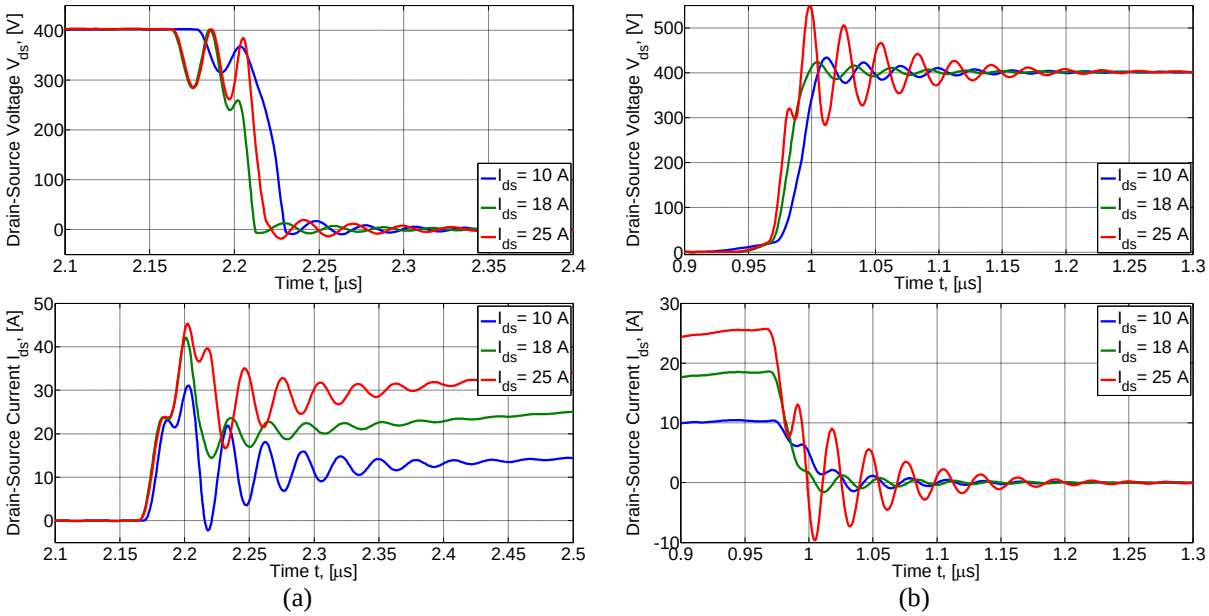


**Figure 5:** Dynamic response with different $I_{ds}$ and $R_g$= 5Ω and $V_{ds}$= 400V: (a) Turn-on and (b) Turn-off

## IV. Snubber Circuit Design

In this paper, the RC circuit is used to damp effectively the switching oscillation. A typical RC snubber configuration in a half-bridge is shown in Figure 6. The snubber capacitor ($C_{snubber}$) and a snubber resistor ($R_{snubber}$) are connected in series. The path of the oscillation current in a half bridge topology is illustrated in Figure 6.

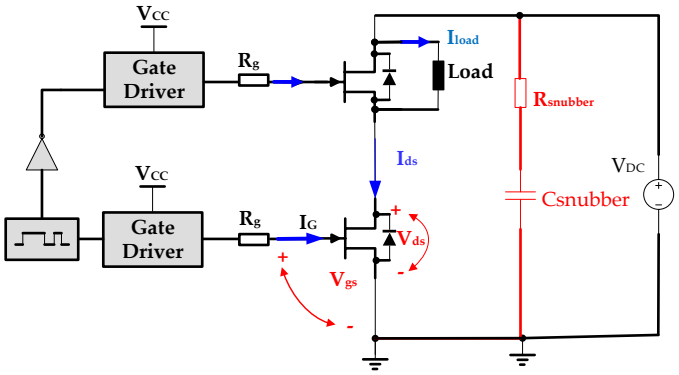


**Figure 6:** Typical DPT circuit With RC snubber.

Based on the equivalent circuit of the switching during both turn-on and –off transitions, the values of the RC elements can be calculated as follows [16]:

$$C_{snubber} > \frac{L_{power}\ I_{load}^2}{V_{ds-peak}^2 - V_{dc}^2} \quad (1)$$

$$R_{snubber} < \frac{-1}{f_{sw}\, C_{snubber}\ \ln(V_{ds-peak} - V_{snubber})/V_{ds-peak}} \quad (2)$$

Where $L_{power}$ is the total parasitic inductance of the power loop, $V_{ds\text{-}peak}$ is the peak overshoot, $f_{sw}$ is the switching frequency, $V_{snubber}$ is the discharge voltage of snubber, e.g. ≈ 90% $V_{snubber}$.

## V. Results and Discussion

The DPT is implemented under the conditions of 400 V and 30 A with the variation of RC snubber values. The comparisons with and without applying RC circuit are shown in Figure 7. The results show a good reduction in oscillations during turn-on and –off transitions. Further, the transition response in the aspects of

on/off time, slew rate of drain current (di/dt) and drain-source voltage (dv/dt) during turn-on and -off transitions are not significantly affected, which results in constant switching losses.

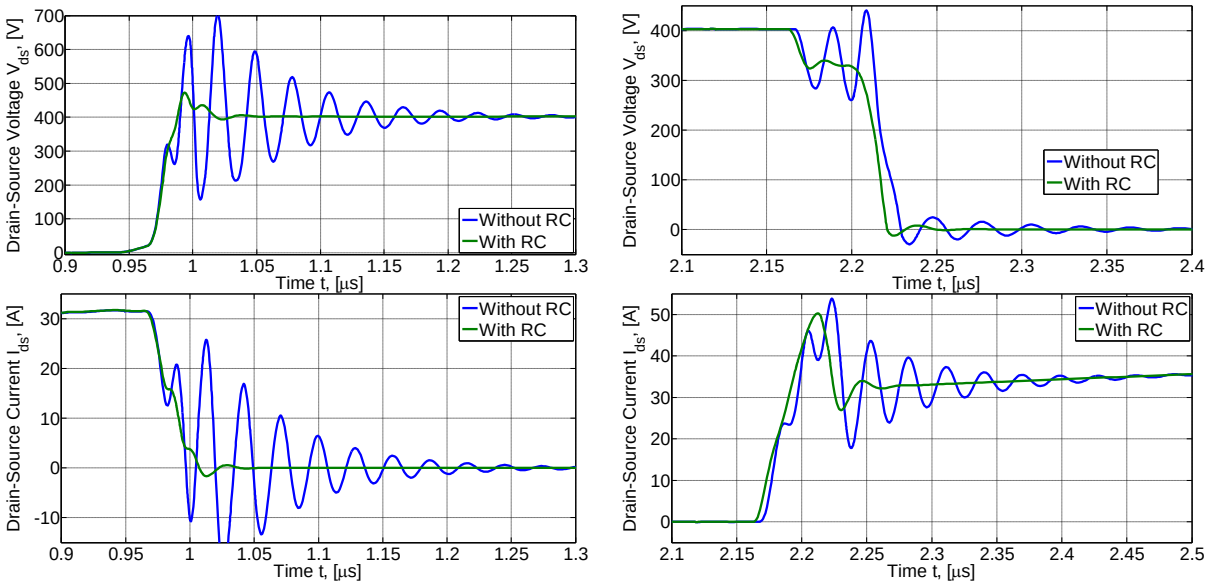


**Figure 7:** Impact of RC Snubber on Switching Oscillation: (a) Turn-on and (b) Turn-off. Test conditions: $I_{ds}$= 30 A, $R_g$= 5Ω and $V_{ds}$= 400V.

As shown, the impact of RC snubber on switching oscillations during turn-on and turn-off is visible. Adding an RC snubber branch allows switching oscillation to be effectively avoided and high-frequency oscillations can be reduced without affecting switching losses. In consequence, high-frequency EMI noise will be reduced.

## VI. Conclusion

For high voltage normally-on GaN devices, the Cascode structure is widely used. EMI and switching oscillations are more severe in GaN transistors due to their fast switching speeds. In this paper, using LTspice simulation, RC snubber branches were considered an effective method for suppressing such unwanted oscillations. Additionally, the effect of using a snubber circuit on the dynamic performance of GaN cascades is investigated. Under high-current turn-on and -off conditions, using RC snubber circuits significantly reduces high-frequency oscillations and improves dynamic performance.

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