Design and Simulation of PFC Circuit for AC/DC Converter Based on PWM Boost Regulator

Mahmoud Milad Alagele, Adel A M Abosdel
Engineering Academy-Tajoura,   Al Zaytuna University

Abstract: *In this paper a simple power factor correction PFC circuit was designed, simulated and tested for AC/DC converter which generates input current harmonics due to its non-linear characteristics. PFC was achieved through current harmonics mitigation by using PWM boost regulator. The circuit utilizes the charging and disc arching increments of boost inductor current to shape a sinusoidal input current. Inductor current was controlled by means of PWM controller. The controller accepts two feed back signals, the first is the inductor current and the other is the output voltage of the AC/DC converter. The simulation results of fast fourier transform FFT show a grate reduction in current harmonic which in turns tends to a grate improvement in power factor.*

I.   Introduction

Currently, the electrical power industry has grown rapidly and loads are changing from simple, non-electronic loads such as tungsten lamps, motors, relays and resistive heaters to electronic ones such as fluorescent lamps, motors with solid-state drivers and industrial drives. These electronic loads (also known as non-linear loads which draw a non-sinusoidal current even when the supply voltage is perfectly sinusoidal) [1] are the major sources of excessive current harmonics which leads to power quality PQ pollution introduced in electrical grids. The current harmonics has a significant effect on customer loads in a form of heating, distortion or operation malfunction.

Harmonic disturbances are the most researched part of all power quality disturbances, especially over the past two decades. The interest in harmonics research can largely be attributed to the advance in power electronics technologies, and this driven by the desire to have more energy efficient equipment and greater control of equipment operation. PFC and harmonics mitigation technologies can be essentially classified into two main categories 1) Passive methods and 2) Active methods

The first methods are simply based on the use of RLC filter that offer a low impedance path for unwanted current harmonics and drive it back away from the load under consideration. These filters have no switches and hence no electromagnetic interference emissions EMI. Beside that it is very simple, robust and has low cost of implementation. However, their performance lower when compared to active circuits, they are heavy bulky specially when designed for low harmonics mitigations. Passive filters are employed either to shunt the harmonic currents off the line or to block their flow between parts of the system by tuning the elements to create a resonance at a selected harmonic frequency [2].

The second technology use switching circuits controlled actively. Some of active technologies based on harmonics-injection techniques and called active filters. The active filter senses the harmonics distortion, and injects currents that are 180 degrees out of phase with the harmonic frequencies that exist in the system. They have the distinct advantage that they do not resonate with the system. They can be used in very difficult circumstances where passive filters cannot lies. They can also address more than one harmonic at a time and combat other power quality problems such as flicker [3]. An other active technique are based on DC-DC switching converters filters that usually applied to the circuits that contain AC to DC converter such as DC motor drive, switched mode power supply and battery chargers. These types of filters are based on current wave shaping technique in which the line current is forced to follow the sinusoidal line voltage. A controlled high frequency pulse width modulation (PWM) applied on the DC-DC converter which is the main component of the filter

Standardization activities in this area of harmonics limitation have been carried out for many years. As early as 1982, the International Electrotechnical Committee - IEC published its standard IEC 555-2, which was also adopted in 1987 as European standard EN 60555-2, by the European Committee for Electrotechnical Standardization - CENELEC. IEC 555-2 standard has been replaced in 1995 by standard IEC 1000-3-2, also adopted by CENELEC as European standard EN 61000-3-2 (IEC Standards 1998). Standard IEC 1000-3-2 applies to equipment with a rated current of up to and including 16A rms per phase which is to be connected to 50Hz or 60Hz, 220-240Vrms single-phase, or 380-415Vrms three-phase mains [4].

II.   The Proposed Pfc Circuit

The proposed PFC circuit is designed for AC-DC converter and it considered as nonlinear load. The PFC circuit is essentially based on current wave shaping technique. Boost DC-DC regulator with high frequency PWM controller are utilized, the controller gets the two control signals and generate the PWM switching pulses accordingly as shown in figure 1.

Feeding the input current reference signal and the DC voltage ripple reference into the switching controller will yield both harmonic reduction and DC voltage regulation. The principle of operation for DC-DC switching regulator harmonic filtering is related to the topology of DC-DC converter through which PWM is performed. Among the different power regulators topologies boost converter shown in Figure.1 is the most suitable one, where the boost inductor is in series with the ac power line. This result in minimum conducted electromagnetic interference (EMI) at the line when the circuit operates in continuous conduction mode (CCM) [5].
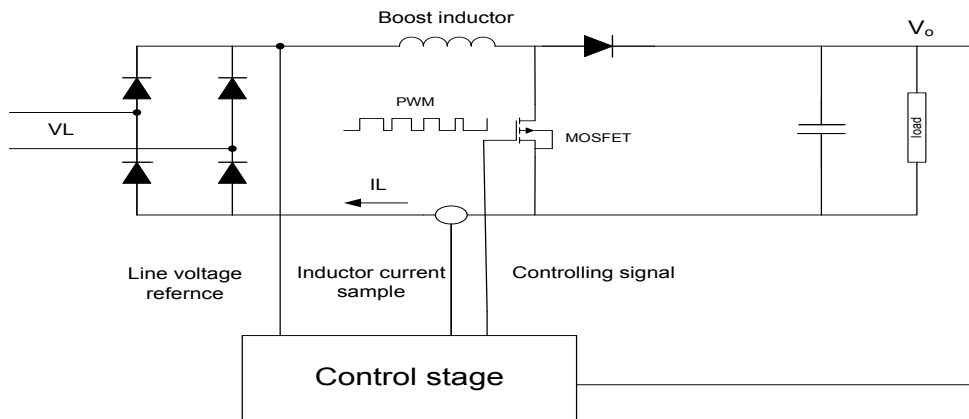
Figure 1: Boost DC-DC Switching Converter Filter

For our boost regulator topology, the input current shaping is performed by controlling the amplitude of boost inductor current, and this in turns is done through the controlling or the modulation of switching pulses.

When the boost switch is turned ON, the inductor current tends to rise due to charging of boost inductor, and when the switch turned OFF, the inductor current will decay down by discharging through boost capacitor. The rise increment is given by equation.1 [6]. These increments up and down of boost inductor current are the key of current shaping.

$$\Delta i_L = \frac{\sqrt{2}V(t)D}{LF_s} \qquad (1)$$

where

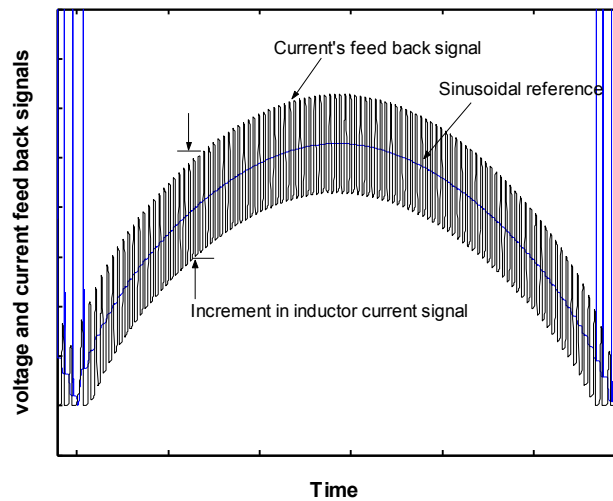|	
Δi_L	Increment in inductor current
$V(t)$	Instantaneous phase voltage
D	Duty cycle of boost switch
L	Boost inductor
F_s	Switching frequency of boost converter

Figure.2 Simulation Shows How the Boost Inductors Ripples Follow the Sinusoidal Reference.

III. Powr Stage Design

The parameters of the designed power stage are listed in Table.1, in which the converter parameter include boost inductance boost capacitance, and also input line voltage, DC output voltage and rated power.

Table.1 Parameters of ASD with Inherent Boost DC-DC Switching Converter Filter

Parameter	Value
line voltage	110 *V rms*
DC output voltage	300 *V*
Motor power	1 *KW*
Boost inductance	1 *mH*
Boost capacitance	6200 *μF*

A) Boost Inductance

It is one of the keys components in the design. The value of this inductor significantly affects the ripple current due to switching operation of boost converter. Inductance value was calculated to give an acceptable level of ripple current which is chosen between 10% and 20% of the peak value. The peak to peak ripple current for any input/output voltage combination can be approximately found by the formula given in equation.2 [7].the value of boost inductance also affect the regulator's mode of operation, higher inductance value moves the regulator to work in discontinues conduction mode DCM mode where the current does reach the zero level which not preferred due to its EMI pollution.

$$\Delta I_{p-p} = \frac{V_{IN}(V_{OUTDC} - V_{IN})}{f L V_{OUTDC}}$$

(2)

Where

V_{IN} Peak value of input full wave rectified waveform

V_{OUTDC} Output DC voltage

f Switching frequency

L Boost inductance

For the values of line voltage = 110 *V rms*, output DC voltage = 300 *V*, input current = 9.82 *A rms* and switching frequency of 20 *K Hz*, the inductance value is calculated and found to be 1 *mH*.

B) Boost capacitance

The capacitance was calculated using the formula in equation 3. [8],

$$C_{OUT} = \frac{2Pt_{HLD}}{V_1^2 - V_2^2} \tag{3}$$

Where

P Rated output power

t_{HLD} Holdup time

V_1 Capacitor voltage at the beginning of t_{HLD}

V_1 Capacitor voltage at the end of t_{HLD}

The parameters that affect the choice of the boost capacitance include:

- Holdup time capability which is the amount of time at rated output power that will take the capacitor voltage to discharge to a minimum operating voltage.
- Output DC ripples current.

For holdup time of 20 *ms*, V_1 at the rated output DC voltage, V_2 of 290 *V* and rated power of 1 *KW*, the boost capacitance is calculated to be 6200 *µF*.

IV. PWM Controller Design

       PWM controller responsible of generating switching pulses for boost regulator to perform two functions; sinusoidal current shaping and maintaining constant and stable output voltage. For this reasons the controller is designed with two feedback signal, one from output voltage of the converter and the other from input line current which is equivalent to boost inductor current as shown in figure (3).
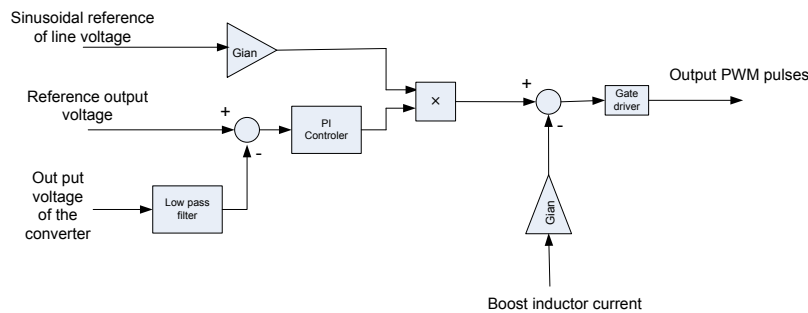

Figure 3: PWM Controller with Two Feed Back Loops

       Low pass filter is used to control the out put ripple voltage of the converter and the reference voltage is used to select the required level of output voltage. Sinusoidal reference is taken as pattern over which the line current is shaped. Gains are used to modify the signal to next controlling stage. The error signal that used as an input for gate driver is generated from comparing the boost current with modified sinusoidal reference after the product. Gate driver generate positive pulse when the error is positive and zero voltage when the error is negative and it works as PWM modulator.

V. Simulation Results

       CCM boost converter was simulation by Matlab, the effect of duty cycle on inductor current saw tooth and output voltage are monitored and calculate.

       Simulink model was used to simulate a PFC circuit for single phase AC/DC converter; the converter can also work as Adjustable Speed Drive ASD by adjusting the output voltage reference in PWM controller. The fast Fourier Transform FFT analysis was applied to the input current of ASD to calculate the harmonic content of the input current which used to calculate the power factor of the ASD circuit before and after PFC.

       Figure 4 shows the input line current after PFC, it is clear that the current tends to rush up at the beginning of operation for a part of half cycle. This is because the output capacitor is empty of charge and works as short circuit at that point. This problem can be solved by using a soft starting circuit which is out of our scope.

       In figure 5, the inductor current (input current) appears as saw tooth due to charging and discharging phases of boost inductance. The conduction point between charging and discharging is kept at none zero value which indicates that the converter works in CCM.
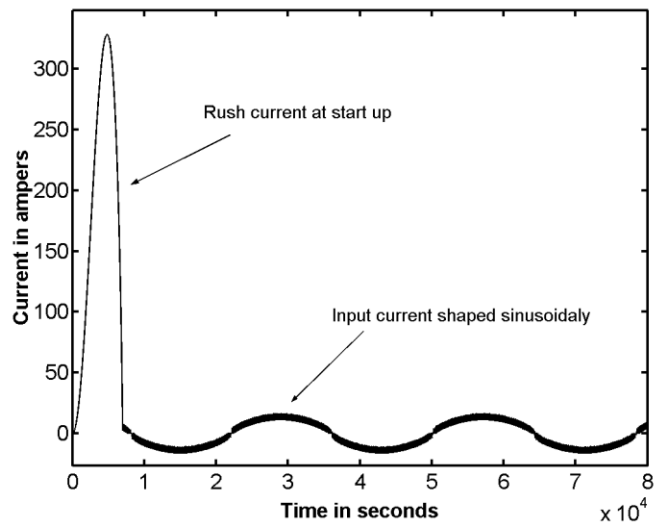
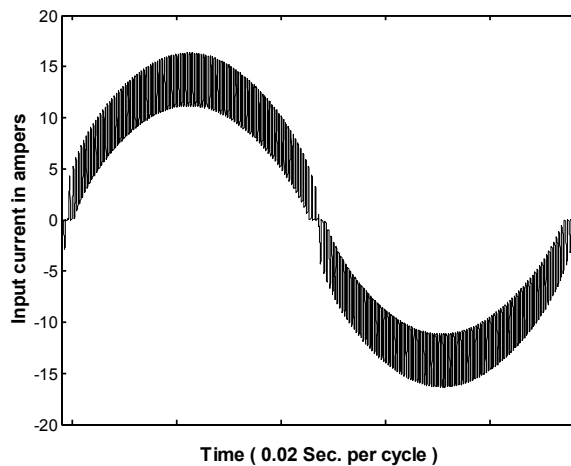Figure 4: Shows the Input Line Current after PFC

Figure 5: Inductor Current Made of Charging and Discharging Phases

Figure 6 shows the input current plotted over the line voltage. PFC achieve unity displacement factor that can be noted from zero phase difference between current and voltage. Also PFC achieve near unity distortion factor due to small harmonics contents of input current and this can be noted visually from a sinusoidal shape of the current and numerically for the result of FFT analyser.
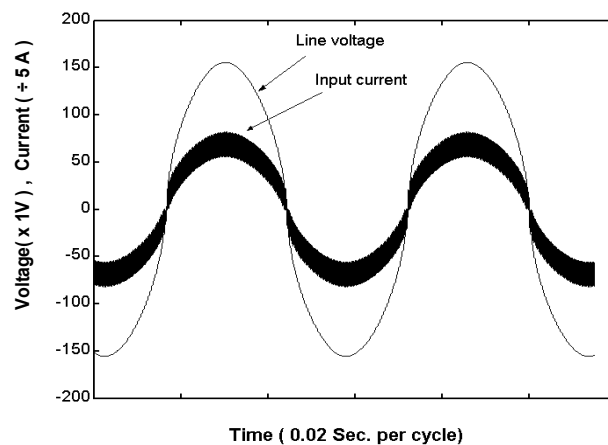

Figure 6: Shows The Input Current Plotted Over The Line Voltage.

The FFT analysis was applied to the input line current generated by the Matlab simulation model. The ASD model is designed to work at a maximum DC output voltage of 300 V, and load of 80 Ω. All measurements were taken at this operating point. Analysis was performed before and after PFC.

The harmonics plot prior to the mitigation is shown in Figure 7. It shows a significant 3rd, 17th and 19th harmonics of 4.85 *V*, 4.85 *V* and 9.26 *V* respectively. Exact odd harmonic levels are listed in Table 2. Different RMS values of phase current are given in Table 3.
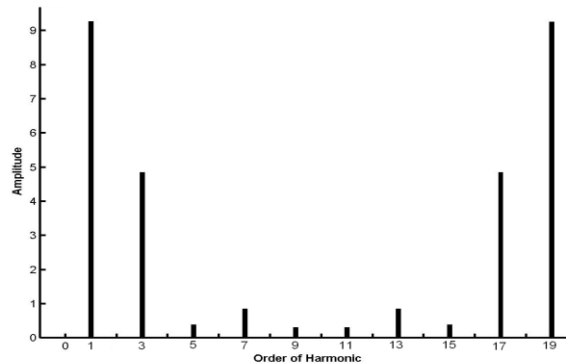

Figure 7: Odd Harmonics Plot Prior to the Mitigation

Table 2:. Odd Harmonics Levels Prior to the PFC

Harmonic Order	DC	1st	3rd	7th	13th	17th	19th
Harmonic Amplitude in *A*	0.00	9.26	4.85	0.86	0.86	4.85	9.26

Table 3: RMS Values of Phase Current before PFC

Total RMS Current	DC Current	Fundamental RMS Current	Harmonics RMS Current
10.5 *A*	0.00 *A*	6.55 *A*	8 *A*

Harmonics mitigation are achieved by using inherent boost DC-DC switching regulator in which harmonics levels were significantly reduced. Figure 8. shows the odd harmonics plot after mitigation. Exact odd harmonic levels are listed in Table 4. Different RMS values of input phase current are given in Table 5.
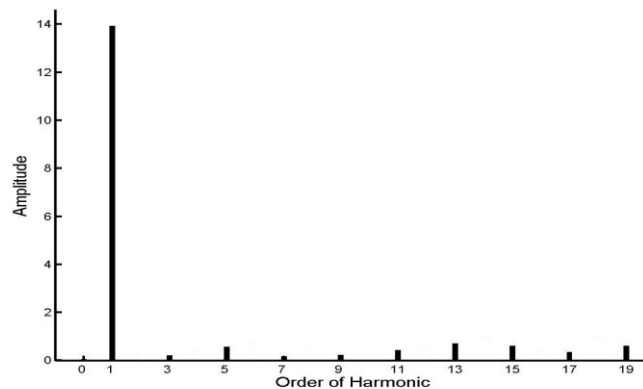

Figure 8: Odd Harmonics After Mitigation

Table 4: Odd Harmonics Levels after PFC

Harmonic Order	DC	1st	3rd	5th	7th	9th	19th
Harmonic Amplitude in *A*	0.6	13.97	0.56	0.48	0.34	0.13	0.76

Table 5: RMS Values of Phase Current after PFC

Total RMS Current	DC Current	Fundamental RMS Current	Harmonics RMS Current
9.99 *A*	0.11 *A*	9.88 *A*	1.48 *A*

The presence of a significant 19th harmonic before PFC is due to switching frequency of DC-DC boost regulator. The 19th harmonic amplitude was mitigated from 9.26 A to 0.76 A, 3rd and 17th are also significantly mitigated. Harmonics mitigation results in a huge improvement in power factor improved from 62.3 % to 98.8 %.

VI.   Conclusion

A single phase power factor correction PFC circuit using pulse width modulated PWM boost regulator has been proposed for AC/DC converter. The design circuit has achieved both output voltage regulation and PFC with two feed back signal from output voltage and input current. Simulation was performed and shows good result in harmonic mitigation and output voltage regulation. Harmonics mitigation results in a huge improvement in power factor improved from 62.3 % to 98.8 %.

References
[1]   Tristan, A. K., P.E., 1999. Distortion and power factor of nonlinear loads. *LTK Engineering Services*: 0-7803-5533-4/99/$10.00.
[2]   Bernard, S., 1995. Harmonics Pollution. http://www.powers quality.com/art0041.
[3]   Akagi, H., 1996. New trends in active filters for power conditioning. *IEEE Transaction on Industry Applications*.
[4]   IEC 1000-3-2 (1995-3) Ed.1, 1995. Electromagnetic compatibility (EMC) - part 3-2: limits - limits for harmonic current emissions (equipment input current ≤16a Per phase). *IEC.*
[5]   Zhou, C., Raymound B. R. & Fred C. L. 1990. Design and analysis of a hysteretic boost power factor correction circuit. *IEEE*
[6]   Phillip C. T., 1999. Boost power factor corrector design with the UC3853. ©, Texas *Instruments Incorporated.*
[7]   Fairchild, 1997. Theory and application of the ML4821 average current mode PFC controller. *REV* **1**: 0 10/25/2000.
[8]   Harding, J., Off-line power supply using the farm ac front-end module. *Vicor Corporation. Applications Engineer*: 800.927.9474.