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Power Optimized Programmable Embedded Controller Using Icg

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Abstract: *In this proposed work I have design and implemented 8 bit microcontroller using intelligent clock gating to optimize the power of PEC.power optimization is a key factor in high integrated vlsi chip.The increasing prominence of portable systems and need to limit power consumption (and hence, heat dissipation) in very high density VLSI chips have led to rapid and innovative development in low power design during the recent years . The driving forces behind these developments are portable device application requiring low power dissipation and high throughput, such as notebook computers . Portable communication device, and personal \digital assistants (PDAs) . In most of these cases , the requirements for low power consumption must be met along with equally demanding goals of high chip density and high throughput. Hence, low power design of digital integrated circuits has emerged as a very active and rapidly developing field. Clock gating is a well-understood power optimization technique employed in both ASIC and FPGA designs to eliminate unnecessary switching activity. This method usually requires that the designers add a small amount of logic to their RTL code to disable or deselect unnecessarily active sequential elements registers.*
Results shows that ICG is very effective in power optimizationof PEM as it reduces power by adding small amount of logic to their RTL code to disable or deselect unnecessarily active sequential elements registers.TheVerilog code for all the modules is written in a hierarchical fashion starting with the smallest units and progressively, building upon them to develop the entire structure. Simulation of the entire FPGA is done to verify the functionality following which, synthesis and design implementation is carried out.
Keywords:*Power, Clock Gating, Intelligent Clock Gating,Dcg,Fpga,Xilinx*

I. Introduction

Low power consumption in embedded systems has become a key factor for many applications. Portable applications, needing long battery life together with highpeak- performance, are demanding a very careful design at all levels.The most important factor contributing to the powerconsumption is the switching activity .

Once the technology and supply voltage have been set , major power savings come from the careful minimization of switching activity. While some switching activity is functional, i.e. it is required to propagate and manipulate information; there is a substantial amount of unnecessary activity in almost all digital circuits. Unnecessary switching activity arises from spurious transitions due to unequal propagation delays (glitches) and transitions occurring within units that are not participating in a computation. One way to avoid these activities is by dynamically turning off the clock to unused logic or peripherals .

Therefore, reducing the power dissipation of integrated circuits through design improvement is also becoming a major challenge in portable systems design .

The need for low power design is also becoming a major issue in high performance digital systems, such as microprocessors, digital signal processors (DSPs) and other application . The common traits of high performance chips are the high integration density and the high clock frequency . The power dissipation of the chip , and thus , the temperature , increases with the increasing clock frequency . since, the dissipated heat must be removed effectively to keep the chip temperature at an acceptable level the cost of packaging cooling and heat removal becomes a significant factor in circuit . several high-performance microprocessor chip designed in the early 1990s (e.g. intel-Pentium , DEC alpha and power PC) operated at clock frequencies in the range of 100 to 300 MHz and their typical power consumption was between 20 and 50 W. modern microprocessors are running at clock frequencies above 1 GHz with 100 W power dissipation.

VLSI reliability is yet another concern which points to the need for low power design .there is a close correlation between the peak power dissipation of digital circuits and reliability problems such as electromigration and hot-carrier induced device degradation . also,the thermal stress caused by heat dissipation on chip is a major reliability concern .Consequently the reduction of power consumption is also crucial for reliability enhancement.

The methodologies which are used to achieve low power consumption in digital system span a ,from wide range device/process level to algorithm level.Device characteristics(or threshold voltage),device geometries or interconnect properties are the proper design styles, reduction of voltage swing and clocking strategies be used to reduce the power dissipation at the transistor- level,.Architecture –level measure include smart power management of various system blocks, utilization of pipelining and parallism , and design of bus

structures. Finallypower consumed by system can be reduced by a proper selection of data processing algorithm, specifically to reduce no. of switching event in given task.

2.1 Programmable Embedded Controller Architecture

Architecture of PEC is shown in Figure.1. Various blocks in the architecture are register fileALU, RAM, ROM, UART, I/O Ports, BCD to 7 segment driver , Control unit, and clocker,designed to perform particular task. Register File is a set of registers that are modeled as RAMof 8 bit words, used to store intermediate values during instruction processing. The ALUperforms 8 bit operations. The Read Only Memory (ROM) is 256 bytes with 8 bit wordlength and is used to store the instruction data. The Random Access Memory (RAM) 1K×8 isused to store temporary data. Port 0 and Port 1 are two ports which are

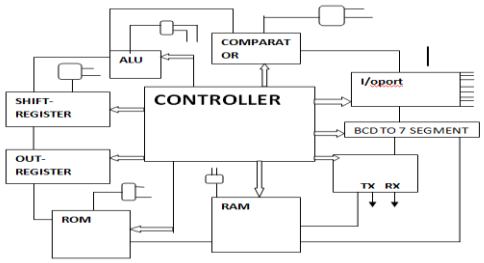


Fig. 1 Block Diagram Of Pm5g

configuredas output andinput ports respectively ..A display driver for BCD to 7 segment display is designed to drive the 7 segment display unit.

The control unit generates various control signals to all other blocks to execute desired taskspecified by the instructions. The PEC is initiated by the reset signal whenever reset signalasserts high, the controller generate appropriate signals to load the PC address of the ROM. Theexternal interrupt mechanism activates on any hardware interrupt or reset signal arriving at thecontroller when it is in idle mode.

2.3. On-Chip Clocking Mechanism

The frequency of the application specific hardwired oscillator shown in Figure isprogrammable by means of the 4-bit number (control word value) contained in the dedicatedregister r_osc. On-chip clocking is used to obtain different frequencies ranging from 44MHz to1GHZ by changing the control word values as shown in Figure.

2.4Intelligent Clock Gating

I have used ICG to reduce the power of fully programmable embedded controller .In this method I have provided an intelligent input externally ,so that when we give input op-code to functional unit this intelligent input signal compares with input op-code if both op-code matches with each other then clock is gated if it does not matches than clock is not gated.

2.2Reducing switching power with intelligent clock gating

Clock gating is a well-understood power optimization technique employed in both ASIC and FPGA designs to eliminate unnecessary switching activity. ICGusually requires that the designers add a small amount of logic to their RTL code to disable or deselect unnecessarily active sequential elements register**.**

Figure.(a) shows the schematic of latch element. A significant amount of power is consumedduring charge/discharge cycle of the cumulative gate capacitance Cg of the latch, when the clockfed directly and there is no change in the clock cycle. Figure(b) shows the latch withgated clock. By gating the clock charge/discharge of Cg can be effected only whenthere is change in the clock cycle thus saving power

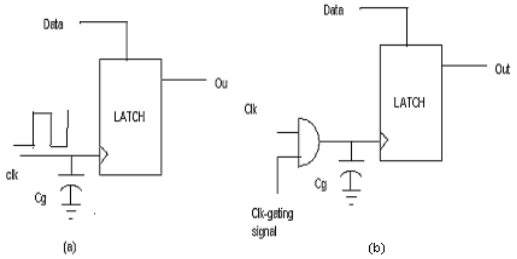


Fig2 Schematic of Latch Element (a) without clock gating (b) with clock gating

The controller shown in Figure.1 supports predefined smart instruction set having length of 16bits each. Gated clock signal generated by the control unit allows the clock to be fed only tothe active blocks and not to the unused blocks.

2.5Reducing switching power with intelligent clock gating

Clock gating is a well-understood power optimization technique employed in both ASIC and FPGA designs to eliminate unnecessary switching activity. This method usually requires that the designers add a small amount of logic to their RTL code to disable or deselect unnecessarily active sequential elements registers, .

Despite the obvious value of reduced dynamic power afforded by this method, the designer faces significant challenges when attempting to perform these optimizations manually.

Truly reducing activity in the design requires intimate knowledge of the design itself and typically requires numerous changes to the RTL.

Most ASIC and FPGA designs today comprise some combination of new, legacy, and third-party IP circuit designs, but typically only the new designs are candidates for clock-gating optimizations. Designers rarely if ever attempt these optimizations on legacy and IP design. They usually do not have sufficient depth of knowledge about the design and operation of the legacy RTL code, and it requires too much time to manually develop meaningful clock-gating optimizations.

Applying clock-gating optimizations usually requires the addition of more tools and more steps to the design flow and can precipitate the creation of an intricate set of new clocks requiring complex timing analyses (as is often the case for ASIC optimization). Unless the gains in power efficiency are sufficient and essential to the success of the design, the additional complexity and time can be prohibitive and add risk.

With the release of ISE Design Suite v12, Xilinx has introduced an automated capability linked to the place-and-route portion of the standard FPGA design flow that uses a set of innovative algorithms to perform an analysis on all portions of the design (including legacy and third-party IP blocks). Having analyzed the logic equations to detect sourcing registers that do not contribute to the result for each clock cycle, the software utilizes the abundant supply of clock enables (CEs) available in the logic of Virtex-6 and Spartan-6 FPGAs to create fine-grain clock-gating or logic-gating signals that neutralize superfluous switching activity, as shown in figure 1.

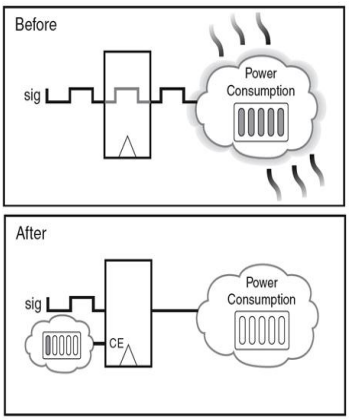


Fig 3: Intelligent clock gating dramatically reduces switching power consumption.

Each CE is ideally suited for power optimization because it connects to the basic cluster of the FPGA logic (the slice). It controls a small number of registers (only eight), see figure 2, providing the level of granularity that matches the minimum size of buses used by the vast majority of designs. The smallest member of the Virtex-6 FPGA family (the XC6VLX75T) offers more than 10,000 CEs, while the largest (the XC6VLX760) offers more than 100,000.

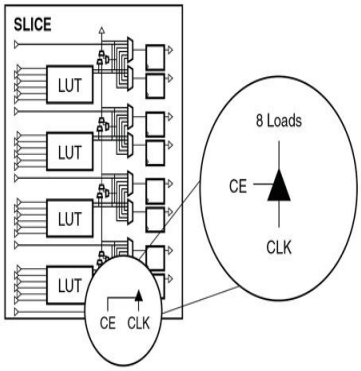


Fig 4 Clock Enables in the Virtex-6 FPGA slice.

It is important to note that these optimizations do not alter the pre-existing logic or clock placement, nor do they create new clocks. The resulting design is logically equivalent to the original and the additional logic created is separate from previous logic, adding only 2 percent more LUTs (on average) to the original design. As a result, the optimization does not affect timing in the vast majority of cases because it does not add levels of logic to the original logic paths.

2.6 Controlunit

The control unit provides all of control signals to regulate the data traffic and necessary signalsto perform the desired functions. The control unit architecture contain a state machine thatcauses all appropriate signal values to update based on current state and input signals andproduce a next state for state machine. The control unit performs two processes. The first is acombinational process (not clocked) that examines the current state and all inputs and producesoutput control signals and next state output. The second is the sequential process (having aclock) that is used to store the current state and copy of the next state to the current state.Figure.5 Signals of Control Unit

If the reset signal is high the sequential process set the current state value to reset1, the firststate of the reset sequence. The logic for clock gating is implemented within the control unit.The controller generate appropriate clock gating signal to reduce power consumption of thechip. When the control unit decodes the opcode of the instruction, the control unit generatescontrol signals as shown in Figure.5, to execute theinstruction.By implementing the instructions given in the instruction set (Table 1) does not cause anyfunctional limitation, but enables an effective way of power saving through generation of gatedclock signals. All the instructions are of length 2 bytes and of direct addressing mode type.nstruction set includes Load, Store, Branch, ALU and Shift instructions.

2.7 Table-1 Instruction Set

00000	NOP	NO OPERATION
00001	LOAD	LOAD REGISTER
00010	STORE	STORE THE REGISTER
00011	MOVE	MOVE VALUE INTO THE REGISTER
00100	LOADI	LOAD REGISTER WITH IMMEDIATE VALUE
00101	BI	BRANCH TO IMMEDIATE ADDRESS
00110	BGTI	BRANCH GREATER THAN TO IMMEDIATE ADDRESS
00111	INC	INCREMENT
01000	DEC	DECREMENT
01001	AND	LOGICAL AND TWO REGISTER
01010	OR	LOGICAL OR TWO REGISTER
01011	XOR	LOGICAL XOR TWO REGISTER
01100	NOT	LOGICAL NOT THE REGISTER
01101	ADD	ADD TWO REGISTER

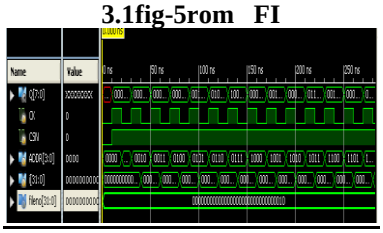
01110	SUB	SBTRACT TWO REGISTER
01111	ZERO	ZERO A REGISTER
10000	PORT0	PORT 0 WRITE
10001	BLT	BRANCH LESSTHAN
10010	BNEQ	BRANCH NOT EQUAL
10011	PORT1	PORT 1 READ
10100	BGT	BRANCH GREATER THAN
10110	BCH	BRANCH ALL THE TIME
10111	BEQ	BRANCH IF EQUAL
11000	B7S	7 SEGMENT DRIVER
11001	BLTE	BRANCH LESS THAN OR EQUAL
11010	SHL	SHIFT LEFT
11011	SHR	SHIFT RIGHT
11100	ROR	ROTATE RIGHT
11101	ROL	ROTATE LEFT
11110	UARTS	UART SEL

2.8Table-2 simulation result

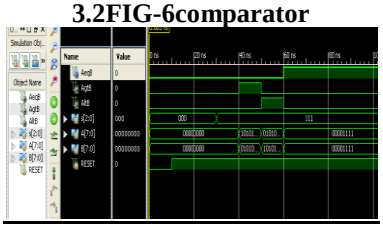
Synthesis Results for	controlunit	Ram	Rom	Alu	comparator	Out reg.	uart	Shift reg.	transmittr	receiver
Number of logic	25	170	170	52	16	-	25	52	35	35
Number of i/o	25	27	27	29	20	19	25	29	21	21
Number of signals	25	435	435	71	29	11	25	71	59	59
Device family	Spartan3a	Spartan3a	Spartan3a	Spartan3a	Spartsn3a	Spartan3a	Spartan3a	Spartan3a	Spartan3a	Spatan3s
Speed grade	4	4	4	4	4	4	4	4	4	4
Dynamic power	0	.007	.003	.0004	.003	.oo2	0	.004	.002	0
Quiescent power	.034	.032	.032	.032	.032	.032	.034	.032	.032	.034
Time Delay	14.195ns	14.195 ns		14.195ns	14.195ns	14.195ns	14.195ns	14.195ns	14.195ns	14.195ns

II. Simulation Waveform

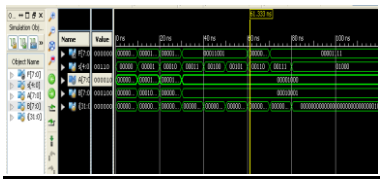
3.1fig-5rom FI



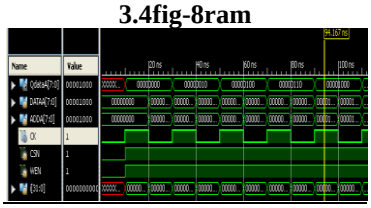
3.2FIG-6comparator



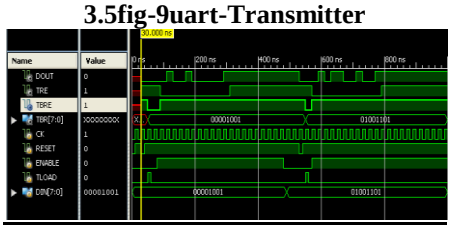
3.3fig-7alu



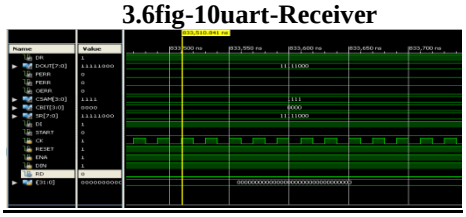
3.4fig-8ram



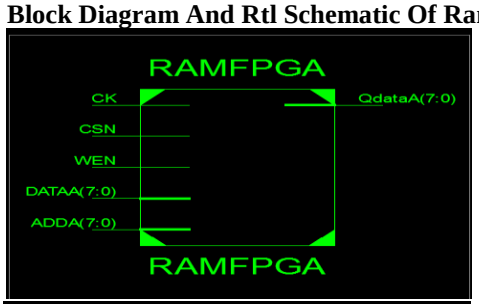
3.5fig-9uart-Transmitter

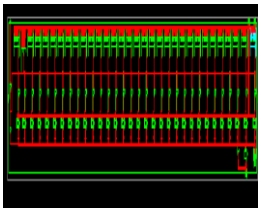


3.6fig-10uart-Receiver

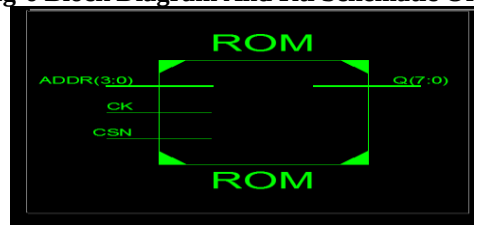


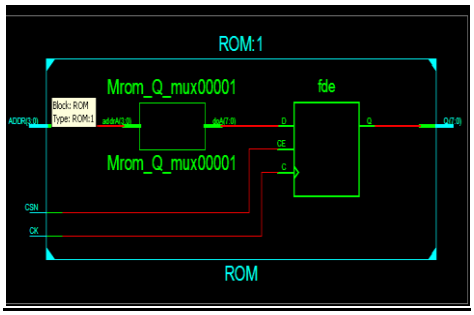
4.IFig-5 Block Diagram And Rtl Schematic Of Ram Fpga



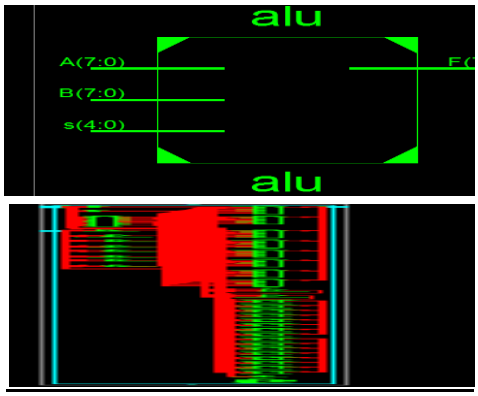


4.2Fig-6 Block Diagram And Rtl Schematic Of Rom

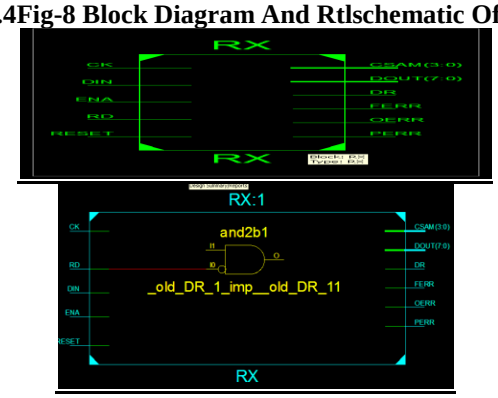




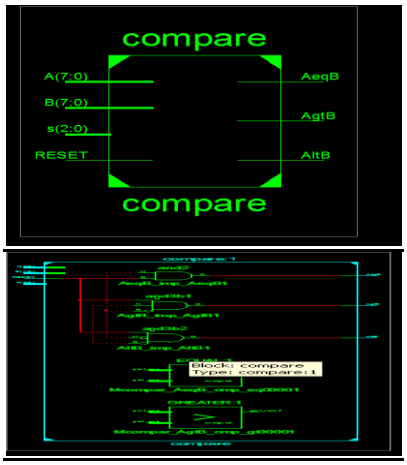
4.3Fig-7 Block Diagram And Rtl Schematic Of Alu



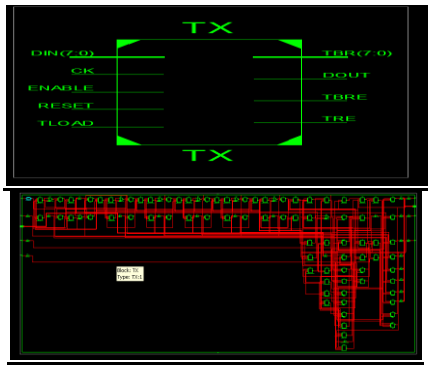
4.4Fig-8 Block Diagram And Rtlschematic Ofrx



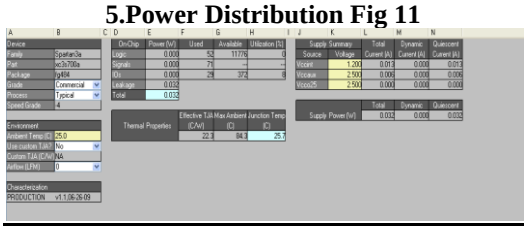
4.5Fig-9 Block Diagram And Rtl Schematic Of Comparator



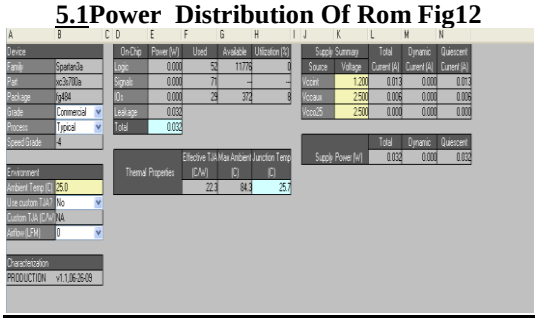
4.7 Fig-10 Block Diagram And Rtl Schematic Of Tx



5.Power Distribution Fig 11

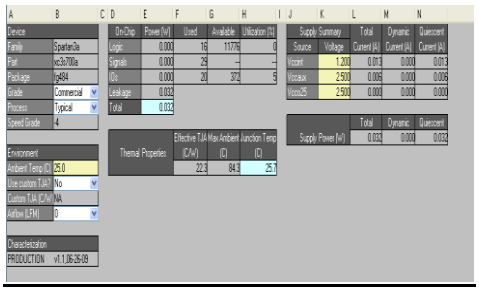


5.1Power Distribution Of Rom Fig12

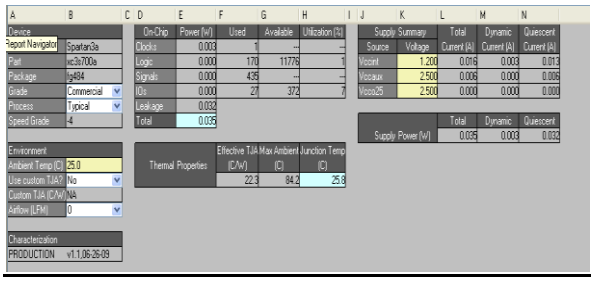


5.2power Distribution OfAlu Fig13

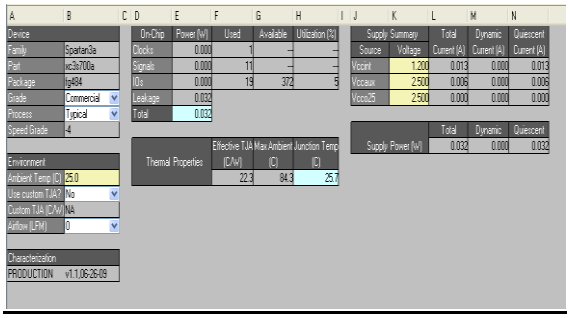
5.3power Distribution Of Shift Rgister Fig14



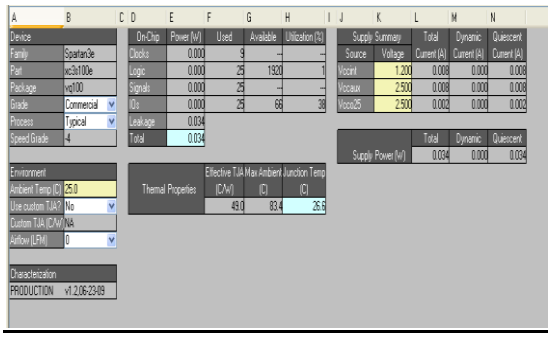
5.4 Power Distribution Of Comparator Fig 15



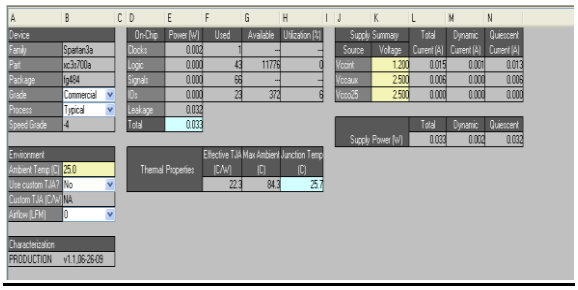
5.5 Power Distribution Of Ram Fpga Fig1 6



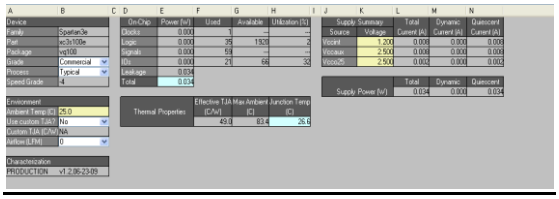
5.6 Power Distribution Of Out Register Fig17



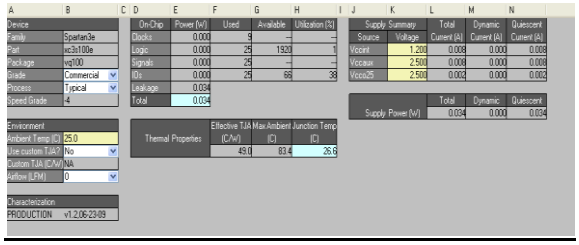
5.7 Power Distribution OfUart Fig 18



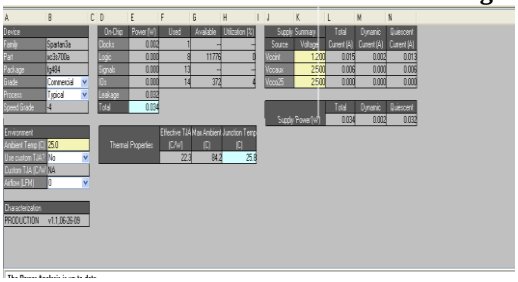
5.8power Distribution Of Transmitter Fig19



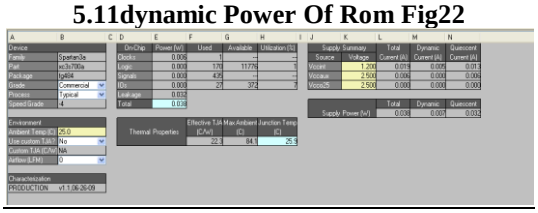
5.9power Distribution Of Receiver Fig20



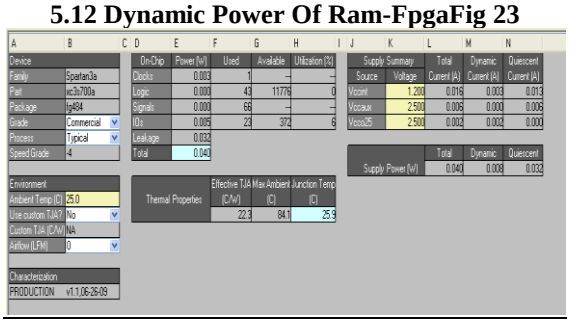
5.10 Power Distribution Of Control Unit Fig 21



5.11dynamic Power Of Rom Fig22



5.12 Dynamic Power Of Ram-FpgaFig 23



III. Power Analysis

The estimation of power consumption of each module is done using Xilinx Xpower's tool. Thegraphical representation of power consumed in various modules.

Power Analysis

Total power csumption is estimated to be 6mW without clock gating and only 2.5 mWafter clock gating technique is employed, thus achieving a power saving of 57%Comparison of Power Consumed without and with Clock Gating

6.1dynamic Power OfTransmiter

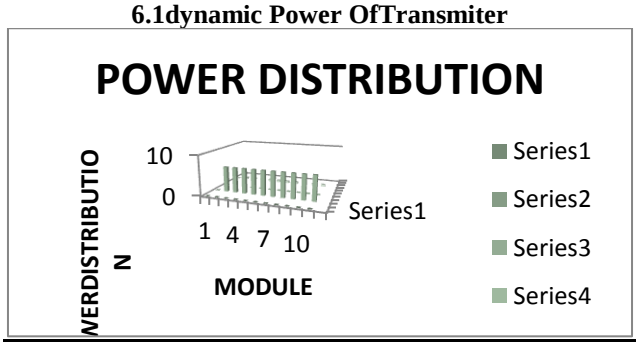


Fig24

Fig 25 Fig.6.2 Power Optimization Graph

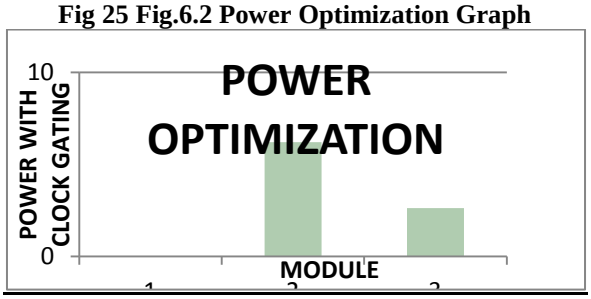


Fig 26

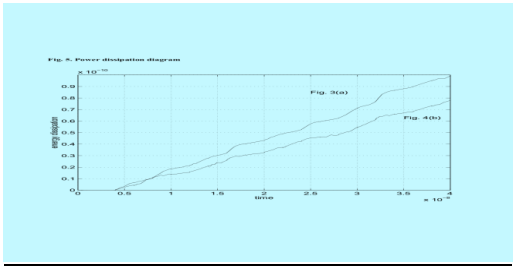


Fig.6.3graph OfwithAnd Without Clock Gating

7.1future Aspect:

To design 8 bit ec with additional csrcuitry like interrupt ckt. Increasedram ,rom capacity etc. and to reducethe power ,energy and sres of chip by utilizing intelligent clock gating efficiency.

IV. Result

Architecture reduces 59.4% of total power consumed by chipCHARACTERSTIC OF CHIP

The characterstics of designed chip are

Architecture	RISC
OPTIMIZATION	POWER
ROM	256bytes
RAM	1KB
INSTRUCTION	2 BYTES
ALU	8Bbit
POWERSUPPLY	2.4V
POWER DISSIPATION	57%
Operating frequency	1GHZ

V. Conclusion

The need for low power systems is being driven by many market segments. There are severalapproaches to reducing the power. In this work clock gating technique is applied to optimize thepower of fully programmable embedded controller employing RISC architecture. The wholedesign is captured using VERILOGHDLlanguage and is implemented on FPGA chip using Xilinx .The chip has less hardware complexity as this works based on single addressing mode to access thedata for processing. The architecture and clock gating technique together have reduced thepower consumption by 59.4% of total power consumed by the chip. This clock gatingtechnique can be applied from chip level to module and then eventually to system

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