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Low Power Technology for Power Reduction in Sram Using Read Stability with Reduced Transistor Count for Future Caches

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ABSTRACT: *This Paper presented Read and write assist techniques are now commonly used to lower the minimum operating voltage (V_{min}) of an SRAM. The minimum supply voltage for SRAM cell is limited by write failures (write-ability) or read disturbs failures (cell stability). In the previous work, various SRAM cells are discussed which offer better variability resilience compared to the SRAM 6T cell. SRAM 6T cell functionality is highly dependent on the supply voltage. The voltage optimization can impact the write failures and the read disturb failures significantly. Here we proposed a, dynamic voltage optimization techniques, for realizing low V_{DD} operation with the conventional SRAM 6T cell while maintaining sufficient READ/WRITE margins. Lowering an SRAM cell voltage V_{dd} level reduces the current to the pull-up P_{mos} device. As a result, this assists an SRAM's write operation with better stability.*

Keywords—*Low-voltage, Process variation tolerance, Read/Write failure techniques, Schmitt trigger, SRAM.*

I. INTRODUCTION

Portable electronics devices have extremely low power to achieve the long battery life time. Various device-/circuit-/architectural-level techniques have been imple- mented to minimize the power consumption [1]. Supply voltage scaling has significant impact on the overall power dissipation. With the supply voltage reduction, the dynamic power reduces quadratically while the leakage power reduces linearly (to the first order) [1]. However, as the supply voltage is reduced, the sensitivity of circuit parameters to process variations increases. This limits the circuit operation in the low-voltage regime, particularly for SRAM bitcells employing minimum-sized transistors [2]. These minimum geometry transistors are vulnerable to interdie as well as intradie process variations. Intradie process variations include random dopant fluctuation (RDF) and line edge roughness (LER). This may result in the threshold voltage mismatch between the adjacent transistors in a memory bitcell, resulting in asymmetrical characteristics [4]. The combined effect of the lower supply voltage along with the increased process variations may lead to increased memory failures such as read-failure, hold-failure, write-failure, and access-time failure [4]. Moreover, it is predicted that embedded cache memories, which are expected to occupy a significant portion of the total die area, will be more prone to failures with scaling [2].

II. PREVIOUS SRAM BITCELL

Existing technique analyze Schmitt-Trigger (ST)-based differential-sensing static random access memory (SRAM) bitcells for ultralow-voltage operation. The ST-based SRAM bitcells address the fundamental conflicting design requirement of the read versus write operation of a conventional 6T bitcell. The ST operation gives better read-stability as well as better write-ability compared to the standard 6T bitcell. The proposed ST bitcells incorporate a built-in feedback mechanism, achieving process variation tolerance a must for future nano-scaled technology nodes. A detailed comparison of different bitcells under iso-area condition shows that the ST-2 bitcell can operate at lower supply voltages. Measurement results on ten test-chips fabricated in 130-nm CMOS technology show that the proposed ST-2 bitcell gives 1.6 higher read static noise margin, 2 higher write-trip-point and 120-mV lower read Vmin compared to the iso-area 6T bitcell.

For the input transition, the feedback mechanism is not present. This results in smooth transfer characteristics that are essential for easy write operation. Thus, input-dependent transfer characteristics of the Schmitt trigger improves both read-stability as well as write-ability of the SRAM bitcell. Two novel bitcell designs are proposed. The first ST-based SRAM bitcell has been presented in our earlier work . Another ST-based SRAM bitcell which further improves the bitcell stability. To maintain the clarity of the discussion, the ST bitcell is termed the "ST-1" bitcell while the other ST bitcell is termed the "ST-2" bitcell.

2.1 ST-1 Bitcell

Fig. 2.1 shows the schematics of the ST-1 bitcell. The ST-1 bitcell utilizes differential sensing with ten transistors, one word-line (WL), and two bitlines (BL/BR). Transistors PL-NL1-NL2-NFL form one ST inverter while PR-NR1-NR2-NFR form another ST inverter. Feedback transistors NFL/NFR raise the switching threshold of the inverter during the input transition giving the ST action. Detailed operation of the ST-1 bitcell can be found in [10].

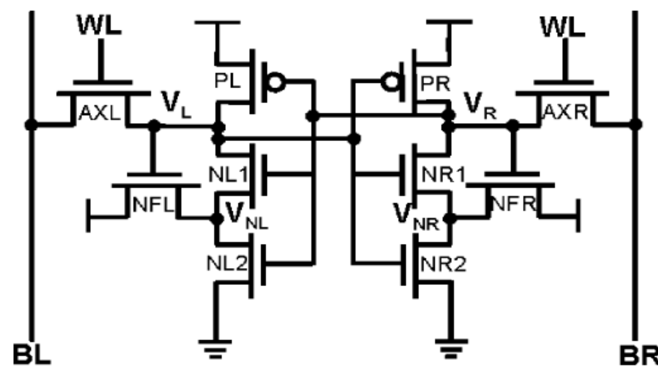

Fig 2.1 ST-1 bitcell schematics

2.2 ST-2 BITCELL

Fig. 2.2 shows the schematics of the ST-2 bitcell utilizing differential sensing with ten transistors, two word-lines (WL/WWL), and two bitlines (BL/BR). The WL signal is asserted during read as well as the write operation, while WWL signal is asserted during the write operation.

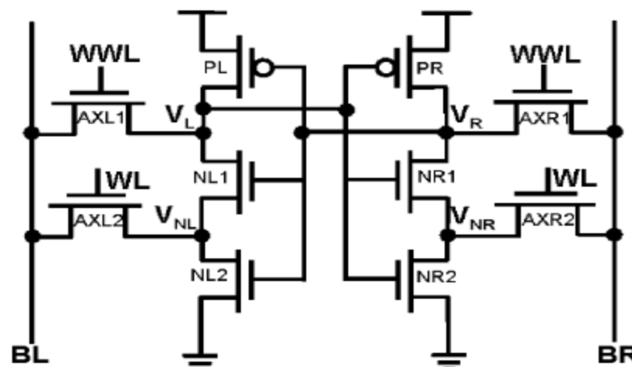

Fig 2.2 ST-2 bitcell schematics

During the hold-mode, both WL and WWL are OFF. In the ST-2 bitcell, feedback is provided by separate control signal (WL) unlike the ST-1 bitcell, where in feedback is provided by the internal nodes. In the ST-1 bitcell, the feedback mechanism is effective as long as the storage node voltages are maintained. Once the storage nodes start transitioning from one state to another state, the feedback mechanism is lost. To improve the feedback mechanism, separate control signal WL is employed for achieving stronger feedback. Detailed operation of the ST-2 bitcell is explained in our earlier work [5].

III. TECHNIQUE USED TO OVERCOME THE FAILURE

The effectiveness of an SRAM write operation is typically quantified by the minimum (or critical) width of word-line pulse during which the bit cell changes state. The definition is important because it captures the dynamic write margin which is more accurate. The static approaches to measure the write margin assume that the word line pulse width is infinite which could lead to erroneous conclusions. Figure 1 shows how the internal nodes (n1 and n2) of a bit cell change when word-line of different pulse widths are applied during the write operation. The pulse width of WL is smaller than the WL crit. The pulse width of WL is equal to or greater than WL crit. The nodes n1 and n2 tend to move towards the other state but they return back to the

original state. However, the nodes n1 and n2 are able to move to other stable state. In other words, to have a successful write, WL(WL crit). Write operation in a bi-stable cell (like a bit cell) can be defined as a transition from one equilibrium state to the other. Write operation in a bi-stable cell (like a bit cell) can be defined as a transition from one equilibrium state to the other.

The separatrix is defined as the boundary which separates the two stability regions. The importance of the separatrix lies in that a state will be generated if and only if the write operation causes the state to be pushed away from the initial stable equilibrium to cross the separatrix. The state space trajectory during the write operation with two different word-line pulse widths. The separatrix in this case is a straight line since the cell is symmetrical. The curve in solid is for the case when the WL pulse width equals. In this case the trajectory starts at the stable point of ((n1; n2) = (1; 0)) and ends back at the same stable point. The dotted line represents the case where the WL pulse width is equal to WL crit. In this case the trajectory starts at ((n1; n2) = (1; 0)), crosses the separatrix and then ends up at ((n1; n2) = (0; 1)), thus successfully completing the write operation.

3.1 WRITE ASSISTS TECHNIQUES

Write-assist (WA) techniques are crucial in reducing the Vmin of SRAMs. In essence, WA techniques aid the bit cell to state during the write operation. The increase in WLcrit is exponential as the supply voltage scales down. To improve the scaling of WLcrit, several WA techniques have been proposed in literature:

3.1.1 V_{dd} lowering WA
3.1.2 V_{ss} raising WA
3.1.3 Word-line boosting WA
3.1.4 Negative bit-line WA

***3.1.1* V_{dd} Lowering**

WL can be reduced by weakening the pull-up device with respect to the pass-gate device. Once the pull-up device is weakened, it is easier to write a new data to the bit cell. The timing relationships using the Vdd lowering WA scheme. This WA scheme is implemented using a second external lower supply which is connected via a multiplexer to the write-selected columns. On-chip regulators can also be used to generate the lower supply voltage during write. Some other techniques to lower the core Vdd voltage include floating the selected write columns charge sharing between the selected column and an appropriately sized predischarged dummy capacitance to create the lower voltage level etc. The main challenge with this technique is to make sure that the lowered column voltage is still higher than the retention voltage of the unselected bit cells in the same column.

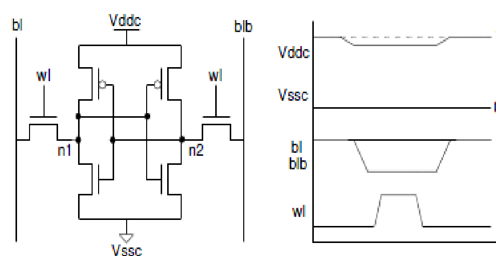

Fig 3.1.1 Write-Assist Based On Lowering Of Core V_{dd}

To simplify the implementation, sometime the voltage supply of the whole array is lowered during the write operation. However, this decreases the dynamic read noise margin (DRNM) of the half-selected bit cells. The impact of the Vdd lowering based WA on the WLcrit for a 32nm bit cell. Although the WA based scheme consistently performs better than the nominal case, the gain is minuscule. This is due to the fact that the pull-up PMOS is already very weak in current generation bit cells and hence making it further weak does not help much.

***3.1.*2 V_{ss} Raising**

A raised ground scheme is another way to aid the write operation thus decreasing the value of WLcrit. This WA technique reduces the risk of data retention failure. The idea is still to weaken the pull-up PMOS but in

this scheme it is done by weakening the PMOS gate voltage instead of the source voltage. The core ground is raised during the write operation. This extra ground voltage can be routed as a separate ground or can be generated internally using a regulator. This WA technique also impacts the DRNM of half-selected bit cells, if implemented globally for the whole array. Figure 4.3 shows the impact of the Vss raising based WA on the WL crit. The WL crit for the WA case is better than the non WA case but the gain is very small.

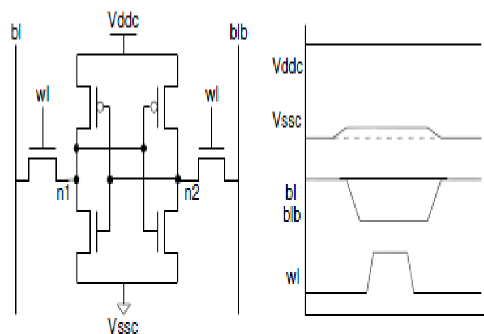

Fig 3.1.2 Write-Assist Based On Raising Of Core V_{ss}

The reason for this marginal increase is similar to that of the Vdd lowering WA case which is that the PMOS is already weak and hence weakening the gate drive does not further weaken it.

3.1.3 Word-Line Boosting

Another technique which assists the bit cell to flip during a write event is boosting the word-line higher than the supply voltage (Figure 3.1.3). The boosting increases the Vgs of the access transistor and hence increases its drive strength. The increased drive strength of the access transistor aids significantly in flipping the bit cell. The boost voltage can be routed as a separate power supply or it can be generated internally by a charge pump or by capacitive coupling. Unlike the techniques mentioned in Sections II and III which work on a column, the word-line boosting technique works on a row.

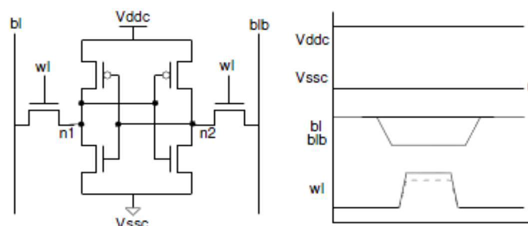

Fig 3.1.3 Write-Assist Based On Word-Line Boosting

Hence all the half-selected cells in a row are more prone to an upset due to reduction in their dynamic read noise margins. Figure 4.3.3 shows the impact of word-line boosting based WA on the WLcrit. The WLcrit in this case is substantially better than the nominal case with no WA. The benefits of this WA scheme increases significantly as the supply voltage is scaled down.

3.1.4 Negative Bit-Line

To create a larger Vgs for the NMOS pass transistor, either the gate voltage needs to be increased (Section III-C) or the source voltage needs to be decreased. The approach of negative bit-line based WA swings the bit-line voltage below 0. during the write operation. The increase in Vgs causes the access transistor to become stronger and hence can flip the bit cell easily. Similar to the word-line boosting, the negative bit-line voltage can be generated internally using a charge pump technique or using a capacitive coupling technique. This WA technique works on a column, hence all the unaccessed bit cells in the column see an increase in Vgs on the pass transistor. Since the word-lines are not asserted for those cells, The bene_ts due to the negative bit-

line WA are very similar to that of the word-line boosting WA scheme. The reason being that both techniques ultimately increase the Vgs of the access transistor. The bene_ts of this WA scheme increases as well when the supply voltage is scaled down.

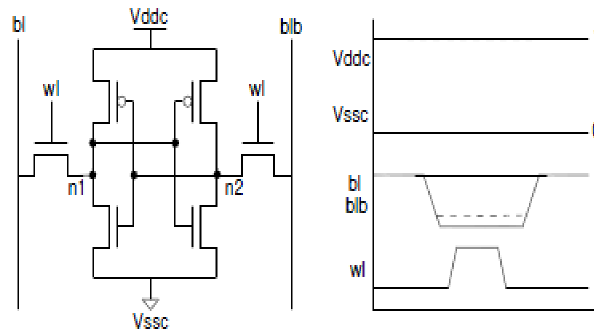

Fig 3.1.4 Write-Assist Based On Negative Bit-Line

3.2 READ ASSIST TECHNIQUES

Three leading read assist techniques are applied in ST-2 SRAM bit cells. These techniques help to overcome read failure in ST-2 bit cells and provide better read stability. Read failure occurs in bit cell when the enough charge on the bit line is transferred to the internal storage nodes and flip it states during read operation. Two ways to achieve read stability in ST-2 with help of read assist techniques.

The first is to improve the cross coupled inverter pair stability, by raising the core V_{dd} and reducing the V_{ss} in ST-2 SRAM bit cell during read operation. The advantage of reducing the V_{ss} is to significantly reduce the read delay due to strengthening both pull down and pass gate transistors.

The second goal is to increase the read stability in ST-2, pull down transistor should be stronger than pass gate transistor.

The proposed read assist techniques in this paper:

- Raising global V_{dd} at cell,
- Negative V_{ss} at cell,
- Word line drooping.

3.3 NOISE MARGIN REDUCTION TECHNIQUE

In electronic engineering, noise margin is the amount by which a signal exceeds the minimum amount for proper operation. It is commonly used in at least two contexts:

- In communications system engineering, noise margin is the ratio by which the signal exceeds the minimum acceptable amount. It is normally measured in decibels.
- In a digital circuit, the noise margin is the amount by which the signal exceeds the threshold for a proper '0' or '1'. For example, a digital circuit might be designed to swing between 0.0 and 1.2 volts, with anything below 0.2 volts considered a '0', and anything above 1.0 volts considered a '1'. Then the noise margin for a '0' would be the amount that a signal is below 0.2 volts, and the noise margin for a '1' would be the amount by which a signal exceeds 1.0 volt. In this case noise margins are measured as an absolute voltage, not a ratio. Noise margins for CMOS chips is usually much greater than TTL because the $V_{OH\ min}$ is closer to the power supply voltage and $V_{OL\ max}$ is closer to zero.

In simple words, Noise margin (in circuits) is the amount of noise that a circuit can withstand. Noise margins are generally defined so that positive values ensure proper operation, and negative margins result in compromised operation, or perhaps outright failure.

IV. SIMULATION METHOLOGY

The simulation of work is conducted in H-Spice and following result with different technique is obtained which is given below

4.1 RESULT FOR WRITE ASSIST TECHNIQUE

To improve the write ability and read stability is performed by some technique. In that Vss play an important role in the write ability and read stability work. To achieve the write ability and read stability by using increase the vss may decrease the write failure. And by using Verilog code the output receive by model simulation.

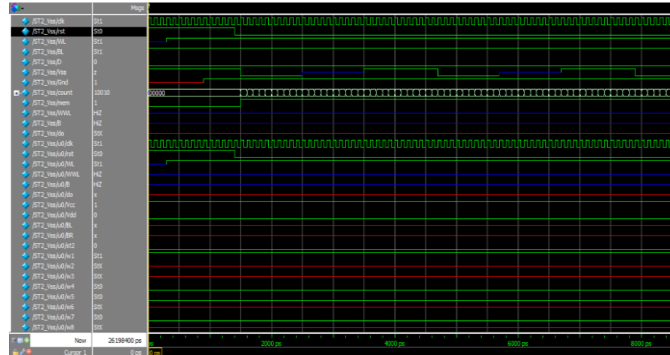

Fig 4.1 Write Assist Technique

4.2 RESULT FOR READ ASSIST TECHNIQUE

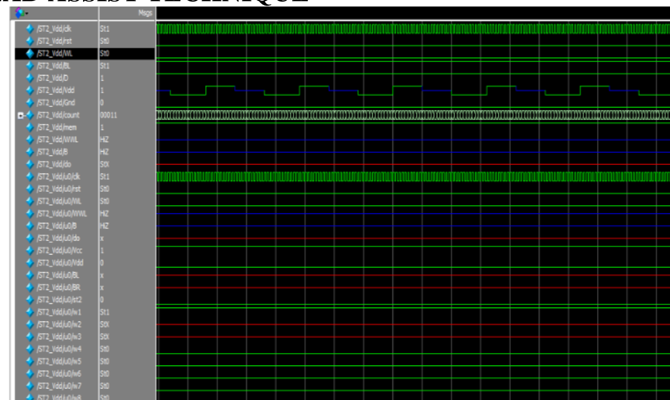

Fig 4.2 Read Assist Technique

To improve the read stability is performed by reducing V_{dd} technique. In that V_{dd} play an important role in the read stability work. To achieve the read stability by using decrease the V_{dd} which cause reduction of read failure. And by using Verilog code the output receive by model simulation.

4.3 OUTPUT OF FAILURE ELIMINATED SRAM

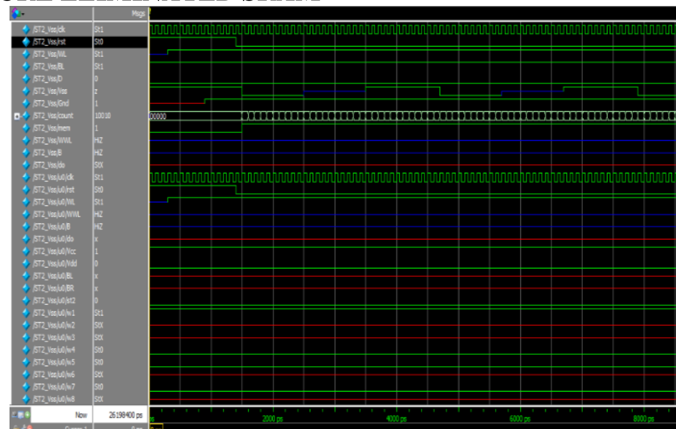

Fig 4.3 Eliminated SRAM Output

By using the techniques, The failure are detected from the array of SRAM. And also the cache miss is reduced by the verilog coding for CM algorithm. And this technique used in the future cache and achieve speed optimization.

V. CONCLUSION

As the technology scales in deep nanometer era, the challenges in designing an SRAM increase substantially. The challenges arise due to increase in write, read, access and retention failures. It is now becoming common for SRAMs to have read and write assist techniques to enable robust operation at lower supply voltages. In this work, we reviewed the efficiency of four leading write-assist (WA) techniques across the operating range of supply voltages in ST based SRAM cells. Our analysis suggests that the word line boosting and negative bit-line WA techniques seem most promising at lower supply voltages. These two techniques help reduce the value of WLcrit by a factor of 2.5X at 0.7V and also significantly reduce the impact of process variations. Also, most of the WA techniques degrade the dynamic read noise margin (DRNM) of the SRAM cells by 10-15%. Understanding these trade-offs and the overhead in terms of area and performance are crucial to choose the best write-assist technique in nanoscale SRAMs to enable robust low voltage operation.

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