IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
ISSN: 2319 – 4200, ISBN No. : 2319 – 4197 Volume 1, Issue 1 (Sep-Oct. 2012), PP 46-50
www.iosrjournals.org

CMOS Body Driven Quaternary Logic Generator

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Abstract— *This paper is about the design, simulation and study of a CMOS quaternary logic generator having a single stage CMOS body driven design. The interest of design is that the circuit consists of only one CMOS circuit, reducing the chip area and also only two supply rails is required to drive the complete circuitry. The multi-valued logic generator, designed here is also demonstrated with and without enable circuitry too. The design has been implemented with 1.8micrometer CMOS technology on Cadence virtuoso schematic Editor.*
Keywords — *CMOS, body effect, decoder, multi-valued logic.*

I. INTRODUCTION

In logic a multi-valued logic [7] is a propositional calculus in which there are more than two values. Traditionally, in Aristotle's [6] logical calculus, there are only two possible values (i.e. "true" and "false") for any proposition. Extension to classical Boolean logic is an n-valued logic for *n* greater than two e.g. three valued logic[8] of "true", "false" and "unknown" and for infinite valued "fuzzy logic"[11] and "probability logic"[12]. There have been many approaches to design multi-valued logic. Methods have also been implemented in voltage mode [14] and current mode [13] circuits. In previous works, the number of transistor use were more than two, which increases the chip area, also it has been seen that most of the approaches to design multi-valued requires more than two different supply rails which causes the use of more metal in the chip increasing the fabrication cost. This paper the is about the design of quaternary logic generator, based on body driven CMOS circuit where binary inputs can be decoded in quaternary logic. Since the module is using single CMOS stage the chip area is very less and also the number of supply rails required to drive the complete circuitry is two, which is a cost efficient design.

II. DESIGN AND SIMULATION

The design of body driven [4][5] quaternary logic generator is based on CMOS circuit[1] in which pMOS and nMOS are connected drain to drain and their gates are common and driven by a bias potential. The driving inputs are connected on the body (substrate) of pMOS and nMOS (fig. 1). These inputs are digital inputs with logical high as 1.8 volts and logical low as 0 volts. V_{dd} is 1.8 volt.

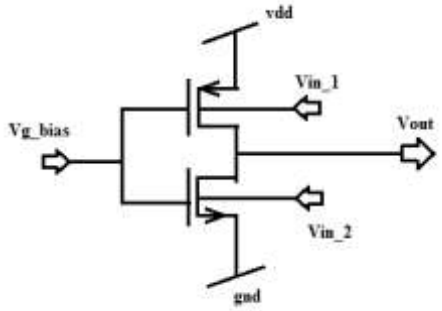

Fig. 1- Schematic of body driven quaternary logic generator

The simulation is executed on Cadence Virtuoso Schematic Editor *180nm* designed by CADENCE. Both the inputs Vin_1 and Vin_2 are applied with pulse inputs with one having double frequency than to the other input so as to generate all the logical combination of the inputs (fig. 2 and fig. 3).

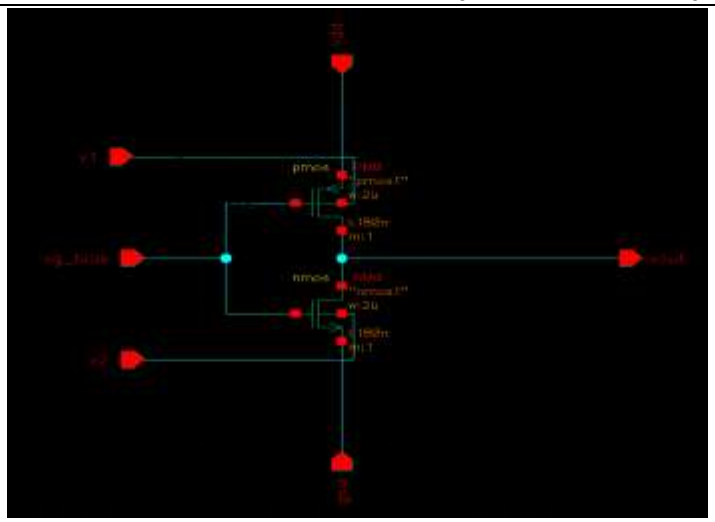

Fig. 2- Simulation of quaternary logic generator

The Vg_bias is gate bias potential to control the logical levels spacing in voltage domain. These spacing can be modulated by varying parametrically this bias potential. In special case to provide equal voltage spacing (approximately) in the logic levels, the potential is chosen 677 mV. The nMOS body input with logical high will be controlling the weak high and weak low output (fig. 3 and table-1). The layout of the design is also shown in fig_4.

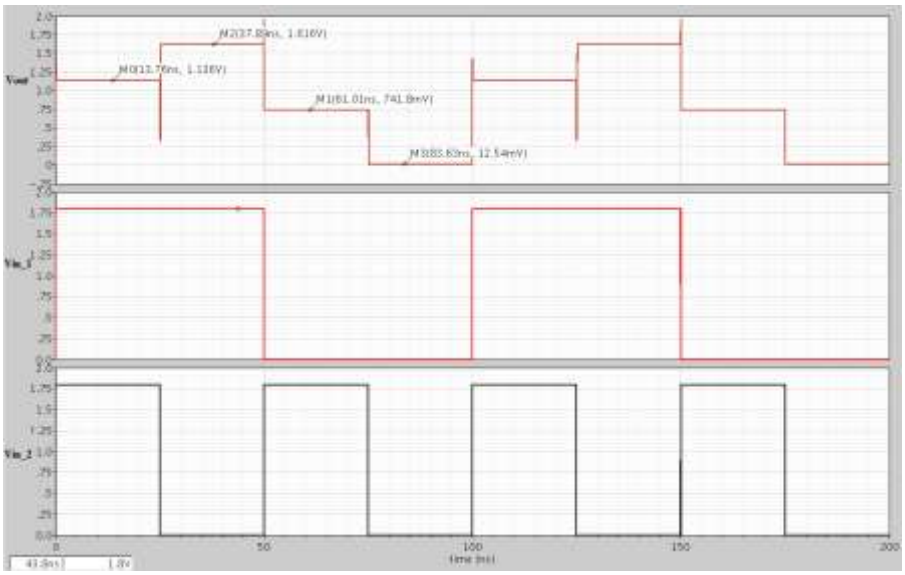

Fig. 3- Circuit response with Vin_1 for pMOS and Vin_2 nMOS inputs at their body

Table -1

nMOS body	**pMOS body**	**OUTPUT**
'**0**' **(0.0 V)**	'**0**'	Strong low '**0**'(0.0 V)
'**0**'	'**1**'	Strong high '**1**'(1.8 V)
'**1**'**(1.8 V)**	'**0**'	Weak low "**0'**"(741 mV)
'**1**'	'**1**'	Weak high "**1'**"(1.136 V)

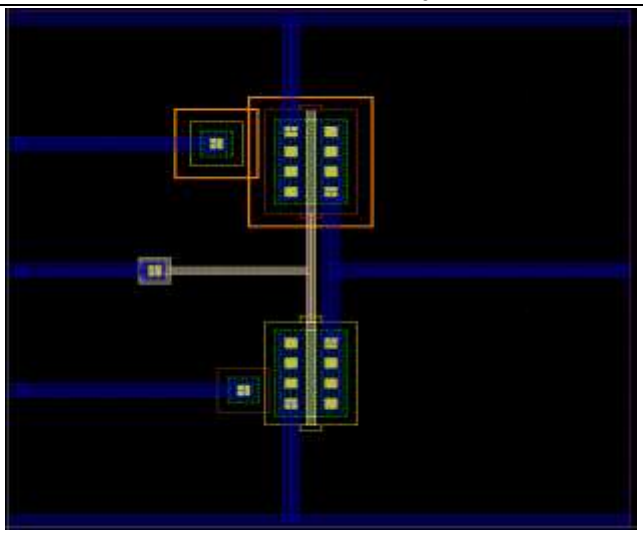

Fig.4- Layout of the module

III. WORKING OF THE MODULE

The module is producing four different and stable logical levels which is comes into possibility due to the MOSFET second order effect[2][3] i.e. body effect, which can be explained by equation (1).

$$V_T = V_{TO} + \gamma \{\sqrt{|V_{SB} + 2\emptyset|} - \sqrt{|2\emptyset|}\} \quad \ldots\ldots\ldots\ldots\ldots (1)$$

Where $\gamma = (t_{OX}/C_{ox})\sqrt{(2q\,\varepsilon_{si}\,N_A)}$ ……. ……(2)

Since four different combinations of threshold voltages are being configured (due to application of four different combinations of the two inputs at the substrate of pMOS and nMOS), there will be four different resistive path on applications of different inputs. Hence four different stable voltages will appear at the output terminal.

IV. DECODER WITH ENABLE INPUT

For introducing an enable input, a pMOS and nMOS are to be inserted between V_{dd} and source of the input pMOS and ground and the source of the input nMOS stages respectively. Their gates must be connected with and extra introduction of CMOS inverter and given to the enable input (fig. 5). When it is required to disable the module a logical high is given to the enable input else wise a zero. This is an active low enable structure. We can also design an active high enable structure shown in fig. 6.

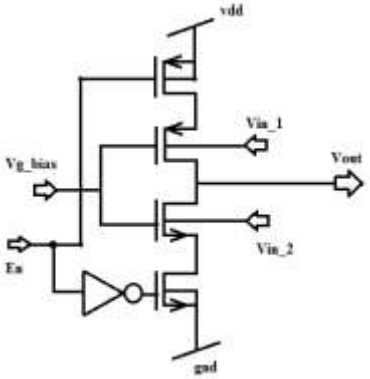

Fig. 5- Module with active-low enable input

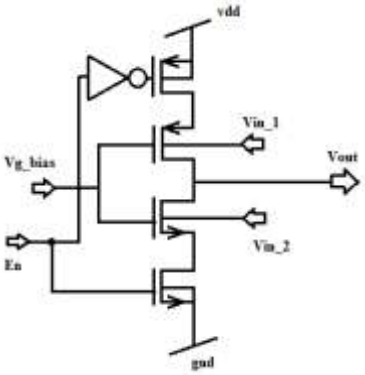

Fig. 6- Module with active-high enable input

V. ISSUES WITH THE DESIGN AND SOLUTIONS

The major drawback of the system is that the pMOS input stage constitutes a source to drain forward biased diode which provide a path for current to flow directly from V_{dd} to the logical input source at the body of pMOS. This current is very high in the order of tens of milliAmps to 500 mA (fig.-7). That is why the design is not much power efficient. To overcome the drawback the circuit input must be designed with high input impedance. One of the possible solutions to the problem is to use SOI technology [15] to reduce the body current in the pMOS.

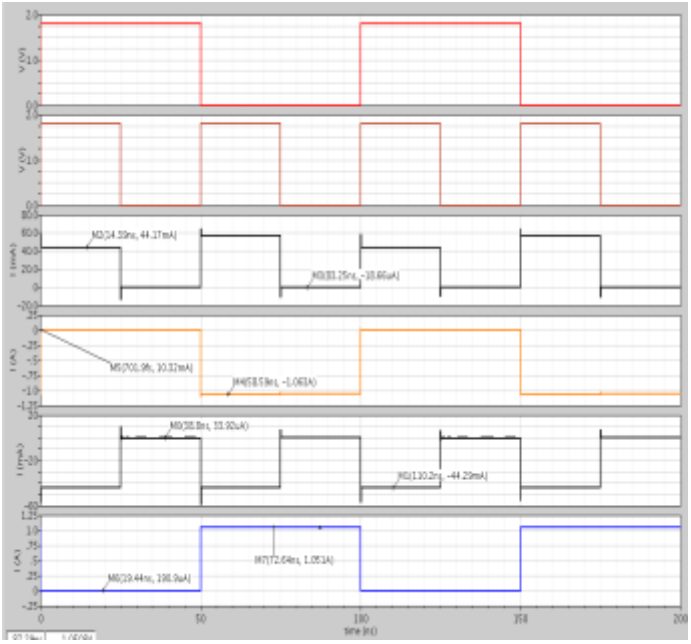

Fig. 7- Current at the source and substrate terminals of the pMOS and nMOS of input stages

Since the design is new, the compatibility with the other modules is not good. So we need extra overhead to design systems where this circuit can be applied. The compatibility issue is just a matter of advancement of the technology. Introduction of the multi-valued logic to current technology still seeks a path of advancement in the technical era.

Introduction of the enable circuitry doubles the chip area required for simple decoder design (without enable circuitry). We can reduce this extra chip area by using only pMOS at the source of the input stage pMOS and its gate is connected to the enable input (fig. 8). If that pMOS is off, the power supply will be disconnected and the circuit will be switched off.

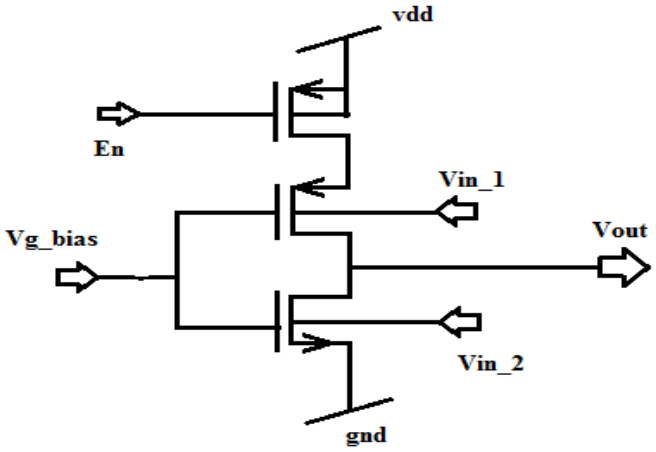

Fig. 8- Enable input with single pMOS stage

VI. CONCLUSION

A new multi-value logic generator design is introduced with a less chip area and with two supply rails. Design can be used as a 2-to-4 decoder circuitry. The design is not much power efficient and less compatible to the other digital system. As per the future scope is considered, the inefficiencies of the circuit can be reduced with some extra components and with the development of the design on SOI technology.

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