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2.5v 900 MHz 0.13µm CMOS cascode low noise amplifier for wireless application

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Abstract : *This paper presents low noise amplifier (LNA) for wireless application as RF front end which has been implemented in 0.13µ RF CMOS technology. The LNA was designed using inductive source degeneration cascode topology which produces better gain and good stability. From the simulation results, the LNA exhibits a gain of 26.46 dB, noise figure (NF) of 1.16 dB at 115µW , output return loss (S22) of −6.55dB, input return loss (S11) of −14.46dB, reverse isolation (S12) of −39.76 dB, and a power consumption is 7 mA from a 2.5V power supply.*

Keywords - *Low noise amplifier; RF front-end, cascode, CMOS, inductive source degeneration.*

I. INTRODUCTION

Nowadays ,there have been many extensive studies and efforts to improve the noise figure in RF transceiver also CMOS integrated circuit for wireless application is receiving much attention, due to their potential for low cost . A key building block for the RF front-end is the low noise amplifier (LNA) which precedes a high noise stage plays a critical role in determining the over-all noise figure (NIF) of the transceiver. From a cost standpoint, the LNA is implemented in 0.13µm RF CMOS technology. Recent works in designing LNA have there have been a difficulty in attaining both low noise figure and low power consumption simultaneously. This paper describes the implementation of LNA using 0.13µm CMOS technology which meets low noise figure, higher gain and low power consumption simultaneously at 900 MHz frequency. Following text is divided into three sections; section II describes LNA design section III gives simulation results, section IV presents the conclusion.

II. LNA DESIGN

1) Circuit Topology

A fig (1) shows a cascode topology, A single-stage cascode amplifier topology with inductive degeneration at the source is used. A cascode topology is chosen to minimize the power dissipation and to improve 1-dB compression point. Here a cascode transistor M2 provides high impedance which improves isolation between input and output that increases stability of amplifier. The work is focused on developing the LNA circuit for 900 MHz application. The use of inductive degeneration provides input matching and noise matching with better gain and stability along with low power consumption simultaneously.

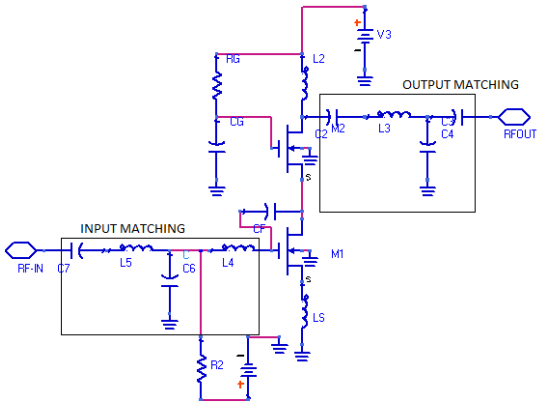

Fig.1: Schematic of LNA

2) Low noise amplifier:

Low noise amplifier is an important block in wireless receiver .it determines the receiver performance .the figure (1) shows schematic of LNA .circuit shown in dashed box both at input and output side are matching components of LNA while rest of the circuit is actual LNA.

The LNA is full of trade off between optimum gains, optimum input matching, low power consumption, lowest noise figure and linearity. The gain of LNA should be high enough to reduce noise contribution of subsequent stages; also noise must be as low as possible to minimize the impact on receiver noise performance. The input impedance of LNA is matched to 50Ω(characteristic impedance of antenna).The transistor M1 and M2 are depletion mode devices .resistor R2 and V2 are used to set voltage condition at M1 gate .RG is used to provide voltage at M2 while CG is used to eliminate any noise from the bias network .LS is used for stability. The input is coupled to gate of M1 with coupling capacitor Cs .the input is matched to 50 Ω using matching network and inductor LS .In this LNA design transistor M1 have gate width of 10 µm and 20 fingers ,transistor M2 has gate width of 5 µm and 1 finger. The transistor M1 is biased at 0.5 v and M2 is biased at 2.5v respectively, CF forms feedback network for M1 .The feedback degrades noise while improves linearity and offers easy input matching for LNA. A simple gain equation of LNA is given by following equation,

AV=RF OUT /RF IN

Feedback network affects gain of LNAQ but provides better stability.

III. SIMULATION RESULTS

All simulation for this LNA has been performed using Agilent's ADS-2009 using TSMC 0.13µm CMOS .a fully integrated 900 MHz LNA in 0.13µm RF CMOS has been designed, LNA employ lumped inductor and capacitor for matching input and output .fig (2) shows gain (S21) and (S12) of LNA .the S21 is -26 dB at 900 MHz, the S12 is -40 dB at 900 MHz.fig(3)shows input and output reflection co-efficient (S11) and (S22) of LNA .the S11 is lower than -10dB while S22 is -6dB at 900 MHz .fig (4)shows stability of LNA which is greater than 1 for all frequencies.fig(5)shows noise figure of LNA .the noise figure is 1.04 dB at 900 MHz . The LNA is biased with VDD 2.5v and consumes 7mA current.

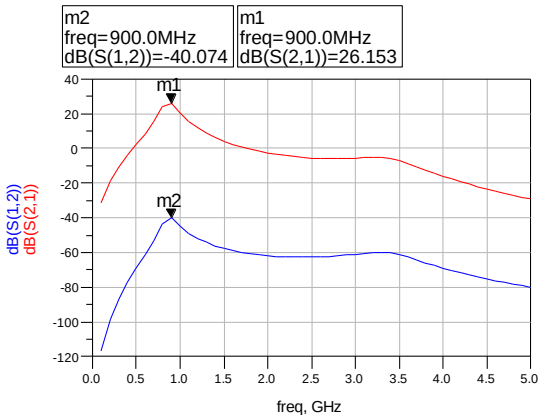

Fig2: *gain and isolation of LNA*

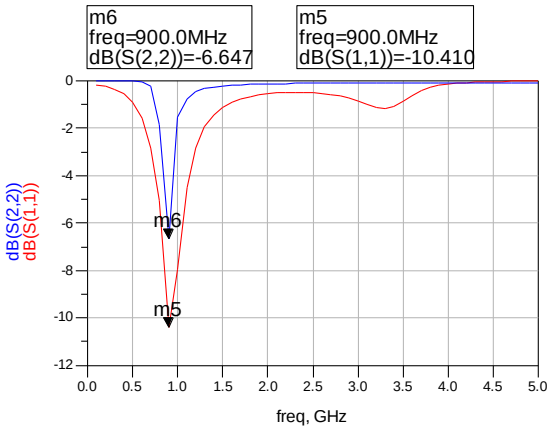

Fig3: *input and output reflection co-efficient*

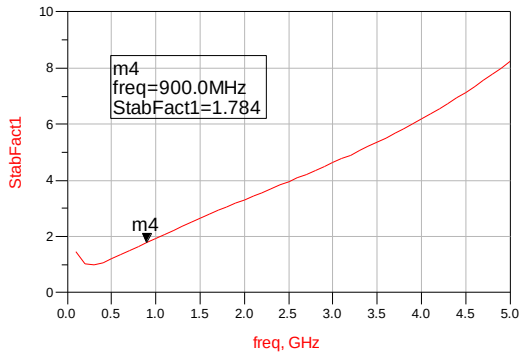

Fig 3: stability factor

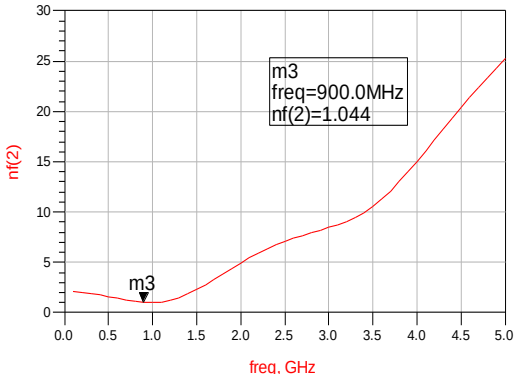

fig 4: noise figure

Table 1: summary of LNA parameters

LNA	Measured parameter
Supply voltage	2.5v
Technology used	TSMC 0.13 µm CMOS
RF frequency	900 MHz
Voltage gain (S21)	26 dB
Noise FIGURE	1.04dB
S11	-14 dB
S22	-6 dB
Power dissipation	115µW
Current consumption	7 mA
Reverse isolation	-40 dB

IV. CONCLUSION

The TSMC 0.13 µm CMOS high frequency model is used to design 900 MHz receiver front end. This paper presents 900 MHz LNA with noise figure 1.04 dB with power consumption of 115 µW from 2.5v power supply .the LNA exhibits gain of 26 dB. From both performance standpoint and cost standpoint, these results show that CMOS is very competitive with available technologies.

REFERENCES

JOURNAL PAPERS:

[1] Brian A. Floyd, Jesal Mehta, Carlos Gamero, and Kenneth K. O, A 900-MHz, 0.8-pm CMOS Low Noise Amplifier with 1.2-dB Noise Figure, *Silicon Microwave Integrated Circuits and Systems Research Group (SiMICS) Dept. of' Electrical and Computer Engineering, University of Florida, Gainesville.*

[2] Andrew N. Karanicolas, A 2.7-V 900-MHz CMOS LNA and Mixer, *Member, IEEE*

[3] Arjuna Marzuki, GaAs pHEMT cascode LNA for wireless application, *International journal of computer and electrical engineering ,vol.1,No.2,June 2009,1793-8163.*

[4] Jon Guerber,Design of an 2.4GHz CMOS LNA, *ECE 621,winter 2010.*