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A Review on Design and Application of CORDIC algorithm

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Abstract: *Co-ordinate rotation Digital computer is the full form of CORDIC is the uncomplicated and structured algorithm to enumerate the problem defined functions such as real and complex multiplications, division, square root etc using simple addition, subtraction and operations like level shifters, hyperbolic and logarithmic functions, calculation of trigonometric. Rectangular to polar and polar to rectangular is an important operations in CORDIC which are generally used in ALUs, wireless communications, DSP processors etc.*

This type of conversion needs a hardware application of square root and arctangent circuits. The outcome of these applications gives complexity in hardware design, area and power consumption. The CORDIC algorithm is used to overcome these parameters. This paper proposes the experimental results based on various methodologies on design.

Keywords: *CORDIC, FPGA, Standard cells, VLSI*

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I. Introduction

Co-ordinate rotation Digital Computer or (CORDIC) which is also known as Volder's algorithm is a easy and efficient algorithm used to calculate hyperbolic and trigonometric functions. When Jack E Volder proposed the CORDIC it was only based on the principles of two dimensional geometry such as trigonometric functions, after five decades the CORDIC has been emerged in various applications and have progressed in the areas of the design algorithm and developed the architectures to provide high performance and less expensive hardware solutions. It is realized that by varying a simple variables, the algorithm might become solitary which results in uniform implementation of the broad range of primary transcendental functions that involves methods like exponentials, log functions and square roots etc. all this parameters was very suitable for an application like scientific calculators.

The other applications which are drawn from the CORDIC algorithm are direct frequency synthesis, modulation and coding for speech/music synthesis and communication, direct and inverse kinematics computation for robot manipulation, and planer and 3-D vector rotation for graphics and animations. The conversion of rectangular to polar and polar to rectangular function are the two major operations in CORDIC. Basically they are the two different coordinates to represent the 2D plane. The rectangular coordinates are in the form of (x, y)where 'x' stands for horizontal plane and 'y' stands for vertical plane from the origin likewise polar coordinates are in the form of(r, Θ) where 'r' stands for distance from the starting point to the estimated point and 'Θ' is an angle measured from positive 'x' axis. The polar coordinates are habitually used in navigation in marine and aerospace using radars. They are used in different processors like ALU, DSP and various communication purposes like wireless and satellite communication. In this paper we will discuss about various methods on implementing hardware architecture on CORDIC.

In this paper, we have reviewed the different implementations of CORDIC algorithm like FPGA and some software implementations. Section III of the paper describes the software implementations of the algorithm, while Section IV outlines the FPGA implementations. In the last section we have discussed the various technologies used f the design of standard cells.

II. The Cordic Algorithm Architecture

The authors [1] describe the CORDIC (CO-ordinate Rotation Digital Computer) algorithm is the most powerful method for understanding the multiple modulation schemes. The CORDIC algorithm is used in modulation to convert coordinates from polar to rectangular. Different digital modulation techniques in MATLAB realization and VHDL implementation include ASK, FSK and PSK with VHDL realization of BPSK, QPSK and QAM modulation. By using this algorithm we can reduce the hardware component i.e. we can adjust

the configuration of a single hardware with the only software element changing. The algorithm is a useful tool for phase conversion to sine amplitude. A basic hardware implements CORDIC by repetitive shift add operations.

III. Software Implementation

For application specific CORDIC processors the most common application is in Digital signal processing for vector rotation. In the paper [2], the design of pipeline architecture is defined based on application-specific CORDIC processor for the computation of Sine and Cosine values. Due to its pipeline architecture, CORDIC's design in circular rotation mode gives high system throughput by reducing latency in each individual pipeline level. Saving area on silicon substrate is important for the design of CORDIC pipeline, which can be accomplished by minimizing the number of micro-rotations.

The synchronizer function is autocorrelation. The autocorrelator is used in wireless communication applications of the fourth generation to detect frames and approximate the carrier frequency. In the OFDM amplifier, CORDIC is efficiently used to measure the frequency offset and to determine the division equation for calculating channels .In the paper [3], by using 130 nm technology, a fast pipeline CORDIC architecture and autocorrelator is designed, implemented and tested. A MATLAB simulation is performed to functional verification before the Verilog HDL coding. Digital signal processing (DSP) has always been driven by advances in DSP applications and very-large-scale (VLSI) technology. This raised many issues with DSP applications deployment. These implementations will meet the DSP systems ' defined real-time sampling rate constraints which require less space and power consumption. Flexibility, high throughput low power and low cost are driving forces for the development of today's VLSI (FPGA / ASIC) based mobile and wireless communications. The OFDM-based WLAN is the next-generation technology, dealing with two small and main components, namely autocorrelation for the synchronization of the received signals and CORDIC for channel estimation computation and OFDM compensation in the wireless receiver.

Several components of the electronic circuit, due to the various factors associated throughout the circuitry, do not get the clock at the same time. For frequency generation and stability the phase locked loop design is very popular. Authors also discussed in a paper [4] that describes an all-digital phase locked loop which is one of the PLL models where all the elements used are digital in nature giving it an advantage over FPGA. PLL's all-digital design uses the digital component that is flexible to use and immune to environmental factors such as temperature and parasite capacity. The use of digital components has provided noise immunity, which enhances circuit accuracy and functionality. The ADPLL is used in a wide range of implementations such as wireless communication, device control, biomedical and many other fields, requiring low power, high speed, and less chip area. The designed ADPLL works on accumulator for 100 MHz, 16 bit.

The paper[2] discussed the use of CORDIC algorithm in DSP for vector rotation using the pipeline architecture which saves area on the silicon substrate and also gives high throughput. In paper[3] the CORDIC algorithm is used in an OFDM amplifier in which also saved significant area and power which are the main constraints in VLSI technology. Paper [4] gave the software implementation of CORDIC in the fields like wireless communication, monitoring and biomedical applications.

With these advantages there are also drawbacks to the software implementation of CORDIC. With the implementation for DSP, the algorithm must follow an imposed sampling rate and must also save space and power along with it. Thus to make this possible FPGA implementation was introduced to lower the cost and power consumption.

IV. FPGA Implementation

The Hough Transform (HT) is seen to be employed commonly in image processing or in pattern recognition, such as circles with arcs, ellipses as well as other forms. The authors [5] proposed architecture for straight line detection, implemented on FPGA computers, uses both the gradient algorithm and CORDIC. To minimize the amount of equations, the gradient was implemented to allow less time and the CORDIC algorithm has been utilized to make the operators less complicated. Increasing the number of samples will increase performance, and will also down the rate of processing.

The paper [6] discussed CORDIC rotator which is built using pipelined architecture. It has a unit controller to control data sequence and give output. A CORDIC operates in 2 main modes: rotation and vectoring. In rotation mode, the input vector is rotated by a vector angle while in vectoring; the inputs are rotated along x-axis recording the amount of rotation. This model is simulated to transform 1024 data (1K) from Cartesian domain to polar domain and vice versa. The output data is compared with the initial data to find the error data. Advantages of pipelined architecture is that it has high throughput, uses less memory to store angle values, free from looping iteration and zero delay. The pipelined CORDIC was implemented in FPGA ALTERA cycling and the design worked at 81.31 MHz with a minimum error value of 0.05. A time and area efficient CORDIC algorithm is designed by properly choosing the approximation of Taylor series which meets the

required range of convergence (RoC).The area, latency requirements and accuracy is achieved by manipulating the iterations in the series.

The algorithm designed by the authors [7] has lower complexity when compared to other available scaling free algorithms which require expansion of RoC over the whole coordinate space. Here the rotational CORDIC mode follows the following some steps. To avoid scaling function, we use sine and cosine function of Taylor series and selecting a proper RoC depending on the values of approximation values of Taylor series. The designed CORDIC algorithm has a low slice delay of 17% with more slice consumption penalty of about 13%. This is implemented in Xilinx Spartan 2E using the code synthesized in Xilinx ISE9.2i.

The architecture designed in the paper [8] is mainly for Attitude determination in satellites using some and cosine functions. The attitude determination system involves higher accuracy which is important for finding point accuracy. The proposed CORDIC approach is faster when compared to the on-chip software installed in satellites with FPGA implementation. The sine and cosine values are considered as integer values and use two's complement for representation for MSB of angle for rotation. Before this, the multiplication factor is multiplied to avoid the use of multipliers. The architecture consists of a clock which makes is a sequential system with required shifts in the clock cycles using barrel shifters. It consist of MUX, adders/subtractors, registers which are coordinated using a control unit which produce a look up table after processing. The RESC and RESET are used for resetting the counter (which count the number of iterations) and the system respectively and SEL for multiplexers. The algorithm was verified using Xilinx ISE 12.1 and implemented on Altera's FPGA. The proposed designed was compared with a C++ program which proved the approach to be 27500 times faster then it. This approach is also used for calculator with good efficiency in area.

The proposed architecture in the paper [9] is a combination of parallelism and pipelining method. This processor is speed-area optimized and is applicable for real time operations. The architecture is formed by combining 'K1 computation architecture' and 'unscaled CORDIC architecture'. In this design, we use radix-4 method which in turn reduces the number of iterations when compared to radix-2. This results in a 32 bit output in every 8 clock cycle with the completion of CORDIC rotation in 5 cycles for 16 but precision. Here, the reciprocal of scaling factor (K) is obtained which is then multiplied with unscaled factor in an array multiplier. The output of this multiplier will X and Y co-ordinate scaled versions, each of which will be 32 bits. MATLAB tool is used for processing the algorithm which computes scale factor in parallel with rotation of CORDIC.(n/2) number of clock cycles are required for the computation for 32 bit output accuracy which defines the latency and the power consumption at 56.96 MHz(operating frequency) is measured to be 380mW using Power software tool. Thus with the help of the proposed design, speed area optimized architecture is obtained. XILINX-FPGA is used for implementing this design which produces a total gate count of 11528.

In another paper the authors [10] compare the various CORDIC architecture in terms of throughput and area efficiency which are verified using Spartan -ll FPGA. The CORDIC, being low cost and efficient as various applications like logarithmic, complex number, solution of linear systems, SVD for signal and image processing, scientific computation, etc. The CORDIC algorithm is based on number of iterations of addition/subtraction or shifting process and doesn't involve division or multiplication. The CORDIC operates in 2 modes. In vectoring mode, the input vector is studied in terms of its magnitude and phase. In rotation mode, the angle of the input vector is calculated with respect to X and Y coordinates. The CORDIC rotator usually analyses arctangent, rectangular and polar coordinates and various trigonometric functions.

1) Iterative architecture: This architecture works upon clock signal which processes the data sequentially bit by bit using shift adders and subtractors. The architecture size increases with increase in internal precision. It consists of a control unit which is operated using state machine.
2) Higher Radix: This architecture decreases the time consumption with higher complexity in hardware design.
3) Parallel or Cascaded architecture: This architecture consists of an array of shift adders/subtractors which perform the iteration simultaneously. Its size depends on number of times internal precision. It has a higher throughput and lesser latency when compared to iterative design. It has two major disadvantage of having larger power consumption amount and greater architecture area.
4) Pipelined architecture: This is similar to parallel architecture with the usage of pipelined registers for analyzing continuous data. It has higher frequency on operation then above described designed which proves it to be the most desirable architecture for satellite communication of higher frequencies. The power consumption of the system gradually decreases with increase in clock period. Major disadvantage is larger are due to registers.

In a paper [11], a method of reconfigurable CORDIC that operates in both hyperbolic and circular trajectories in vectoring and rotation modes of CORDIC. This is the first ever systematically designed methodology for reconfigurable CORDIC to operate in both the modes for both the trajectories. Reconfigurable CORDIC has higher values of applications in signal processing, robotics, scientific calculations, etc because of its ability to switch between hyperbolic and circular trajectories in both the modes.

The most disadvantageous part of conventional reconfigurable CORDIC is the scaling factor and incompatibility for RoC of both the trajectories.

- Rotation-Mode Reconfigurable CORDIC: This CORDIC consists of 3 main steps, the pre-processing, rotation unit and post-processing. The pre-processing unit keeps a track of the rotation angles of input while the post-processing unit is necessary for swapping the cosine and some values for circular trajectory.
- Reconfigurable Vectoring-Mode CORDIC: This CORDIC makes use of pipelined architecture for processing which results in the output in 8 stages.
- Proposed Generalized Reconfigurable CORDIC: This CORDIC operates in both vectoring and circular mode by choosing the trajectory using a bit signal T.

The designed CORDIC is implemented in Xilinx ISE and the code is written in Verilog. The proposed design saves up to 60% of area when compared to recursive reconfigurable CORDIC. Also the pipelined vectoring and rotation mode CORDIC saves up to 30% -50% of area without any change in operating frequency with respect to reference reconfigurable design.

The method put forward in another paper [12] is obtained from a single coordinate architecture using FPGA. This algorithm is verified on Virtex-ll and Virtex-E systems which results in larger space when compared to single mode architecture. It is also observed that, if this algorithm is implemented in RTL would result in a larger area with falling throughput. With a little larger increase in the cost of hardware, an algorithm is designed with 3 configurable modes of operations. Optimized design can be developed which would help in saving area at the sequential received point with loss of data rate in signal processing.

This authors also proposes a CORDIC and SVD algorithm in a paper [13] for hardware implementation which consideration of floating and fixed point logic. These are processed in Xilinx tool with VHDL code. This process involves replication of CORDIC modules for analyzing matrixes in terms of accuracy, allocation of resource and speed. Higher speed and lesser allocation of resources is seen in fixed point method. The advantage of this method helps to obtain a methodology for computations of larger dimensions. This would reduce the independence of complexity.

The paper [14] explains about Mixed Scaling Rotation CORDIC algorithm is a combination of scaling Micro-Rotation phases for digital signal processing systems which require high speed and angles in advance because many simple CORDIC algorithms have round off noise. Along with this control and impairment reduction schemes are designed. This design results in Increases, the signal to noise ratio using internal dynamic range. The variance and mean along with first and second order statistical properties are analyzed which shows an enhancement in these properties. The VLSI design structure as a compromise in quantization error performance and complexity of hardware.

The proposed scheme is applied for various processors involving FFT process of different lengths with the help of twiddle factors. This is also applicable for EVD (Eigen value decomposition), SVD (singular value decomposition), etc. Another method has also been proposed called the EEAS that stands for 'Extend Elementary Angle Set' which basically decreases the number of iterations to a larger extend with which the proposed method is being compared with. The major advantage of MSR designed CORDIC is high performance EEAS, Universal Vector Rotational CORDIC Engine, a combination of rotational and scaling operations, decrease in round-off noise and SQNR with smaller variations. The basic parameter of image processing is the rotation of input vector which increases its complexity in real time applications. The process introduced in a paper [15] is highly useful in robotic and medical applications.

The main features of image processing are accuracy, precision and speed. The proposed design is a combination of bilinear interpolation and modified CORDIC algorithm in a repetitive and folded method. This method increases RoC area and calculates the scaling factor in parallel rotations. This algorithm is processed in Xilinx FPGA with verilog code showing a lesser complexity, power consumption and area of hardware. The designed method requires only added/subtractors with shifters for computation. Thus it concludes that the proposed method is highly efficient than Xilinx CORDIC core and the throughput of this design can be increased by using parallel methodology.

In a paper [16] the authors have also compared the outputs of two FPGAs are compared for processing CORDIC algorithm with increased throughput and speed using pipelined architecture. The cost is calculated depending upon the area occupied. Because of higher speed of FPGAs they are used as co-processors when compared to microprocessors.

Depending on the two modes of the CORDIC, unrolled CORDIC is found to be the highest speed hardware circuit when compared to serial and parallel bit CORDIC. The latency of parallel bit and unrolled CORDIC is count to be n cycles while serial bit has a count of $n \times n$ cycles. While high-radix CORDIC is slower because of its complexity.

V. Standard Cell Design

A standard cell library consists of cells with many templates which differ in area, driving capabilities, intrinsic delay, and capacitive loading. A logical circuit is designed using the best template which reduces the area of the cells and the delay.

The algorithm developed by the authors [17] in the paper helps in effective selection of the standard cells. The deal selection of standard cells is a cell-based sizing problem of each transistor. Hands on and analytical approaches have been tried in combination to optimize the size of each transistor. The algorithm suggested provides outputs in different stages. At each stage the templates of a group cells is changed based on their sensitivity and criticality values. Map command from misII performs the mapping of the Boolean network using gates from the library. If there are different gates with varying area satisfying the Boolean network then a selection from the misII cell library can be considered. The algorithm can handle large networks efficiently considering the entire circuit instead of the paths.

In a paper [18] authors also introduced Synopsys Design Compiler which is used to perform logic translation and minimization based on the standard cell library with both pass transistor logic (PTL) and CMOS logic cells. PTL circuits have been claimed to be better to use for arithmetic circuits than the CMOS logic. They perform better in circuits which use exclusive OR function compared to the CMOS logic. The PTL cells and CMOS have different features in area, speed and power. A hybrid of these cells can modify the design flow in terms of area, speed and/or power. The CMOS circuits have less delay and the PTL circuits have less area and power. Hence the hybrid of both types gives optimum results for individual goals. The hybrid

PTL/CMOS can be easily applied into the standard cell based design flow with the Synopsys Design Compiler. This leads to best performance in AO and DO synthesis.

The libraries for ultra-low voltage requirements are designed with respect to the criteria which vary with respect to the regular above threshold libraries. The paper [19] discusses the severe problems at the ultra-low voltage and sub-threshold are identified and analyzed using simple principles. These principles are also used to design the CMOS standard cell libraries.

Ultra-low powered circuits are used for applications where the primary aim is to reduce the power consumption. Consumption is a key factor and low performing circuits are preferred. Consumption is reduced by reducing the V_{DD} voltage or the operating voltage. The PMOS/NMOS balancing principle is used to reduce the voltage to V_{DDmin}. Based on this a standard cell library s designed. On Silterra 180 nm and 130 nm, ASCLIC was able to distinguish the standard cell library, and the findings were comparable to the commercial resource. For 180 nm, the highest percentage shift is 0.02729 %, 1.26948 % and 0.00128 % respectively of leakage capacity, internal power, and timing. For 130nm, the highest percentage change is 0.00172%, 1.92737% and 0.00198% of leakage power, internal power and timing respectively.

Table no 1: Standard cell's timing and power (ASCLIC and NCX) in 180nm and 130nm technology

Cell	Measurements Percentage Changes (%)					
	Leakage Power		Internal Power		Timing	
	180nm	130nm	180nm	130nm	180nm	130nm
BUFX1	0.00691	0.00167	0.00136	0.01257	0.00002	0.00002
INVX1	0.02729	0.00000	0.00626	0.51630	0.00069	0.00047
AND2X1	0.00376	0.00054	0.38637	0.52018	0.00002	0.00002
XOR2X1	0.00212	0.00009	0.00093	0.01466	0.00002	0.00002
AND3X1	0.01434	0.00094	0.63558	1.22125	0.00005	0.00002
AOI21X1	0.00606	0.00060	1.26948	1.40209	0.00128	0.00047
AND4X1	0.00495	0.00172	1.13208	1.92737	0.00010	0.00002
AOI22X1	0.01205	0.00007	1.12707	1.20348	0.00076	0.00198

Software for characterization of standard cells are built but not many softwares are available for public use. The paper [20] introduces ASCLIC (Automated Standard Cell Library Characterization) that was built to solve this problem. Unlike other services ASCLIC does not require paid license as it is a web service. The netlist should be uploaded after which models and configurations are e-mailed to the user. The software specializes in the characterization of Non-Linear Delay Model (NDLM) and Non-Linear Power Model (NLPM). Software like CCS give higher accuracy for process below 90nm technology, NLDM offers uncomplicated and faster output with respect to simulation time and test-bench generation. The software was tested on Silterra 180nm and

130nm technology based on combinational technology and varying number of inputs. Fast and slow processes were compared to the typical process whose results are divided into two categories: characterization accuracy comparison and benchmark performance.

The design flow for characterization of standard cells has five different technologies. The paper [21] tool uses the results of the technologies and combines them with other VLSI tool processes that can be implemented easily. The false-technology FreePDK45 is used as one of the technologies for 45nm technology. Other technologies used are 0:18 µm, 0:25 µm, 0:35 µm and 0:5 µm. The design flow is automated for Virtuoso liberate from Cadence Design Systems. For each technology each library is made up of multiple cells with different drive strength. Detailed views on the electrical behavior of each of the cells are generated upon characterization of the cells. The database is generated by the tool and all of this information is stored and characterization reports are obtained. The reports consist of timing, power and signal integrity and the electrical behavior of the cell. Fabricable standard cells from other technologies like 0:18 µm, 0:25 µm, 0:35 µm and 0:5 µm can also be characterized using this design flow.

CORDIC rotator is build using pipelined architecture. It has a unit controller to control data sequence and give output. A CORDIC operates in 2 main modes: rotation and vectoring. In rotation mode, the input vector is rotated by a vector angle while in vectoring, the inputs are rotated along x-axis recording the amount of rotation.

The model introduced in the paper [22] is simulated to transform 1024 data (1K) from Cartesian domain to polar domain and vice versa. The output data is compared with the initial data to find the error data. Advantages of pipelined architecture is that it has high throughput, uses less memory to store angle values, free from looping iteration and zero delay. After the architecture of the cortex, the verification process is carried out which includes functional simulation, waveform simulation, and signal tap in FPGA. Functional simulation is used to verify the Verilog code and the synthesis result is used for waveform simulation and signal tap. The pipelined CORDIC was implemented in FPGA ALTERA cycling and the design worked at 81.31 MHz with a minimum error value of 0.05.

Several contributions have been made to harness the underlying physics of sub-threshold devices to develop an improved cell library for sub-threshold synthesis. The authors [23] discuss the factors affecting CMOS device sizing in sub-threshold operations are The Reverse Short Channel Effect (RSCE) and the Inverse Narrow Width Effect (INWE). In RSCE, as the HALO dopings are inserted at the drain and source, their dopants overlap in short channel systems, increasing the total density of dopants in the channel A 12-track implementation (2.4µm height) has been chosen, since this is the form factor used by the existing ARM R&D library. This provides a maximum width of 840 nm for each device, taking into account minimum poly overlap rules, P&R boundary distances and assuming equal P and N type diffusion areas. Two of these are discussed. The first is the standard cell sizing method, as used in the super-threshold. This suggests that increasing the width of the NMOS and PMOS devices increases their current capacity to produce, and thus produces faster cells. The second boundary suggests that to maximize gate control and thereby the ION/IOFF ratio, minimum width devices should be chosen as this maximizes the advantage produced by INWE.

The impact of negative short-channel effects in transistors is rising, especially at and below the 28 nm technology, with the reduction of geometrical sizes. Use of FinFET technology introduced in the paper [24] for 22 nm node and below instead of standard planar CMOS offers an alternative to short-channel effects problems. The mathematical model provides the analysis of the circuit timing on the basis of Elmore delay model for the specific transistors and their parallel and serial connections. This model replaces each of the transistor cells to its equivalent Pi-model. The gate delay is defined as a function of its corresponding output node resistance and capacitance.

With the change to nanometer technology as transistor sizes shrink to 28 nm and below, a range of fundamentally new design challenges are not addressed in current VLSI EDA devices, including the issue of schematic synthesis and 3D transistor structure architectures for MOS technology. With the rise in level of implementation of current microelectronic devices and the decrease of regular cells in structural sizes, design rules get more complex and their quantity grow. Despite the technology scaling decreasing sizes, the normal systems become increasingly relevant.

Typically, portable / implantable biomedical instruments have high energy resources to extend battery life, but vague operating frequency requirements caused by low bio-signal bandwidths, typically below a few kHz which are discussed by the authors [25] in the paper. For biomedical applications power consumption is important. This requires a methodology to develop a suitably designed custom SCL for biomedical devices to achieve better performance in terms of strength. On comparison with the commercial standard cell library with the designed sub-threshold standard cell using a 5-stage ring oscillator and an ECG designated FIR filter the results showed a total power saving of 95.62% and a leakage power reduction of 97.54%.

Table no 2: Overall Comparison between ASIC, FPGA and PCB

(Anysilcon, 2018) **Parameters**	**ASIC Design**	**FPGA solution**	**PCB Solution**
Area	Smaller	Large	Largest
Power	Lower	Higher (9-12x)	Highest (12-15x)
Performance	Fastest	Slow	Slowest
Protection	More secure	Easy to reverse engineer	Least secure
Cost	Low for high volume	Lower for small volume	Lowest for very small value
Time to market	Long	Short	Shortest
Flexibility	Inflexible	Configurable	Flexible

VI. Conclusions

This paper gives a review of CORDIC algorithm. We have surveyed the various implementations of CORDIC algorithm mainly the software and FPGA implementation and the work done by various authors on improving the area used on the silicon substrate. [2] From the survey we can conclude that both software implementation and FPGA implementation have advantages of their own.

The paper reviews the work on standard cell design and their optimization in the area and power consumption. Major aspects to be considered to build a standard cell library are the area covered by the cell, its time constraints and the power consumption. A standard cell library can be constructed for application specific requirements.

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