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Novel Scheme For Multiple Scan-Chains Bist And Weight-Based Segmentation For Testing

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Abstract: *The objective of proposed system is to design the weighted based cell segmentation algorithm for multiple scan-chains BIST in order to reduce the average power consumption during the scan in of new test vectors, and to reduce the test application time. The technique is based on selecting the best group of cells to be connected in the same scan-chain. This group of cells should have the same or very close weight of logic 1's and 0's that will be optimal to get the highest fault coverage in a specified test length. Then each scan-chain input will be connected to an output of a combinational circuit located after the Linear Feedback Shift Register (LFSR) that will generate biased test vectors according to the optimal weight of this segment of cells in the scan-chain. Thus, increasing the fault coverage and smoothing the applied test patterns will reduce the power consumption. The System is designed by using Verilog HDL and Simulation will be done through Modelsim 6.4 c. Finally the Synthesis will be done by means of using Xilinx FPGA with the model of Spartan 3 XC3S 200 TQ-144.*

I. Introduction

Linear Feedback Shift Registers (LFSR) is the most widely used pseudorandom Test Pattern Generators (TPG) in Built-In Self-Test (BIST) systems. The reasons why LFSRs are commonly used as TPGs is that a small overhead in the hardware area can change a normal register to an LFSR during test mode, and the LFSR can generate all possible test vectors in a pseudorandom way (with the exception of the all 0-vector, since this will lock the LFSR). Using LFSR as a TPG is considered to be better than BIST systems were an extra memory is used to store a deterministic set of test patterns that can get high fault coverage because of the cost of that memory.

However, the pseudorandom testing will take longer time than deterministic test to achieve the same fault coverage. In the recent decades, many techniques have been introduced to minimize the power consumption of new VLSI systems. This is because in high performance VLSI design it is important to reduce the heat dissipation as it greatly affects the performance of the system and may lead to system malfunction or to a permanent damage of the chip. Furthermore, with the advancement of portable devices more work is done on low power design to lengthen the battery time as well. Thus, the low power design is considered one of the most important challenges in VLSI system design. However, most of these methods focus on the power consumption during normal mode operation, whilst test mode operation has not normally been a predominant concern till the last period.

One of the main reasons why the switching activity is high during testing is the low correlation between the consecutive vectors generated by the LFSR which applied to the primary inputs of the CUT. As a result of the excessive switching activity, power consumption will increase, thus reducing battery lifetime, and also causing heat dissipation which may permanently damage the CUT. On the other hand, it is important to get high fault coverage in a CUT while minimizing the test length as much as we can. Shorter test length has mainly two advantages in the system: First, it will reduce the test application time without degrading the fault coverage. And reducing the time will also decrease the energy consumed during test and will improve the battery lifetime. The first type is test-per-clock, in which the outputs of a TPG directly feed the inputs of the CUT, and the outputs of the CUT are directly connected to a signature analyzer. In this scheme a test vector is applied to the CUT, and a response is captured from the CUT on each clock cycle. The second scheme is test-per-scan, in which a scan path is used to shift test patterns into a CUT.

A full scan cycle requires m+1 clock cycles, where m is the number of flip-flops in the scan-chain. The response to an applied test pattern is captured into a scan-chain and scanned out in the next scan cycle in parallel with scanning in another test pattern. In these test schemes, which is widely adopted in the design of combinational circuits (test-per-clock) and the sequential circuits (test-per-scan), most of the CUT nodes undergo switching whilst applying test patterns. Hence, a substantial amount of the power dissipation occurs during this operation because of the uncorrelated patterns produced by the LFSR.

To solve highly complex VLSI testing problems, the built-in self-test (BIST) technique has been extensively studied and widely used. This approach introduces the embedded test structure into the circuit under test (CUT) to make testing easier and more efficient. This structure usually consists of the pseudorandom test pattern generator (TPG) and the test response analyzer, and both of them are usually based on the linear feedback shift-register (LFSR). LFSR, built with little area overhead, is effective to test VLSI circuits. However, the conventional LFSR cannot efficiently test nanometre technology circuits and system-on-chip (SOC) systems. Another major drawback of LFSR is that the number of switching activities in a CUT during test can be significantly higher than that during normal operation. This can cause heat effect, and seriously influence the life span of a CUT. In addition, the LFSR-generated pseudorandom sequence is very long, and test times are excessively long.

A new technique to reduce the average power consumption and to reduce the test application time will be presented. The proposed algorithm will be based on selecting the group of cells that will be connected together in the same scan segment and be fed by the same input during the scan-in of new test vectors. Therefore, for each cell, the weight of logic 0 and logic 1 to maximize the fault coverage will be found, then each group of cells that have same or very close weights will be connected in the same scan-path and will be fed from the same circuit that will be designed to produce biased patterns according to the found weight.

Weight calculations:

Assume that certain circuit has m scan cell (C1,C2,C3,....Cm) and n faults

(F1,F2,F3,..Fn). To find the weight of any cell (Ci) for any of the faults (Fi). We first find all test vectors for the fault (Fi).

W (Ci=1) for Fi =(Number of test vectors for Ci=1)/(Number of all the test vectors for the fault F)

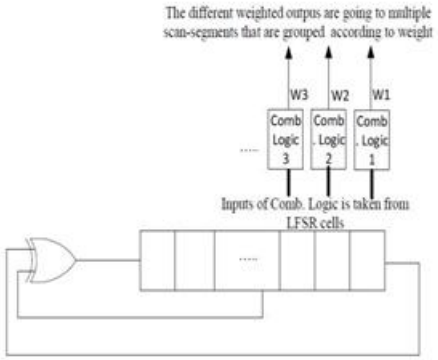

Figure 1: General Structure of the proposed design

II. Simulation Results

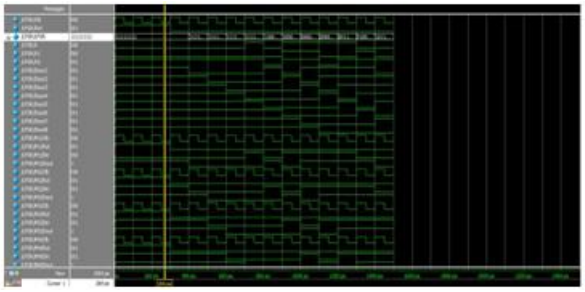

Figure 2: Output wave form for LFSR

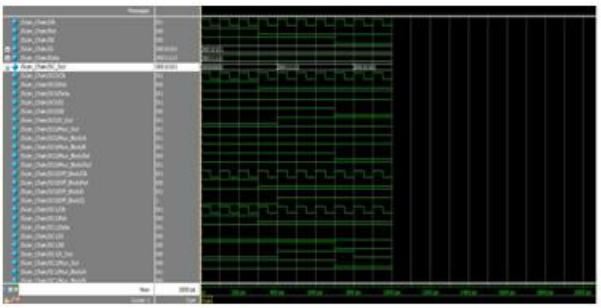

Fig 3: Output wave form for Scan Chain

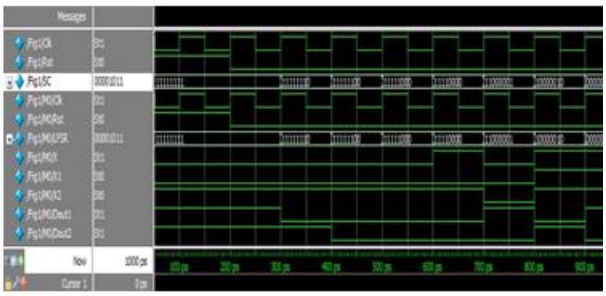

Figure 4: output response

III. Conclusion

It is clear that the proposed design achieved sufficient reduction in both the test length and average power consumption and these two factors will efficiently reduce the energy consumption by time. As a future work the proposed design can be combined with a previously proposed techniques for cell can reordering for further reduction in power consumption.

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