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Design of Read and Write Operations for 6t Sram Cell

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Abstract: *As we observe, that with the evolution of technology, devices are scaling down from time to time, which leades to reduction in the the length of the channel of the MOSFET, giving importance to speed of operation. This paper consist of designing 6T SRAM cell, along with its READ and WRITE operations which operates at high speed consuming less power. The SRAM cell is simulated and the graphs for READ and WRITE operations and respective power results are presented.The tool used for designing of 6T SRAM cell is Tanner Tool which operates at 250nm technology and 2.5volts as supply voltage*
Keywords: *SRAM, Read,Write,Tanner,250nm.*

I. Introduction

CMOS devices have been scaled down in order to achieve higher speed, performance and lower power consumption[1]. SRAM means Static Random Access Memory. The SRAM cell that we considered in this paper was 6T SRAM cell which consists of two crossly coupled inverters and access transistors to read and write the data. In case of the SRAM cell the memory built is being stored around the two cross coupled inverters. If we consider that, the input to the first inverter is logic 1 then the output of this inverter will be logic 0. So, after one cycle the output of second inverter will be logic 1. From this we can say that as long as the power is supplied to the SRAM cell logic 1 will be circulated in the inverters. Hence there is no need for periodic refreshing of the circuit. Where as in DRAM the circuit need to be refreshed periodically [2]. SRAM technology is most preferable because of its speed and robustness [3]. Therefore, SRAM is much faster when compared with the DRAM.

II. Working Of 6t Sram Cell

The 6T SRAM cell contains a pair of weakly cross coupled inverters holding the state, It also contains a pair of access transistors to read and write the states[2]. The write operation is done by driving the desired value and its compliment into the bit lines named as bit and bit_b, then raising the word line named as word.

The Overpowering of the data is done using the cross coupled inverters. The pre charging of the two bit lines is first set to high and then let to float. When word is raised the bit_b is pulled down, indicating the value of the data. The main challenge of the SRAM is to ensure that the circuit holding the state is weak enough to ensure the write operation by overpowering the previously stored value and strong enough so that it can be retained during the read operation. Both of them should be ensured to for proper READ and WRITE operations respectively. SRAM operation is divided into two phases. Let the two phases be called as ϕ1 and ϕ2. These are generated generally from clk (clock) and its complimentary clkb. Let the circuitshown in the below figure.1[2] is phase 2 pre charged circuit.

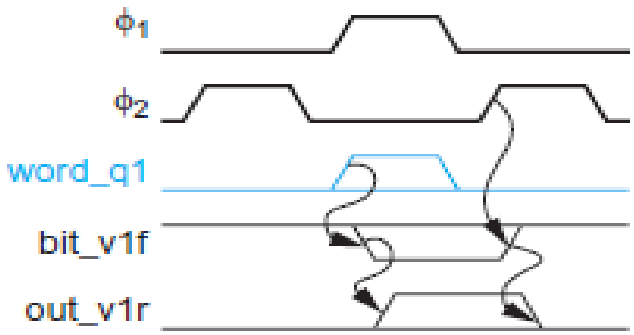

Fig.1Precharge circuit

In Phase 1, the read and write operations are performed. Here our main concern is phase 1 of the SRAM cell.The detailed structure of 6T SRAM is shown in below figure.2[2]

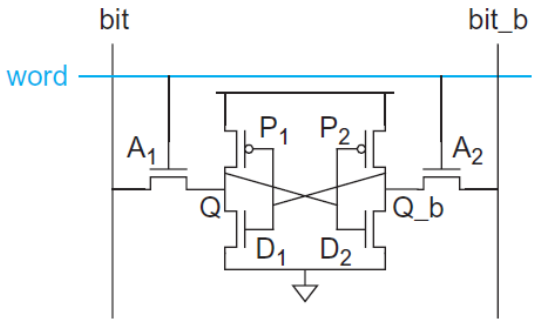

Fig.2 Detailed structure of 6TSRAM cell

Access transistors A1 and A2 are connected to bit and bit_b, so that we can read from the memory or write into the memory. If word line is equal to 1, we can access the access transistors and hence read and write operations can be performed. If word line is equal to 0, the access to the transistors will be off and memory will be in hold state[3]. In stand by mode (or) hold mode (i.e.; wordline=0) the access transistors A1 and A2 are turned off. So as long as SRAM in this mode, the data will remain unchanged [4]. To write into the memory bit and bit_b acts as input, to read from the memory bit and bit_b acts as output lines.

1.1 Read Operation

In SRAM, for any operation to be performed, the word line should be high. To perform read operation, initially memory should have some value. Therefore let us consider memory has Q=1 and Q'=0. Raise the word line to high, to perform the read operation. bit and bit_b acts as output lines, and these bit lines are initially pre-charged i.e. there will be a node voltage Vdd at bit and bit_b. As Q and bit are high, there will be no discharge in the circuit. As Q' is 0, there will be a voltage difference between the Q' and the node voltage at bit_b, hence bit_b voltage decreases. Therefore there will be discharge in the circuit and current flows. Bit and bit_b are connected to the sense amplifier, this sense amplifier acts as a comparator, so When bit' is low the output will be 1. Hence input Q=1 and we got the output as 1, read operation verified. In the same way consider Q=0 and Q'=1 in the memory. There will be a discharge in the circuit at Q and bit, since there is voltage difference. The transistors must have ratio such that Q lies below the threshold region of P2/D2. This is called read constraint. As bit voltage decreases the output will be 0.when input Q=0, the output we get is 0. Therefore in both the cases read operation is verified. Output waveforms for READ operations is shown in the below figure.3

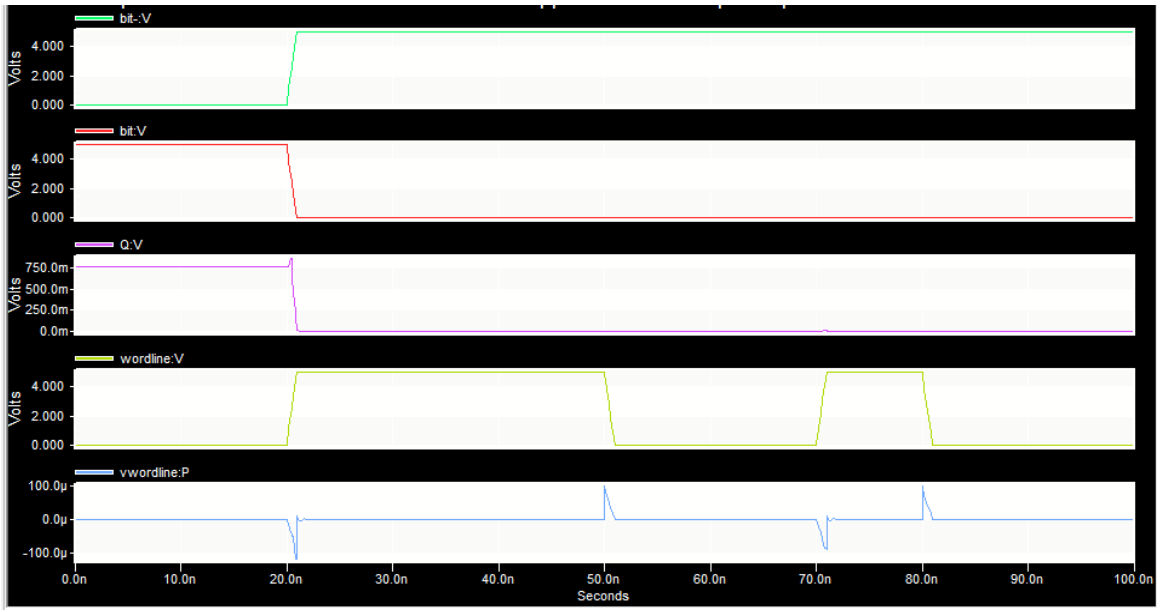

Fig.3 Read operation

1.2 Write Operation

Consider the memory bits consists of Q=0 and Q'=1. Initially word line is high and hence write operation can be performed. In the write operation bit and bit' are input lines. As we have control on the bit lines, initially make the bit_b connected to ground so that we can have the voltage difference between Q' and bit_b. To write 1 into the SRAM cell, D2 must be stronger than P2,this can be achieved by changing the aspect ratio of the transistors. Hence Q will be 1. Initially Q=0 after the operation Q=1, hence we write successfully into the memory. Output waveform is shown in Figure.4.

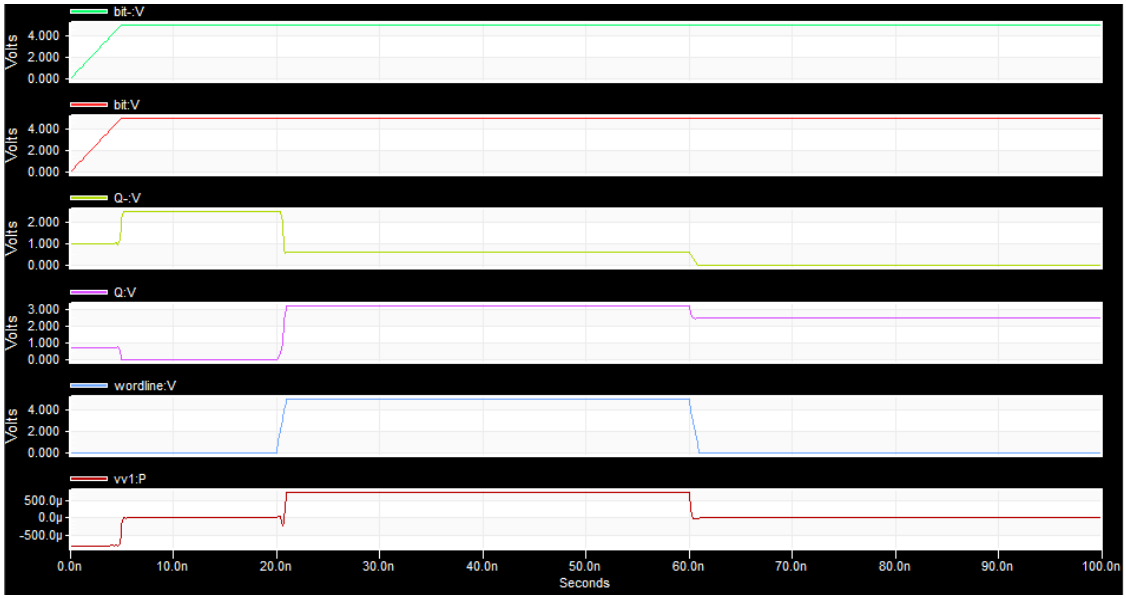

Fig.4 Writeoperation

III. Figures and Tables

The parameters used in designing the pmos and nmos transistors in 6T SRAM cell are shown in the table1 and respective READ and WRITE operation power values are shown in the table 2.

TABLE-1. Pmos and nmos parameters

Operation	Width(µm)				Length(µm)			
	P1	P2	D1	D2	P1	P2	D1	D2
READ	1.50	1.50	2.0	2.0	1.25	1.25	1.25	1.25
WRITE	1.50	1.0	1.50	1.0	0.25	0.25	0.25	0.25

Table-2. Power Values

Operation	Power	Total Time
READ	1.028720e-007 watts	2.51 Sec
WRITE	2.483478e-004 watts	2.15 Sec

IV. Design of 6t Sram In Tanner

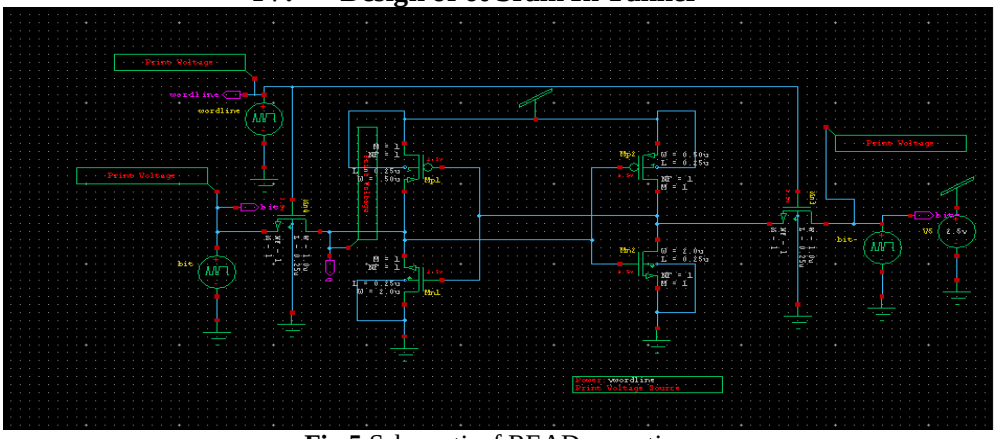

Fig.5 Schematicof READ operation

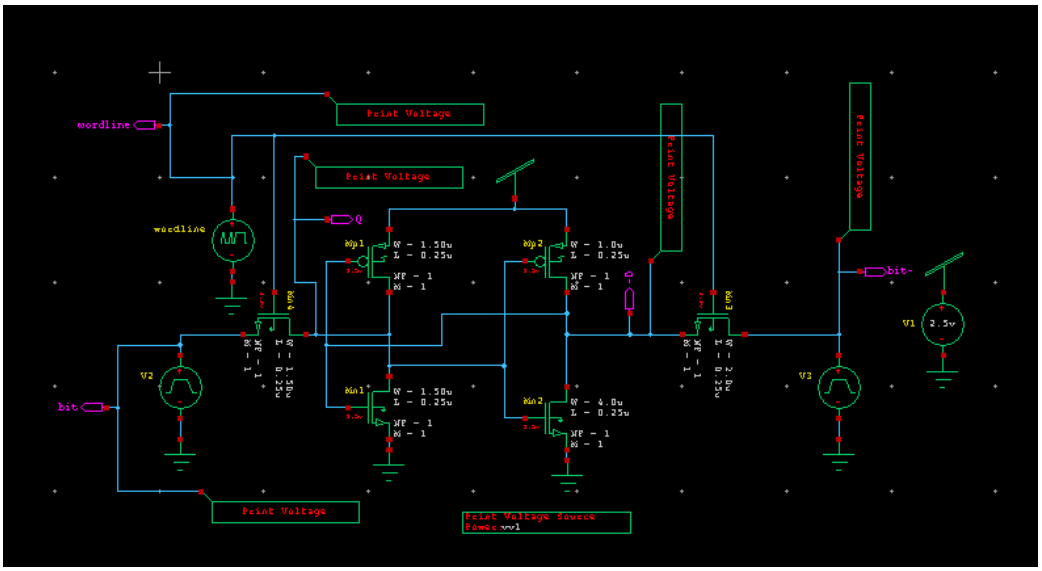

Fig.6 Schematicof WRITE operation

V. Conclusion

In our paper we have designed a basic 6T SRAM cell in which READ and WRITE operations are observed one after the other. Each operation is done using the Tanner tool in the S-EDIT. There is no need to refresh the circuit each time because the power supply is given as the bits are already stored in the memory. Also, the circuit operates at low power that is READ operation power is about 1.028720e-007 watts and WRITE operation power is about 2.483478e-004 watts.In ideal conditions, it consumes very less amount or negligible amounts of power in the circuit.

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