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Detection of Faults in SRAM Using Transient Current Testing

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Abstract: Fast development of memory devices cause more area occupation of memory in a chip and the strong market competition have increased the standards of the produced memories. The increased demand on reliability has, in turn, stressed the importance of failure analysis and device testing techniques. More and more effort and thought is being dedicated to the study of testing memory devices with regards to new fault models, fault diagnosis and new memory architectures. In order to detect these faults, March test has been widely used. However, some defects on SRAM cells may not be detected by the conventional March tests. This detection of defects in CMOS SRAM has been a time consuming process. Hence we go for current testing method. This paper implements a transient current testing (I_{DDT}) method to detect defects in CMOS SRAM cells. By monitoring a transient current pulse during a transition write operation or a read operation, defects can be detected. In order to measure the transient current pulse, a current monitoring circuit is designed.
Keywords— SRAM, memory testing, March algorithm, IDDT, Current sensor circuit.

I. INTRODUCTION

Today's systems on chips (SoCs) are moving from logic dominant chips to memory dominant devices in order to deal with today's and future application requirements. The forecast for 2013 from International Technology Roadmap for Semiconductors (ITRS) [1] [2] states that 90% of the area of SOCs will be made up of memories most specifically static random access memories (SRAMs). e. As a result, the overall SoC yield will be dominated by the memory yield. The device failure rates increase significantly with decrease in device sizes. Memory unit usually has more hardware components than other circuits and therefore is the most unreliable part. The SRAM memory cell has highest density and is more vulnerable to defects compared to other logic circuits. As the technology scales the process variations also affect the functionality of the memory.
This implies that test cost of memories will make a large impact on the test cost of the SOCs. The faults in memories result in reduction of yield. In critical systems these may cause system‘s failure. Thus adequate test methods must be employed in order to minimize the cost while maintaining efficiency thereby increasing the quality of the product. In a SRAM testing, various fault models such as stuck-at, transition, coupling faults are used. In order to detect these faults, March tests [3] [4] has been widely used. But these detection processes are time consuming. Testing using quiescent current (IDDQ) is also used [5] [6]. However, some defects in SRAM cells may not be detected using IDDQ. This project proposes a transient current testing method to detect open defects in CMOS SRAM cells. By monitoring a transient current pulse during a write operation or a read operation, faults can be detected.

II. BACKGROUND

A. SRAM Cell

Transient current testing yields higher efficiency with repeating structure. Hence this method is good for SRAM cells. The 6T CMOS SRAM [7] cell is the most widely used SRAM cell in today’s SOCs and microprocessors. Accordingly, a 6T CMOS cell, as given by Figure 1 is considered**.** It consists of two cross coupled inverters formed by transistor complementary pairs M1-M3 and M2-M4, and by two access transistors M5 and M6 that are usually NMOS transistors, which ensure read and write operations in the cell.

The writing operation of a SRAM can be classified as transition writing and non transition writing. Transition writing will cause transient current to flow from the power supply to ground. Thus if a transient current is detected during non transition write or no transient current is detected during a transition writing can confirm the presence of fault in the cell. The peak of the transient current also varies with the presence of different faults, which can be sensed to predict the occurrence of faults

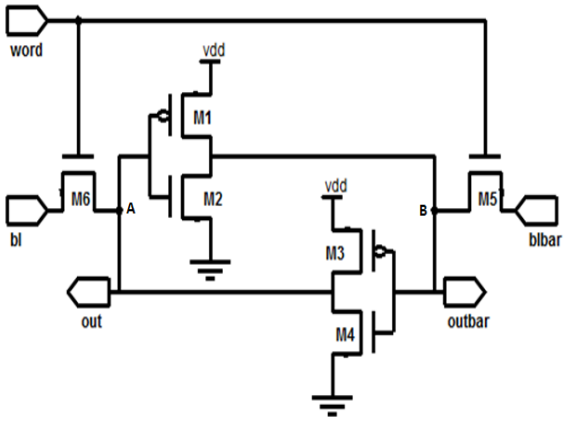

Figure 1: 6T CMOS SRAM cell

B. ***Faults introduced***

Fault occurs in SRAM due to logical or electrical design error, manufacturing defects, aging of components, or destruction of components (due to exposure to radiation) or process variations. Manufacturing defects are defects that were not intended. A manufacturing defect can occur despite of careful design.

The size of memory causes physical examination of SRAM impossible. Thus testing mechanism is based on the comparison of logical behaviour of faulty memory against good memory. To compare logical behaviour of faulty memories against good ones, modelling the physical failure mechanisms as logic fault models is required. The failure in SRAM occurs due to open and bridging faults

The study on the influence of resistive-open defects [8] [9] in the SRAM core-cell is generally made by injecting defects in the circuit itself. For simplicity, only one defect can be considered for each analysis, because the occurrence of multiple defects has a low probability in such small circuit composed of only six transistors. The defect injection in the SRAM core-cell is depicted in Figure 2. The resistive open defects are placed on the interconnections of the circuit. Due to the symmetry of the structure, these six locations allow an exhaustive analysis of the resistive-open defects within the core-cell structure.

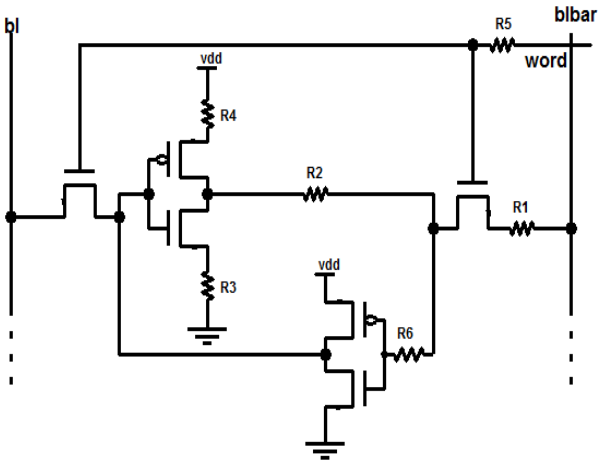

Figure 2: Open faults in SRAM

The position of the resistive-bridges [10] [11] has been chosen taking into account the actual industrial core cell layout. Each defect has been explored in a wide range of resistance values and particular conditions of supply voltage, memory size and temperature. As shown in Figure 3, five resistive-bridging defects (R7 to R11) have been placed in different locations of the core-cell. R8 to R11 have symmetrical resistive-bridges. R7 is a defect between the internal nodes of the core-cell and has no possible symmetrical defect

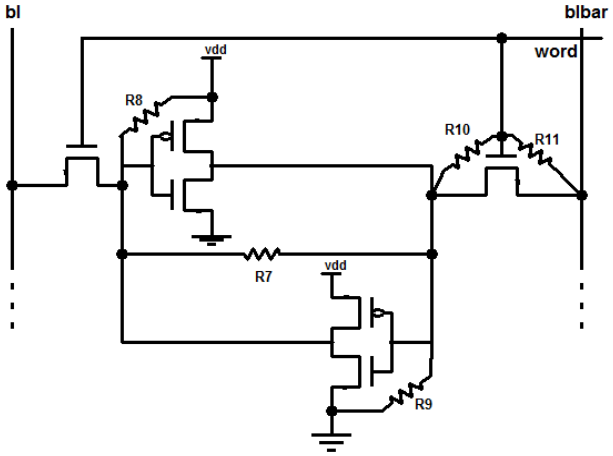

Figure 3: Bridging faults in SRAM

Bridging defects can be classified into two groups according to how they affect the working of SRAM:

Group_1: This group includes defects that may affect the behavior of the core-cell when read and/or write operations are performed on it Group_1 defects involve single-cell faulty behaviors. Group_1 includes R7, R8 and R9, as these defects may impact electric nodes within the core-cell only.

Group_2: This group includes defects affecting the behaviour of the defective core-cell and of other non-defective core-cells of the array. Defects in Group_2 may involve double-cell faulty behaviours. Group_2 includes R10 and R11 as these defects may impact BL and WL nodes. The considered simulation scheme includes the whole SRAM array and not only the single defective core-cell. In order to speed-up simulations, most of core-cells are replaced by current sources, thus modelling leakage effects.

Thus any resistances shown above can be introduced into a SRAM to make it faulty. The values of resistance used are given in Table I. It also states the nature of that particular fault.

TABLE I RESISTANCE INTRODUCED IN SRAM TO MODEL OPEN FAULTS

Resistance	**Resistance Value(Ω)**	**Nature of fault**	**Fault model**
R1	1MΩ	Open defect 1	TF
R2	1MΩ	Open defect 2	DRF
R3	1MΩ	Open defect 3	S-a-1
R4	1MΩ	Open defect 4	DRF
R5	1MΩ	Open defect 5	SOF
R6	1MΩ	Open defect 6	DRF
R7	10Ω	Bridging defect 1	SAF
R8	10Ω	Bridging defect 2	S-a-1
R9	10Ω	Bridging defect 3	S-a-0
R10	10Ω	Bridging defect 4	CF
R11	10Ω	Bridging defect 5	CF

The established logic fault models in SRAM are listed below. The model predicts five functional fault classes, stuck-at fault (SAF), transition fault (TF), stuck–open fault (SOF), coupling fault (CF) and data retention fault (DRF).

SAF: A memory cell always contains either zero or one value and fails to write the other value is considered as having a stuck-at fault. Stuck at 1 is represented as S-a-1 and stuck at 0 is represented as S-a-0.

TF: A memory cell which makes a transition '0→1' or '1→0' but fails to make a transition the other direction, is considered as having a transition fault. A transition fault is a special case of stuck–at fault.

SOF: A memory cell which is unable to be accessed is considered as having a stuck–open fault. If a cell has a SOF, neither read nor write operation to the cell is possible.

CF:A memory cell is considered as having a coupling fault if a write operation to the cell affects the contents of a neighbouring cell, or vice versa.

DRF: A memory cell which lost its content after certain period of time is considered as having a data retention fault.

III. SENSOR ARCHITECTURE

A. *VDDT Sensor*

IDDT current [12] [13] is a very fast action, it is extremely difficult to sense and process it. Mostly in low power technologies, processing the dynamic supply current is almost insoluble. Thus by transforming the

current to voltage, and then handling the resulted voltage waveform is a possible solution [14]. A VDDT sensor is shown in Figure 3. The output voltage keeps the shape of the dynamic current, but they are stretched in time. This stretch in time is useful for further processing**.** The main advantage is the speed of test, where only two write operations are required as compared to March tests, where minimum 4 operations are required to detect the fault.

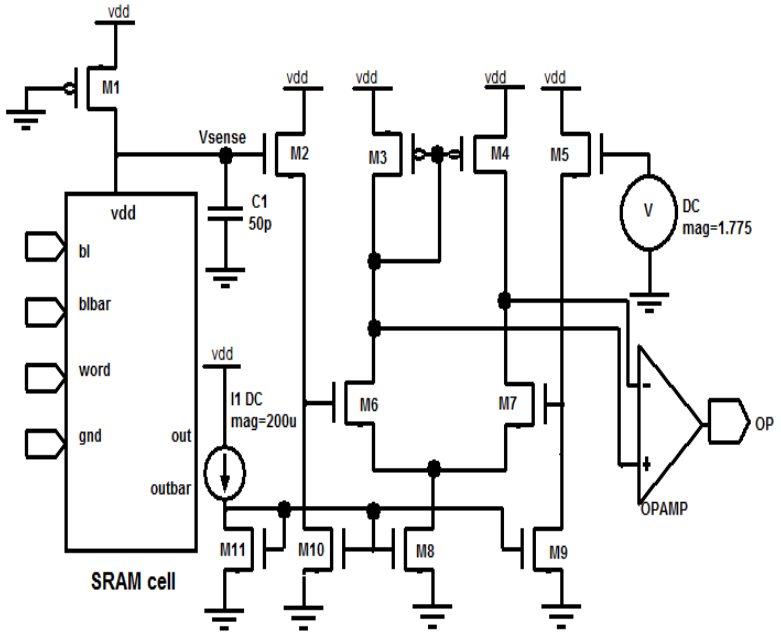

Figure 4: VDDT Sensor

M2 and M5 act as two emitter followers, which have the same DC conditions resulting from the fact, that since M1 is larger compared to transistors in the cell and that the gate of M1 is grounded, the voltage drop on it is nearly zero. Thus, the gate of M2 can be considered as connected to VDD, just like the gate of M5. Currents through M5 and M2 are also identical and hence, transistors have the same DC conditions. This way stable DC conditions are ensured on the differential pair (M6- M7) as well. The role of capacitor C is to stretch the voltage waveform in node Vsense. The main requirement for this circuitry is good device matching. Output of the differential amplifier is connected to an opamp of high gain hence the transient voltage in µV can be transformed to mVolts and Volts

A fault-free SRAM cell draws no significant supply current in a steady state, which means quasi zero static current. Substantial supply current is only driven when the cell is changing its state. Under this condition, a temporary current path is induced between the voltage supply and ground. In combination with the charging and discharging of node capacitances, it causes a current flow for the time of the switching, which is called the dynamic or transient current

This current is sensed by pmos M1. This sensed voltage is given in V(SENSE). Small spikes of µV range appears in the waveform V(SENSE). This transient voltage is sent to the differential pair. With good device matching of differential an approximately equal output is made at the output nodes. These two outputs are given to a high gain opamp. The voltage is at V range, and could be processed easily.

The testing circuitry consist of one reference VDDT sensor with good SRAM and another VDDT sensor with the SRAM under test The outputs from the both sensor is compared using the comparator. And if there is any fault in SRAM the outputs of opamps will vary due to the change in transient current change. And hence a pulse is obtained at the output of comparator. Instead of a SRAM cell an array of cells can also tested with this same circuitry.

IV. Simulation Results

A. *Sensor Output*

The transient current is sensed by pmos M1. This sensed voltage is given in V(SENSE) in Figure 5. Here spikes occur at every 50ns because a write operation is performed at every 50ns. And during the write operation transient current flows. V(OP) is the output of sensor. The transient current at every write operation is converted to voltage.

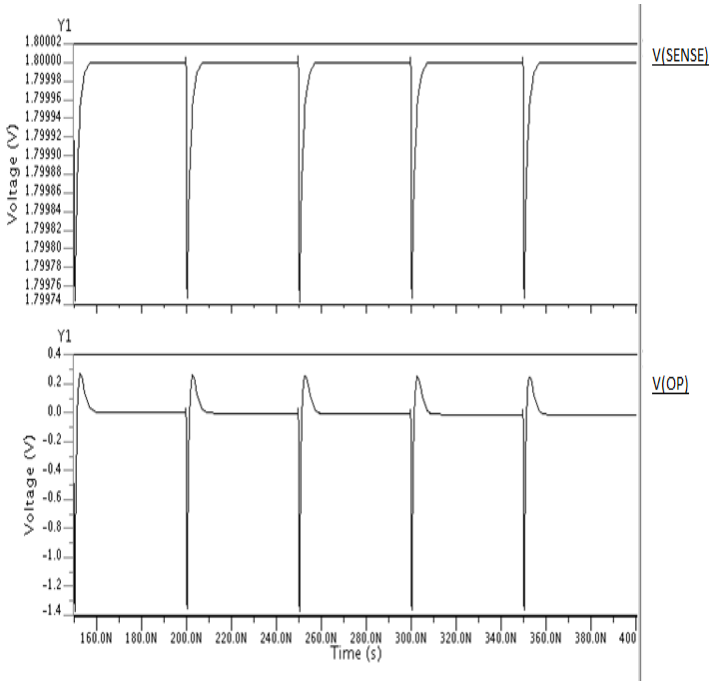

Figure 5 . Output of Vddt sensor implementation

Presence of fault in a SRAM changes the transient current flowing during a transition writing. Figure 6 shows the difference in transient current of a faulty and fault free SRAM

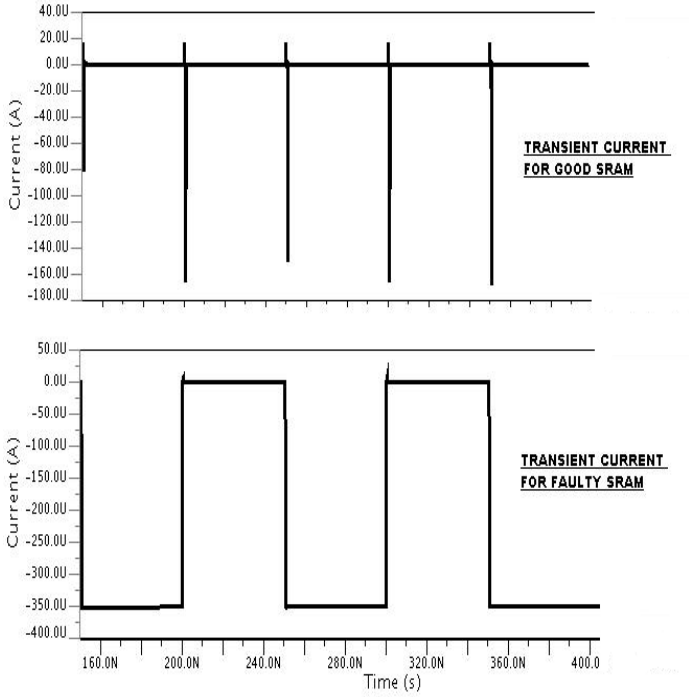

Figure 6 . Difference in transient current

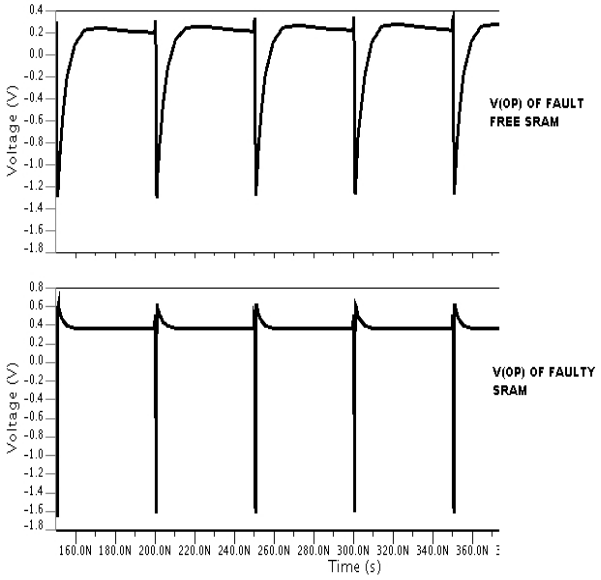

Figure 7 . Difference in V(OP)

As the transient current for faulty and fault free SRAMs vary, their VDDT sensor output also varies. This variation is depicted in Figure 7.

IV. CONCLUSIONS

In this paper a SRAM testing circuit using transient current approach for fault detection, is implemented and its effectiveness has been tested using simple memory architecture having single and multiple faults.

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