

Dissipated Power Reduction in Domino Circuit

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Abstract : In this paper we have analyzed the advantages of using dynamic circuits over static circuits with result oriented example for NAND operation. The different aspects covered under this discussion include power, speed, area, input Capacitance and timing delays calculation. We have also covered the problem of increase in dynamic power dissipation at the dynamic and the output node in dynamic circuits. A circuit is proposed for un-footed dynamic buffer circuit where the power dissipation is reduced from 256 μ W to 142 μ W at the output node in the proposed circuit as compared to that in standard dynamic domino logic buffer circuit. Simulation results are obtained using 0.12 μ m CMOS technology.

Keywords - Dynamic Circuits, Domino Logic, Keeper Circuit, Buffer, Power Dissipation, Skewed Gates

I. INTRODUCTION

Dynamic circuits are the fastest commonly used circuit family because they have lower input capacitance and no contention during switching. They have zero static power dissipation. Dynamic circuits overcome the drawbacks of both static and ratioed circuits by using clock pull-up transistor rather than PMOS that is always ON. This significantly reduces the area. We can study the operation of dynamic circuits in two modes i.e. pre-charge mode and evaluation mode. During pre-charge mode the clock is set to 'zero', so the clocked PMOS is active i.e. ON and initializes the output to high state. Whereas during evaluation mode the clock input to PMOS is set to 'one' this turn off the PMOS and the output may retain the high voltage or may be discharged to low voltage through pull-down network. Dynamic circuits however need to be taken critical care while clocking. This is the fundamental difficulty faced using dynamic circuits. This can be overcome by maintaining the input to be monotonically rising during evaluation phase i.e. the input can start LOW and maintained LOW, start LOW and go HIGH, start HIGH and remain HIGH, but cannot start HIGH and fall LOW. As the output of the dynamic gate may not be satisfying rising monotonicity therefore the output of dynamic gate cannot be directly given to the second dynamic gate connected concurrently. This monotonicity problem can be solved by placing a static CMOS inverter between dynamic gates [1]. This will convert the monotonically falling output into a monotonically rising signal suitable for next gate. The dynamic-static pair together is known as Domino gate. The static inverter is usually a HI-skew gate to favor the rising output. Dynamic circuits also suffer from the problem of charge leakage on the dynamic node. If the dynamic node is pre-charged high and then left floating, the voltage on the dynamic node will drift over time due to sub-threshold, gate, and junction leakage. Also, dynamic circuits suffer from poor input noise margin. If during the functioning of domino circuit input rises above threshold voltage while the gate is in evaluation mode, the input transistor will turn on weakly and can incorrectly discharge the output. Both junction leakage and noise margin problems can be solved by adding a Keeper circuit.

In this paper we have shown variation in different parameters of NAND gate when designed using static CMOS logic, footed dynamic logic and using un-footed dynamic logic. The remaining of the paper will discuss how the dynamic power dissipation problem in dynamic circuits and charge leakage problem in domino circuits be improved by giving an example for Low Power Dynamic Buffer [2] circuit. Also a circuit is proposed how to reduce dynamic power further. The remainder of this paper is as follows. In Section II, Parametric analysis of Basic NAND gate are described using static and dynamic circuit, in Section III, Standard Domino un-footed circuit, in Section IV, Proposed Buffer circuit, in Section V, Simulation result comparison and in Section VI is Conclusion.

II. PARAMETRIC ANALYSIS OF BASIC NAND GATE

In our analysis we will see the reduction in power consumption, area, input capacitance, rise and fall time delays by dynamic NAND circuit in against with the static CMOS NAND circuit. We will compare both the footed and un-footed dynamic NAND gate parameters with the static CMOS NAND gate. Static CMOS circuits

for basic NAND functionality with complementary n-MOS pull-down and p-MOS pull up network is shown in Fig. 1. Also the power dissipation for the static CMOS NAND circuits is shown in Fig. 2.

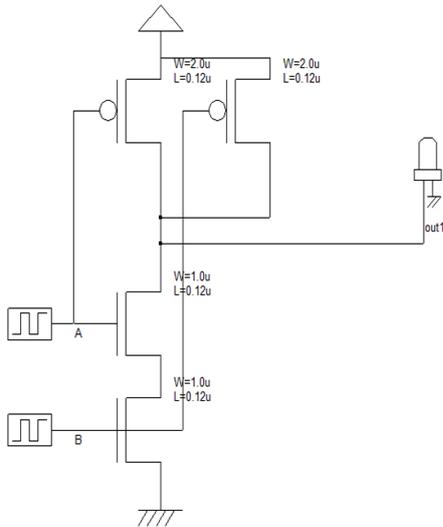


Figure1. Circuit for Static NAND gate

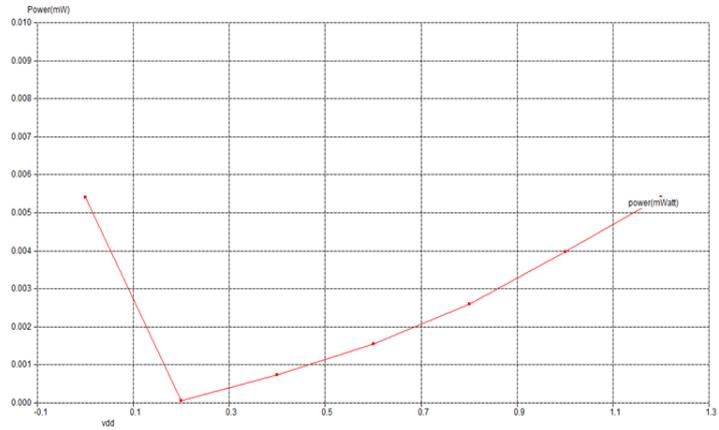


Figure2. Power dissipation in Static NAND gate

Also the same NAND functionality is obtained by Dynamic footed and un-footed circuit shown in Fig. 3.

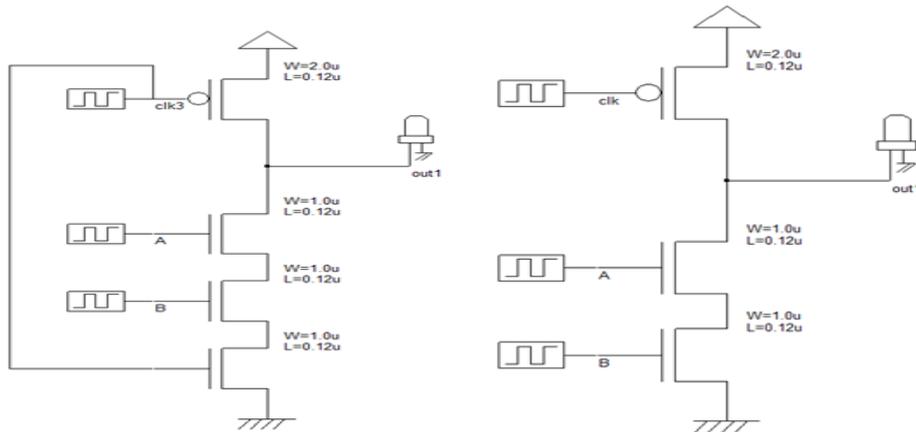


Figure3. Dynamic NAND (a) footed NAND, (b) un-footed NAND.

Thus, from the Fig. 4 Power dissipation in footed NAND gate and Fig. 5 Power dissipation in un-footed NAND gate, it is clear that power dissipation reduces from $5.286\mu\text{W}$ in static CMOS NAND circuit to $3.566\mu\text{W}$ and $3.802\mu\text{W}$ in footed and un-footed dynamic NAND circuits. Some more improved results are tabulated as under in Table1.

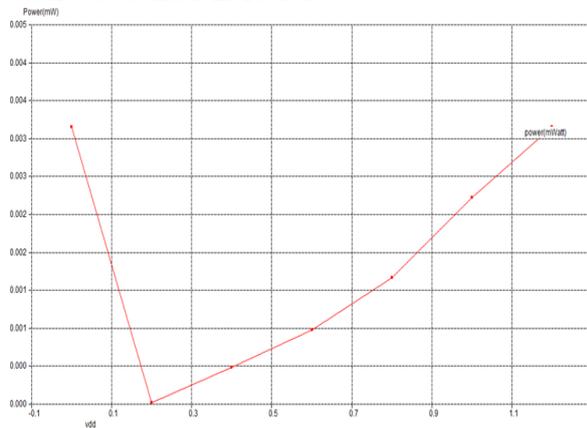


Figure4. Power dissipation in footed NAND gate

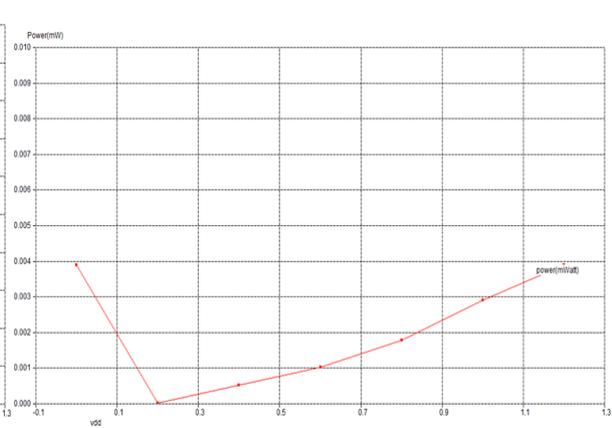


Figure5. Power dissipation in un-footed NAND gate

Table1. Parameter analysis of Static, un-footed and footed NAND gate

Parameter	Static NAND	Un-footed	Footed
Power (μ W)	5.286	3.802	3.566
Layout width/height(μ m)	11X11	8X10	9X11
Total cap. (fF)	3.02	1.92	1.79
Diffusion Capacitance (fF)	0.38fF	0.24fF	0.23fF
Fall Delay (ns)	0.002	0.001	0.001
Resistance (Ω)	858	559	535
Inductance (nH)	0.03	0.00	0.00

III. STANDARD DOMINO UN-FOOTED BUFFER CIRCUIT

The standard Domino un-footed buffer circuit is shown in Figure6. Standard Domino un-footed buffer circuit. The operation of this circuit can be divided into two phases as shown in the timing diagram Figure7. Voltage V/s. Timing Diagram. First, when input is LOW, the NMOS is OFF. Thus, the dynamic node is at high voltage during precharge because PMOS is ON. The dynamic node also maintains near to high voltage during evaluation as there is no path for discharging. Thus, throughout giving fixed zero output in this phase.

Second, when the input is high and the clock input is zero i.e. during precharge, PMOS is ON and the dynamic node has high voltage resulting in zero output. Whereas during evaluation, PMOS is OFF, thus dynamic node is at LOW voltage which results in HIGH output. Here propagation of precharge pulse is needed at the dynamic node and prevented at the output node to make the circuit stable. This redundant switching increases the power consumption.

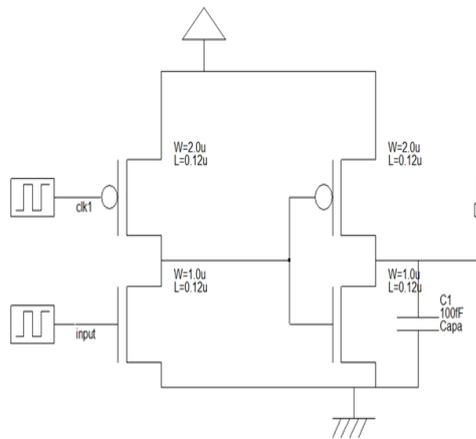


Figure6. Standard Domino unfooted buffer circuit

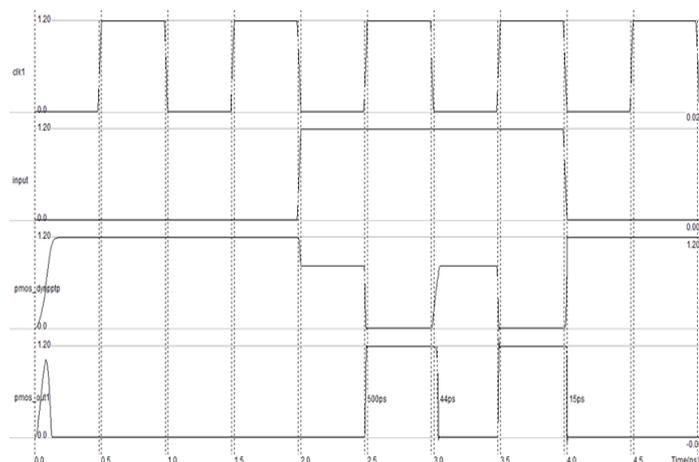


Figure7. Voltage Vs. timing diagram

IV. PROPOSED BUFFER CIRCUIT

The proposed circuit 1 for the standard domino buffer circuit is shown in Figure8 Proposed circuit 1. Here we have used a conditional pulse generator using NAND gate. The inputs of three input NAND gate are clock, delayed clock and output feedback. The NAND gate gives LOW output only when all the inputs to it are HIGH. Thus, turning PMOS pull-up transistor active. Considering two cases, first when the input is LOW, dynamic node holds high voltage if or not PMOS is active. Thus, making output to be LOW. Second, when the input is HIGH and output of NAND is HIGH, the dynamic node is LOW pulling output HIGH. On the other hand, if input is still HIGH and output of NAND is LOW. In this case contention current flows and the width of pull-down transistor is sufficient to take the dynamic node to LOW voltage. Thus giving HIGH output.

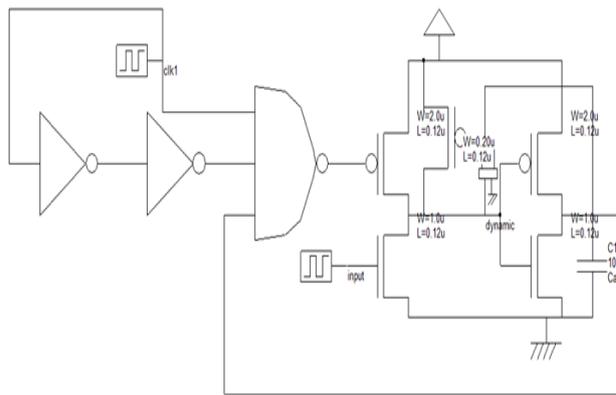


Figure8. Proposed circuit 1.

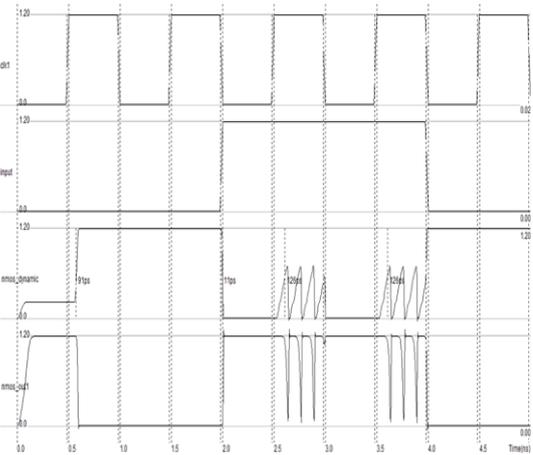


Figure9. Voltage vs. timing diagram

The above Figure9. Voltage vs. timing diagram shows timing behavior of the clock, input, dynamic node voltage and NMOS output voltage with respect to time. As it can be analyzed from the above timing diagram the output exhibits fluctuation when the input is hold HIGH and the clock input is also HIGH voltage.

This fluctuation can be removed by converting the output inverter to HI-skew circuit by reducing the n-MOS width to 0.2μm and input inverter circuit to LO-skew by reducing the width of p-MOS to half of the original. Doing this LO-skew inverter will keep the dynamic node near to zero voltage. Thus, it will make p-MOS in second inverter (HI-skewed) to ON faster, resulting in keeping output of the buffer to constant HIGH voltage. Thus, removing fluctuation in the voltage at the output node which in result reduces power dissipation at both the dynamic and the output node. The schematic of the proposed dynamic circuit 2 is shown below in Figure10. Proposed circuit 2.

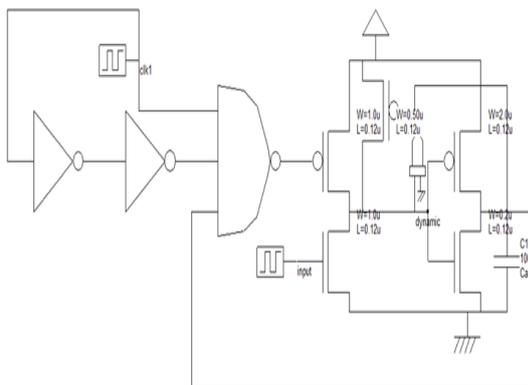


Figure10. Proposed circuit 2.

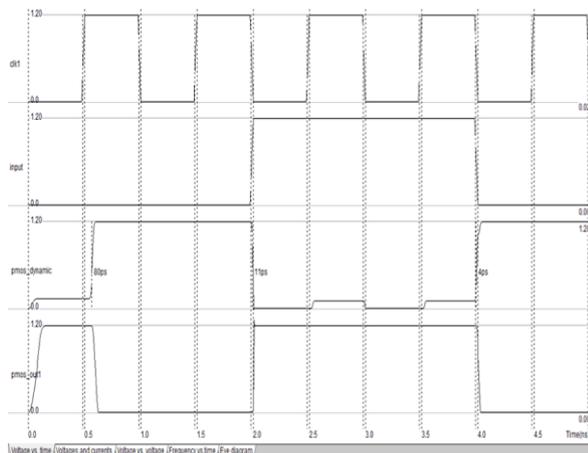


Figure11. Voltage vs. timing diagram.

The output waveform for the proposed circuit 2 is shown below in Figure11. Voltage Vs. timing diagram. It is observed that the output maintains the constant HIGH voltage without any variation when the input to the circuit is HIGH. Thus giving stable output compared to Proposed Circuit 1.

V. SIMULATION RESULTS

The schematic of all circuits are made using DSCH 2.7F and simulation is done on Microwind 2.6K. The foundry used is CMOS 0.12μm-6 Metal. The result below shows the variation of Power dissipation of all the three circuits for given supply voltage. The voltage V_{dd} and discharge capacitance is kept constant for all three circuits to 1.2V and 100fF. It is clear from the results that power dissipation reduces in the proposed circuit as compared to the standard circuit. As can be observed from the Fig.12 power increases with increase in supply voltage. As the results are simulated using 1.2V supply voltage, we can observe the decrease in power dissipation for the proposed circuit with the same supply voltage. The Power dissipation plots for both the proposed circuits are shown in Fig.13 and Fig. 14.

In addition to reduction in power dissipated, the proposed circuit also reduces diffusion capacitance from 0.24fF in standard circuit to 0.18fF in proposed circuit 2. This results in improving parasitic delay of the buffer circuit. The layout of the standard dynamic and the proposed circuits are implemented in Microwind 2.6K using

0.12 μ m CMOS technology. The clock and the input time period were set to 5ns and 10ns respectively. The load at the output was set to 100fF.

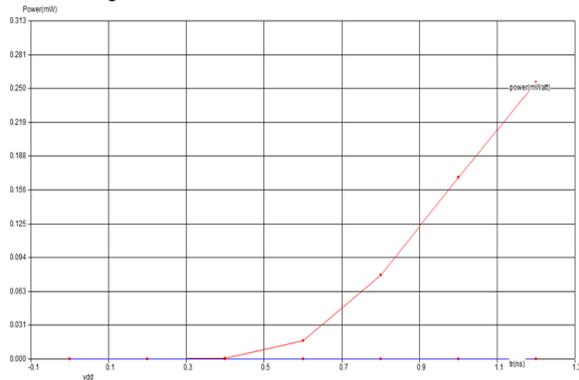


Figure12. Power dissipation in standard circuit

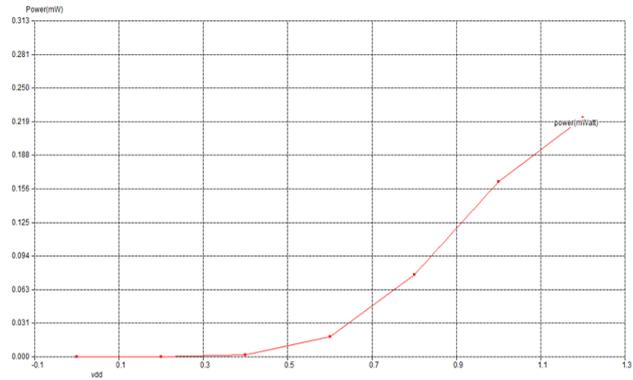


Figure13. Power dissipation in proposed circuit 1

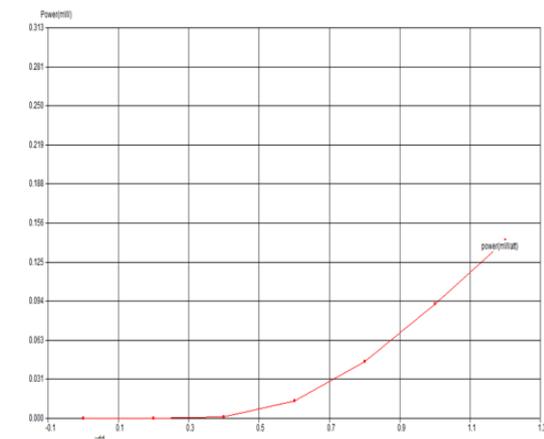


Figure14. Power dissipation in proposed circuit 2

Table2. Power dissipation in standard and proposed circuits

V _{dd} (V)	Power Dissipated in (mW)		
	Standard circuit	Proposed Circuit 1	Proposed Circuit 2
0.00	0.000	0.000	0.000
0.20	0.000	0.000	0.000
0.40	0.001	0.002	0.001
0.60	0.017	0.019	0.014
0.80	0.077	0.076	0.046
1.00	0.168	0.163	0.091
1.20	0.256	0.222	0.142

VI. CONCLUSION

In this paper a two new proposed circuit is designed. The difference in this circuit is the additional pulse generator gated circuit and the HI-skew and Lo-skew gated inverters. The pulse generator avoids the precharge pulse to propagate at the output node. And the skewed gates make charging and discharging of the dynamic node and the output node faster. The simulation of the standard and the proposed circuit is done on using Level-3, 0.12 μ m CMOS technology. This proposed circuit reduces the power dissipation at the output node. For the load capacitance of 100fF the proposed circuit reduces the power dissipated by 16.36% and 44.53% in proposed circuit 1 and proposed circuit 2 respectively. Also reduces the diffusion capacitance in proposed circuit 2 by 25%.

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