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An Efficient Viterbi Decoder Architecture

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Abstract: *A breadth first trellis decoding algorithm is introduced for application to sequence estimation in digital transmission. The decoding effort adapts to the prevailing noise conditions to yield low average effort. The proposed method of a performance of error correcting in noisy channels to reduce the power dissipation, the decoding speed in much to design a VD for TCM is presented in this paper. VD is used to decode the digital data communications and storage devices without any performance loss. A viterbi decoder uses the viterbi algorithm for decoding a bit stream that has been encoded using Forward error correction based on a code There are other algorithms for decoding a convolutionally encoded stream as well as punctured codes The advandage of VD is errors and correction and digital communication. The pre computation VD could reduce the power consumption by 70% with only 11% reduction of the maximum decoding speed.*

Keywords- *Convolution codes, Trellis coded modulation(TCM), Threshold,Viterbi decoder , VLSI.*

I. Introduction

Viterbi algorithm is a well-known maximum-likehood algorithm for decoding of convolution codes. The approach is suitable both for hardware and software. Convolution codes are used to correct errors in noisy channels. The redundant information is the users data and then correcting errors using this informations are given in section– II. The trellis coded modulation is many bandwidth of high rating of convolutional code.The viterbi decoder for the TCM decoder is a Constraint length of the code moderate.It uses the deep space communication for reducing the power supply voltages ove rscaling or not The encoder generates the two output code word bits as a function of the input information bits and the encoder state. The output bits are transmitted over a nosy channel. The encoder state evolution and the decoding processes can be represented by the trellis encodingstates are discussed in section III.

The incoming channel to the branch metrics unit is the combined signal. It is convolutional to correct the errors in noise .The convolutional encoder for shift register performs the serial and parallel states to scares state transistion in limited code. The punctured code is performed the decoding should ignore the erased bits during lower correction in branch metric calculations. The branch metrics units are discussed in section IV-4.1.

The high rate of bit error in metrics to ACSU is estimated by the inherent drifting error between path metrics and accurate measurement shifting. the efficient clock speed of a VD for critical path is rotated by synchronize clock cycles. The set (or) reset of a data is information of next stages to the input of a shift keying.BMs are fed into the ACSU that recursively computes the PMs and outputs decision bits for each possible state transition. After that the decision bits for stored in and retrieved from the SMU in order to decode the source bits along the final survivor path. The Pms of he current iteration are stored in the PMU. The ACSU loop for calculating the optimal PM and puncturing states are discussed in section IV-4.2.

The adaptive decoder discards some states with high path metrics dynamically during the decoding process. The use of a scarce state transition scheme for the multimedia mobile communication. The scheme employs simple pre decoder followed by a pre encoder to minimize signal transitions at the input of a convolutional , which leads to lower dynamic power dissipation. The decision bits are allowed to pass through the state metric unit. The decoding process is done of the pre-encoding to convert the decoded output. The register exchange method & the trace back method needs to move the data in memories for every cycle to do implementation of SMU is discussed in section IV-4.3.

II. Viterbi Decoder

A Viterbi decoder uses the Viterbi algorithm for the decoding a bit stream that has been encoded using Forward error correction based on a code. A conventional Viterbi decoder contains three major parts. A Branch Metric Unit-BMU which calculates the branch metrics; An Add-compare-Select Unit -ACUS which recursively7 accumulates the branch metrics as the path metrics (PM), compares the incoming path metrics, and makes a decision to select the most likely state transitions for each state of the trellis and generates the corresponding decision bits [1].

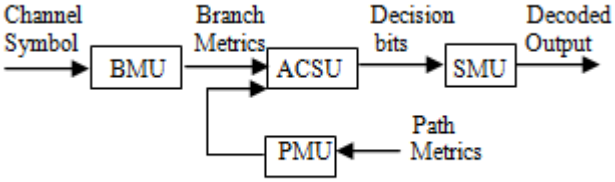

Fig. 1 Functional diagram of a viterbi decoder

A survivor memory unit-SMU, which stores the decision bits and helps to generate the decoded output. Among these three units, the ACSU and SMU consume most of the power of the decoder. There are two known methods for the implementation of the SMU, namely the Register Ex-change method(RE) and the Trace Back (TB) method. In general, Re has the advantage of high speed, low latency, and simple control but it consumes more power than the Trace (TB) mechanism since it needs to move the data among the memories in every cycle. Therefore, the TB mechanism is commonly used for the implementation of the SMU [3].

III. Viterbi Decoder Algorithm

The Convolutional encoder adds redundancy to the input signal and the encoded output symbols are transmitted over a noisy channel. The input of the Convolutional decoder that is the input for the Viterbi decoder is the encoded symbols contaminated by noise. Then the decoder tries to extract the original information from the received sequence and generates an estimate. The path in the trellis for the channel output r is the one that maximizes the function. This is called the metrics in branches of the encoded data. In $[Pr(r/x_m)]$ is the functions of metrics in the decoder. Moreover finding the trellis with the largest function corresponds to the maximum decoding. The Hamming distance between the trellis code word and the received sequence is a constraint length[3].

3.1 BMU Calculation

Methods of branch metric calculation are different for hard decision and soft decision decoders. For a hard decision decoder as branch metric is a Hamming distance between the received pair of bits and the ideal pair therefore a branch metric can take values of 0,1 and 2. Thus for every input pair we have 4 branch metrics. For a soft decision decoder, a branch metric is measured using the Euclidean distance let x be the first received bit in the pair, y-the second, x_0 and y_0- the ideal values. Then branch metric is in Equation 1

$$M_b = (x - x_0)^2 + (y - y_o)^2 \quad (1)$$

$$M_b = (x^2 - 2x\,x_0 + x^2_0) + (y^2\ 2\text{-}y\,y_o + y_o^2) \quad (2)$$

$$M^*_b = M_b x^2 - y^2 = (x^2_0 - 2\,x\,x_0) + (y^2_0 - 2y\,y_0) \quad (3)$$

Note that the second formula, M^*_b, can be calculated without hardware multiplication x_0^2 y_0^2 can be pre-calculated, and multiplication x by x_0 and y by y_0 in equation 2 &3. M^*_b is signed variable is calculated in 2's complement format[3].

3.2 ASCU Calculation

The optimal choice for the convolutional encoder to correct the lower noise in puncturing and the serial and parallel states of the transition metrics from branch metrics. The 64 states and PMs are labeled from 0to 63.the minimum value of each BM group can be calculated in BMU and the threshold Generator to calculate (PM_{opt} +T) and the functions of synchronize speed is calculated through ACSU[1].

$PM_{opt}(n)$=
Min[min[min(cluster0(n-2))+ min (BM G0(n-1));
Min[min[min(cluster1(n-2))+ min (BM G1(n-1));
Min[min[min(cluster2(n-2))+ min (BM G2(n-1));
Min[min[min(cluster3(n-2))+ min (BM G3(n-1));

3.3. Path Metric Calculation

Path metrics are calculated using a procedure called ACS. This procedure is repeated for every encoder state. There are two ways of dealing with this problem. Since the absolute values of path metric don't actually matter, we can at any time subtract an identical value from the metric of ever path. It is usually done when all path metrics exceed a chosen threshold. This method is simple, but not very efficient when implemented in hardware. The second approach allows overflow, but used a sufficient number of bits to be able to detect

whether the flow took place or not. The compare, select. have two paths, ending a given state. As these are 2^{k-1} encoder states in a survivor paths at any given time[7].

3.4 SMU Calculation

The decoded data is based on the 64 to 6 priority encoder based on three 4 to 2 priority encoders. The encoders will determine the index [1:0] the MUX2 select one group of flags based on index[1:0] input of the priority encoder at level 2 can be computed from the output of MUX2 by OR operations[1].

IV. Low –Power High Speed Viterbi Decoder Design

4.1 BMU Design

The BM module generates branch metric for ACS module in terms of the received channel symbols. It provides branch information for branch metric computation, in terms of constraint length selection The channel symbol comes to BMU performing Convolutional codes in it. The incoming channels have a noisy, cc is used to correct the errors in noisy. The number of rows in a puncturing matrix is equal to the number of output polynomials. The elements of this matrix are 1's. The puncturing matrix is applied to the output stream. This is done in BMU to correct a low capable errors[7]. The serial bits stre3am in BMU is doing by shift registers. The output from the registers cell is Polynomial in constraint length[10].

4.2 ACSU Design

The ACSU so that it can be operated at reduced supply voltage. The ACSU loop for calculating the optimal PM and puncturing states. In order to evaluate of process variations on the BER, the delay distributions of various metrics found in the ACSU. The rotate synchronize BER is used to speed up the VD into a synchronizing clock frequencies. The enable signal is activated during the one clock period at the end of the frame clock pluses for synchronizing[1].

Each state in the trellis of Viterbi decoding, current path metrics are obtained from current branch metric and path metrics of the previous states, which lead to current state, by executing addition, comparison and selection operators to speed up this module. The first architecture is based on permitting limited decision errors in order to decrease the critical path delay of the ACSU so that is can be operated at reduced supply voltage[3].

4.3 SMU DESIGN

The two, methods are namely the register EX-change method(RE) and the trace back (TB). In general, Re has the advantage of high speed , low latency, and simple control but it consumes more power than the trace(TB) mechanism since it needs to move the data among the memories in every cycle[1].

The addition, best metrics of the branches to select the decision bits to convert the encoder to decoder. The conversion is required to synchronize clock pulses the output decoded bits are coming from SMU.A register is assigned to each state, and the length of a register is equal to the frame length in decoder. The corrected output sequence is produced by tracing the decision vectors. The trace back module is used to decide the final output. Viterbi decoder in trace back approach, it saves about 68.82% of power compared with conventional Viterbi decoder[3].

Table 1. Area power dissipation and speed comparison of proposed method,

Type	Cell area(mm^2)	Power dissipation in mw	Speed of operation in MHZ
Full-trellis VD	0.58	21.473(100%)	505
Conventional T-Algorithm	0.685	20.91	232
VD with 2 step pre computation	0.68	20.069	446.4

V. Simulation Results

The full trellis VD is used for VHDL coding to implement the output & input datas using xilinx 9.2 version. The serial state transitions & punctured polynomials in the branch metrics calculations are shown in Fig. 1 & 2. In ACSU, to evaluate the BER performance for incoming branch metrics for normalizations of a signal to pass through the ACSU to select the decision bits in different path metrics are shown in Fig.3. The synchronize the clock speed of the encoding error rate as shown in Fig. 4.

The decision bits are encoded from the different path to choose the ACSU finally the decoded process output in SMU is coming from the decoding of Viterbi decoder.

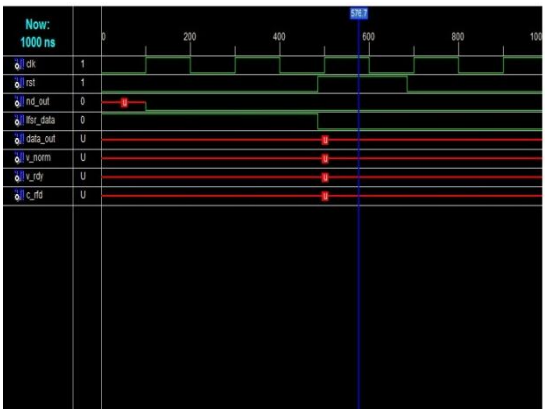

Fig.1 Serial bits in BMU

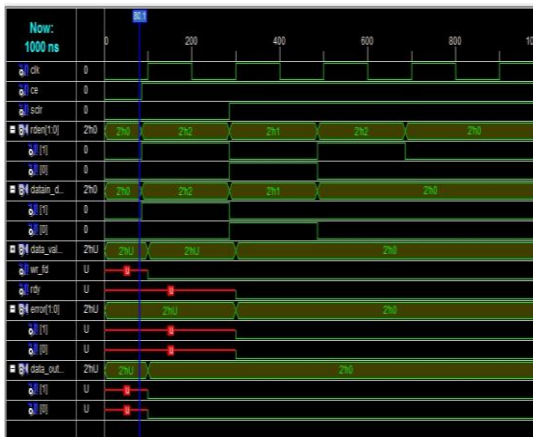

Fig.2 Punctured Codes

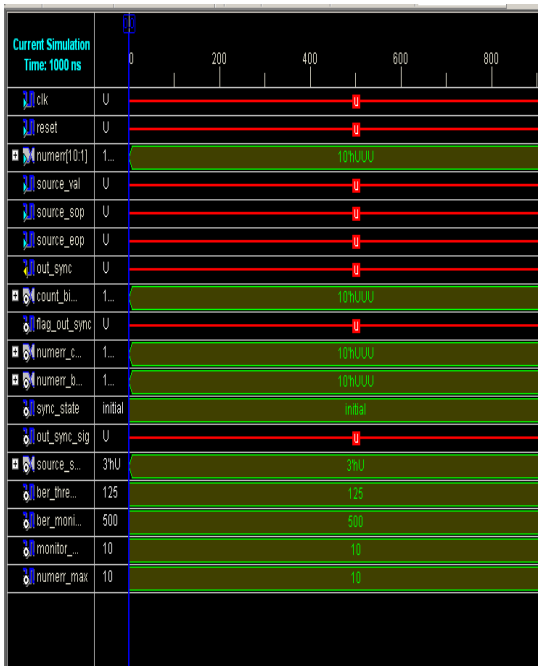

Fig. 3 VD BER threshold in acsuthe bit error rate in acsu is calculated by the matrices of BER threshold.

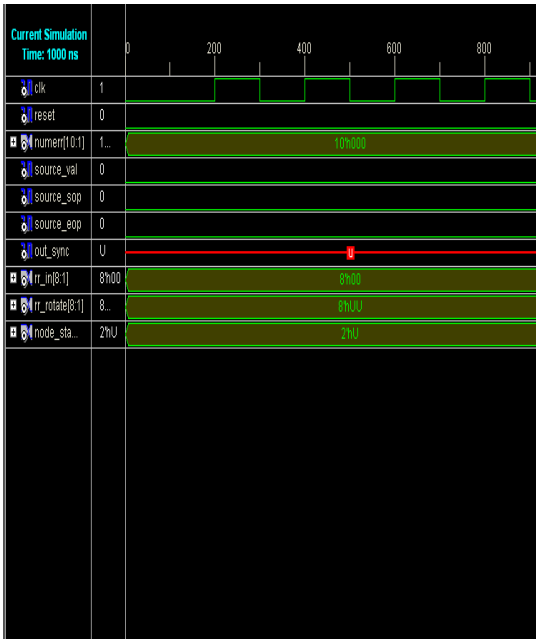

Fig. 4 Rotate synchronize clock speed in path metrics to ACSU

VI. Conclusion

A design starts with the development of a behavioral VDHL description. if the target throughput is moderately high, the proposed architecture can operate at a lower supply voltage, which will lead to quadratic power reduction compared to the conventional scheme. ASIC synthesis and power estimation results show that, compared with the full trellis VD without a low-power scheme, the pre-computation VD could reduce the power consumption by 70% with only 11% reduction of the maximum decoding speed . The use of error-correcting codes

has proven to be an effective way to overcome data corruption in digital communication channels. The error in channel symbols are reduced by VD, it makes to design for future to less correction coding error bits. The purpose is to avoid the over scaling to reduce the speed & noise in data. The best metrics of encoded bit streams are filtered noise fully in the trellis coded modulation. The fuzzy logic of decision bits are avoid the un encoded the puncturing states to improve a performance of execution speed for low supply dissipations.

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