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Charge Pump, Loop Filter and VCO for Phase Lock Loop Using 0.18µm CMOS Technology

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Abstract : *This paper presents a Low power charge pump, second order low pass filter and voltage controlled oscillator for low power phase lock loop. The paper contains the detailed circuit diagram of charge pump, loop filter and voltage control oscillator with 1.8v power supply. The design has been realized using 0.18um CMOS technology. Here current starved voltage control oscillator is use for phase lock loop.*
Keywords: - *charge pump, second order low pass filter, voltage control oscillator*

I. INTRODUCTION

Digital Phase locked loop (PLL) is one of the most inevitable necessities in modern day electronic systems. It finds widespread applications in generation and synchronization of well timed clocks ,recovery of signal from noisy communication channel, FPGA,,s, communication systems, frequency-synthesizer, trans-receivers. Since a PLL can be incorporated in a single chip, it is highly preferred. low power DPLL is becoming essential for portable and battery operated compact electronics device, which decreases the risk of reliability problems. The Phase Lock Loop plays the versatile roles in the application of clock generation, time synchronization and clock multiplication. A basic block diagram of PLL is introduced in Fig 1. It consist five main blocks

1) Phase Frequency Detector (PFD)
2) Charge Pump (CP)
3) Low Pass Filter
4) Voltage Controlled Oscillator (VCO)
5) Divided by N Counter.

In this paper improve the circuit of charge pump, loop filter, current starved VCO. The paper is organized as follows, Section II contains charge pump, Section III second order low pass filter and Section VI Voltage Controlled Oscillator.

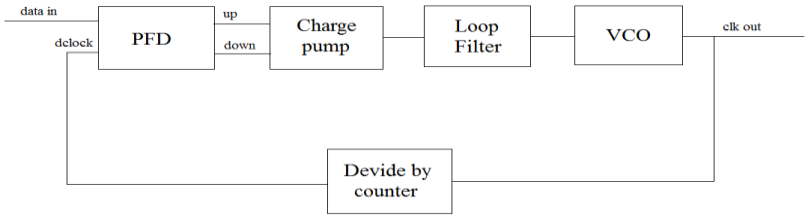

Fig 1 A Basic Block Diagram of Phase Locked Loop [1]

II. CHARGE PUMP

Charge pump is the next block to the phase frequency detector. The output signals - UP signal and DOWN signal generated by the PFD is directly connected to the charge pump. The main purpose of a charge pump is to convert the logic states of the phase frequency detector into analog signals suitable to control the voltage-controlled oscillator (VCO). Basically, the charge pump consists of current sources and switches. The output of the charge pump is connected to a low pass filter that integrates the charge pump output current to an equivalent VCO control voltage (Vcntl). Three states in the charge pump correspond to its output to the loop filter:

State 1: Charging current: +ICP
State 2: Discharging current: -ICP
State 3: Zero current

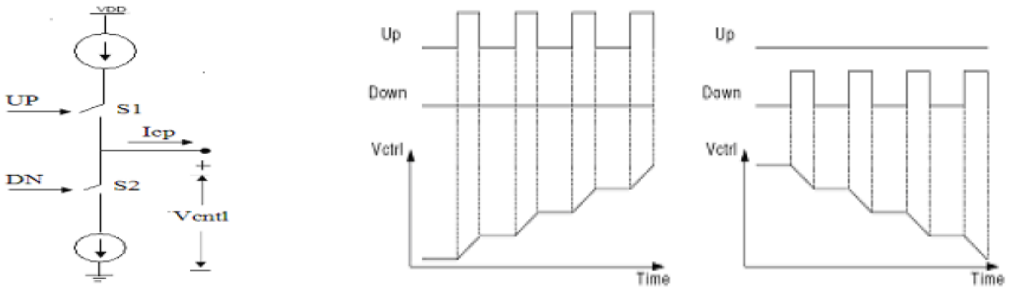

Fig 2 Basic block diagram of Charge Pump with Ideal Behavior [1]

The overall operation of the charge pump can be observed in Fig. 3, which is the ideal behavior of the charge pump. It shows both the conditions of the charge pump. It charges or discharges the current of the charge pump related to the value of the error signal (pulse width of the UP signal or DOWN signal) generated by the PFD.

Table No.1 Operation of Ideal Charge Pump[1]

UP signal	DN signal	Condition	Note
1	0	Charging	Icp flows into filter
0	1	Discharging	Icp flows out from filter
0	0	Vout constant	Icp = 0
1	1	Vout Constant	Icp = not 0

In Fig. 4 seen the CMOS Circuit of Charge pump that i have selected. Fig. 5 is waveform of charge pump, and Fig. 6 is waveform of charge pump when they are connected with PFD.

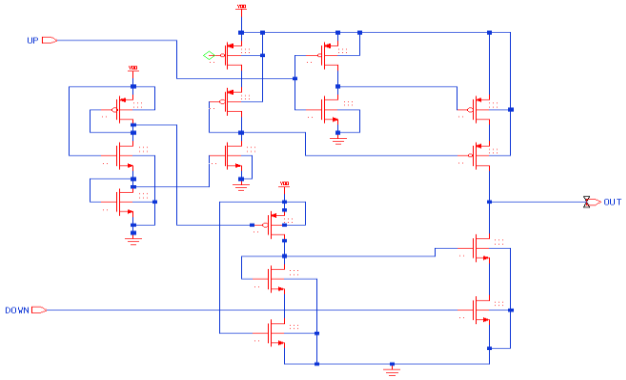

Fig. 3 CMOS circuit of Charge Pump [4]

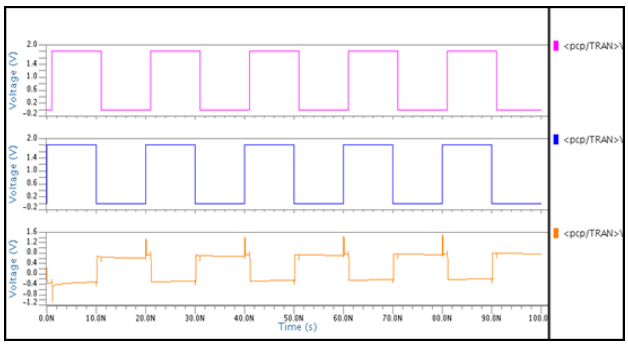

Fig. 4 Waveform of Charge Pump

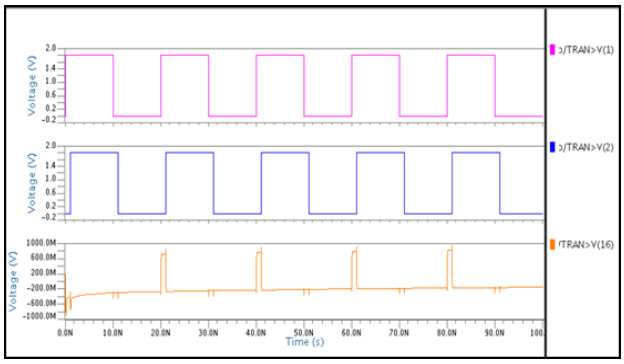

Fig. 5 Waveform of Charge Pump with PFD

III. LOOP FILTER

The loop filter is the heart of PLL. It is inevitable to choose the loop filter values correctly, as inappropriate values may either lead the loop to oscillate for long without reaching the locked state or it may so happen that once locked, small variations in the input data may cause the loop to unlock. A second order low pass filter is used as loop filter. The main function of the loop filter is to convert the current coming from charge pump to control voltage that is directly connected to VCO to control the frequency of VCO. The inclusion of a loop filter at the output of the charge pump serves two functions.

The second-order loop filter has the second capacitor to smooth out current spikes. This type of filter has two poles one at low frequency and one have high frequency and a zero which will add the stability of the system. The passive low pass loop filter is used to convert back the charge pump current into the voltage. The output voltage of the loop filter controls the oscillation frequency of the VCO. The loop filter voltage will increase if DCLOCK leads DATA and will decrease if DATA leads DCLOCK. If the PLL is in locked state it maintains a constant value.

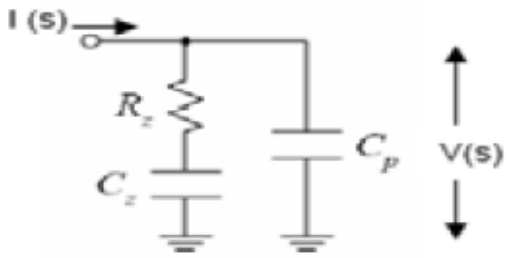

Fig. 6 Second order loop filter. [2]

Total simulation from phase frequency detector to loop filter is shown in figure 7 and value of loop filter is shown in figure 8 .

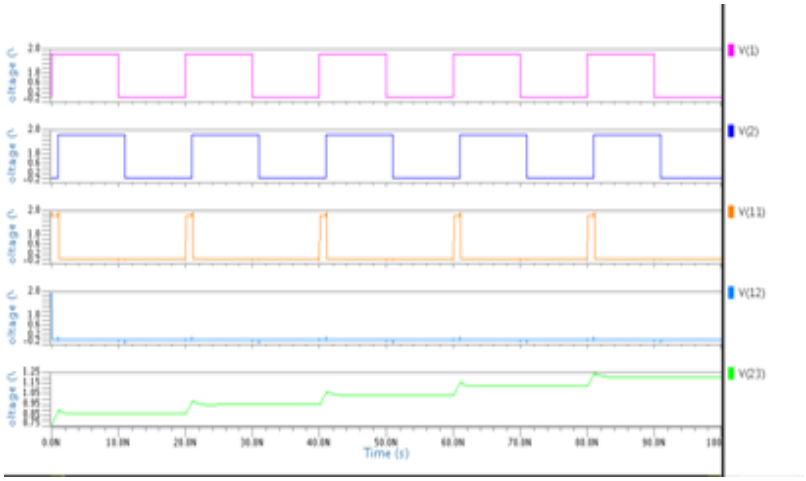

Fig. 7 simulation from phase frequency detector to loop filter at 50MHz

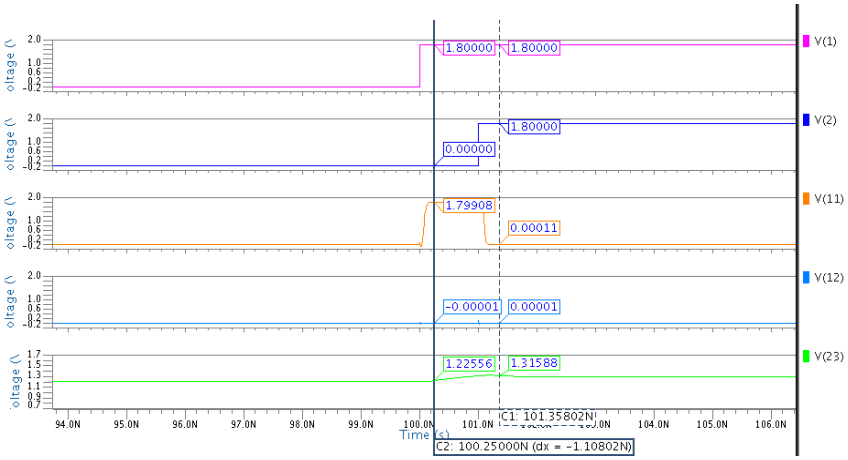

Fig. 8 90mV value of loop filter at 50MHz

IV. VOLTAGE CONTROLLED OSCILLATOR

An oscillator is an independent system that generates a periodic output without any input signal. A voltage controlled oscillator is an electronic oscillator designed such that its oscillation frequency is controlled by a voltage input.

The current-starved VCO is shown schematically in figure 9. Its operation is similar to the ring oscillator. MOSFETs M44 and M45 operate as an inverter, while MOSFETs M39 and M34 operate as current sources. The current sources M39 and M34 limit the current available to the inverter M44 and M45 ; in other word , the inverter is starved for current. The MOSFETs M32 and M33 drain currents are the same and are set by the input control voltage. The currents in M32 and M33 are mirrored in each inverter/current source stage. An important property of the VCO used is the input impedance. The filter configuration we have discussed rely on the fact that the input resistance of the VCO is practically infinite and the input capacitance is small compared to the capacitances present in the loop filter.

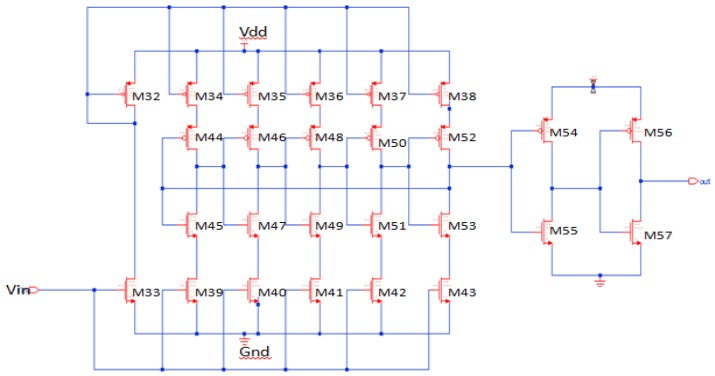

Fig. 9 Current starved VCO [2]

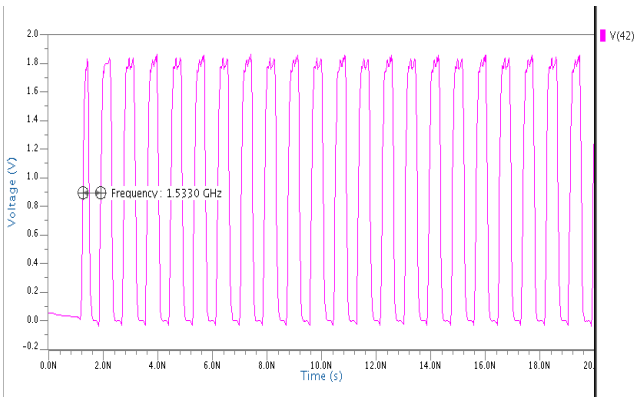

Fig. 10 Simulation result of VCO at 90mV input voltage

Table No.2 VCO Result

Vdd	1.8 V
Input Voltage	90 mV
Technology	180 nm
Output Frequency	1.53 Ghz

In fig. 10 the simulation result of current starved VCO and output frequency is 1.533 GHz.

V. CONCLUSION

A PLL is a closed loop system that locks the phase of its output signal to an input reference signal. This thesis is based on the clock generation application. This paper is presented a PLL with better designed in CMOS 0.18µm technology. The goal of this paper is to achieve more than 1GHz and successfully achieved 1.53GHz frequency.

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