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Open-Source 32-Bit RISC Soft-Core Processors

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Abstract: *A soft-core processor build using a Field-Programmable Gate Array (FPGA)'s general-purpose logic represents an embedded processor commonly used for implementation. In a large number of applications; soft-core processors play a vital role due to their ease of usage. Soft-core processors are more advantageous than their hard-core counterparts due to their reduced cost, flexibility, platform independence and greater immunity to obsolescence. This paper presents a survey of a considerable number of soft core processors available from the open-source communities. Some real world applications of these soft-core processors are also discussed followed by the comparison of their several features and characteristics. The increasing popularity of these soft-core processors will inevitably lead to more widespread usage in embedded system design. This is due to the number of significant advantages that soft-core processors hold over their hard-core counterparts.*

Keywords: *Field-Programmable Gate Array (FPGA), Application-Specific Integrated Circuit (ASIC), open-source, soft-core processors.*

I. INTRODUCTION

Field-Programmable Gate Array (FPGA) has grown in capacity and performance, and is now one of the main implementation fabrics for designs, particularly where the products do not demand for custom integrated circuits. And in recent past due to the increased capacity and falling cost of the FPGA's relatively fast and high density devices are today becoming available to the general public. The commercial vendors now not only support but also have incorporated fixed hard processors on their FPGA's so that the complete systems can be implemented on a single programmable chip. When a certain soft core processor meets the requirements of an application to a certain extent, the designer has an advantage of describing that portion of the application using a high-level programming language. It is observed that more than 16% of all FPGA designs [1] contain soft processors, even though a soft processor cannot match the performance, area, and power of a hard processor [2]. Soft Core Processors are becoming increasingly popular because of the flexibility of reconfiguring the same core as the application changes. One of the captivating features of the Soft Core Processor is its optimized design that produced a compact size processor.

This paper presents a survey of six open-source soft core processors available from the open-source communities. The organization of this paper is as follows: Section II provides a summary of available soft-core processors provided by the open-source communities. Section III presents some applications which utilize soft-core processors. We compare several soft-core processors in Section IV based on important features such as the pipelining, area required for implementation, maximum clock frequency, etc followed by the conclusion in Section V.

II. AN INSPECTION OF SOFT-CORE PROCESSORS

In this section inspection of six open-source soft-core processors available from the open-source communities is done.

The SecretBlaze [4]: The SecretBlaze [3] is a MicroBlaze instruction set compliant processor which was developed using VHDL. The internal architecture is mainly based on the well-known DLX processor from John Hennessy and David Patterson.

The SecretBlaze implements a classic 32-bit RISC data path exploiting the instruction level parallelism with a 5-stage pipeline. It uses 32-bit addresses providing a 4 GB linear address space with 32-bit word-length. This is the only processor with global hazard controller, providing synchronous stall and flush signals for appropriate pipeline stages, to handle data and branch hazards. This hybrid approach, which combines both distributed and centralized control path methods, was introduced to strike the balance between the design quality and the efficiency of the Secret Blaze's data path. Indeed, the data path supports several optional instructions to make the best design trade-offs. These instructions include barrel shifter operations, pattern comparators, integer multiplications and integer divisions. Although not deeply optimized for FPGA devices, the implementation results confirm that the SecretBlaze provides a performance level close to the MicroBlaze, which offers an interesting alternative for an open-source processor.

LatticeMico32 [5]: The LatticeMico32 is a 32-bit RISC Harvard architecture soft-core processor. It provides the visibility, flexibility and portability that you expect in an open source hardware design.

By combining a 32-bit wide instruction set with 32 general purpose registers, the LatticeMico32 provides the performance and flexibility suitable for a wide variety of markets. It can handle up to 32 external interrupts and supports optional instruction and data caches. Using RISC architecture, the core consumes minimal device resources, while maintaining the performance required for a broad application set. To accelerate the development of microprocessor systems, several optional Wishbone compatible peripheral components may be integrated with the LatticeMico32.The LatticeMico system is based on the Eclipse C/C++ Development Tools Environment, which is an industry open-source development and application framework for building software.

LEON3 [6]: The LEON3 is a 32-bit processor based on the SPARC V8 architecture which is designed and maintained by Gaisler Research. Its implementation is based on Harvard architecture and uses the AMBA Advanced High-performance Bus (AHB) as its main on-chip communication bus. It implements a 7-stage pipeline and separate instruction and data caches.

The number of register windows is configurable within the limit of the SPARC standard. Using register windowing a new 'set' of local registers is selected upon a procedure call which makes the time consuming process of storing register contents in memory redundant. A default implementation has 8 global registers and 8 sets of register windows, and each window consists of 24 registers. At every time instant 32 registers will thus be visible for a program, while a total of 200 registers exist. It has a unique debug interface which allows non-intrusive hardware debugging and provides access to all registers and memory. A great advantage of the LEON3 processor is that it uses a structured organization of packets, folders and VHDL records, which influences the usability in a positive sense. This processor is very reliable and hence is used in a large number of military and space applications.

OpenRISC1200 (OR1200) [7] [8]: All OpenRISC implementations, whose first digit in identification number is 1, belong to OpenRISC 1000 family. Second digit defines which features of OpenRISC 1000 architecture are implemented and in which way they are implemented. Last two digits define how an implementation is configured before it is used in a real application.

The OR1200 is a 32-bit scalar RISC with Harvard micro architecture, 5-stage integer pipeline, virtual memory support (MMU) and basic DSP capabilities. This Harvard architecture has 32 bit instructions and can operate on 32- or 64-bit data. Default caches are 1-way direct-mapped 8KB data cache and 1-way direct-mapped 8KB instruction cache, each with 16-byte line size. Both caches are physically tagged. By default MMUs are implemented and they are constructed of 64-entry hash based 1-way direct-mapped data TLB and 64-entry hash based 1-way direct-mapped instruction TLB. It is amongst one of the high performing soft-core processors with 300 Dhrystone 2.1 MIPS at 300 MHz using 0.18u process.

OR1200 is intended for embedded, portable and networking applications. It can successfully compete with latest scalar 32-bit RISC processors in its class and can efficiently run any modern operating system.

OpenFire 0.3b [9]: A configurable 32-bit RISC processor that leverages the development tools of the Xilinx MicroBlaze soft-core processor. The OpenFire processor executes a subset of the MicroBlaze instruction set, eliminating instructions and functionality that are not needed in a processor array. It has 32-bit instruction and data words and includes all basic arithmetic operations. The instructions are pipelined in 3-stages which makes it different from the MicroBlaze architecture specification. The OpenFire is cycle-accurate to the MicroBlaze for every implemented instruction with a single exception. The hardware multiplier on the OpenFire introduces five cycles of latency as opposed to three cycles in the MicroBlaze.

Performance of the OpenFire is comparable to the MicroBlaze in Dhrystone MIPS and area. The OpenFire's maximum speed in xc2vp30-6 is 100 MHz using a 32-bit data path. When compared to a minimal MicroBlaze implementation (no OPB, cache, and barrel shifter or hardware divider) the OpenFire is 13% smaller and less than 1% slower in version 2.1 of the Dhrystone benchmark. The slight difference in DMIPS is most probably due to the OpenFire's longer multiply latency.

AEMB [10]: The AEMB is a clean room implementation of the EDK3.2 soft-ware compatible MicroBlaze core using information from the Internet. It is cycle and instruction compatible to the MicroBlaze for most software commands. It is not meant as a drop in replacement for the MicroBlaze as it is not architecturally compatible. It uses the Wishbone interface for both data and instruction memory bus. It has a CPU core that is capable of moving and manipulating data to and from memory. It does not have any peripherals nor interrupt controllers although support for external interrupts is provided. Any peripherals and their respective registers could be mapped to the data memory space.

AEMB has Harvard architecture with a separate 32-bit instruction and data busses. The address space for each bus can be separately configured with core parameters. It has a 3-stage integer pipeline that is capable of executing one instruction per clock. This short pipeline allows it to context switch quickly. It supports hardware multiplier and barrel shifter. Implementation of a single cycle multiplier and barrel shifter will improve software performance.

III. APPLICATIONS

In this section, discussion of some of the applications that exploit the use of above mentioned soft-core processors is done.

3.1 Video Processing

NASA's Communication Navigation and Networking Reconfigurable Testbed (CoNNeCT) experiment uses the Milkymist System-On-Chip (SoC). The Milkymist SoC uses the LatticeMico32 core as a general purpose processor. The Milkymist project is an informal association of people and companies, who develop, fabricate and trade an open source solution for the VJ's (Video Jockey) [11]. The LatticeMico32 processor is assisted by a texture mapping unit and a programmable floating point VLIW coprocessor which are used by the Flicker noise video synthesis software. It is also surrounded by various peripheral cores to support every I/O device of the Milkymist One.

3.2 Security and Authentication

University of California, Los Angeles (UCLA) students developed a prototype fingerprint authentication device using the LEON soft-core processor in their architecture for the ThumbPod [12]. In the prototype, the LEON processor is configured onto a Xilinx Virtex-II FPGA along with two co-processors: an encryption processor implementing the Advanced Encryption Standard (AES) and a Discrete Fourier Transform (DFT) processor. The LEON processor serves as the main core processor of the device and runs an embedded Java kilobyte virtual machine (KVM) to aid in software development. The ThumbPod is able to capture a fingerprint, extract its features, compare it to a known template, and return a matching score from 0 to 100 indicating the degree to which the captured fingerprint matches the template.

3.3 Image Processing

Shenzhen Graduate School Peking University, students developed the camera drivers that are able to demonstrate different special effects, including mirror effect, line-scanning effect, diff effect, edge blur effect and noise effect[13]. The distinctive feature is that these drivers were integrated at the level of driver rather than application program layer. The platform is consisted of open source software and hardware, which makes its cost lower. The Design of these special effect drivers is based on the OpenRISC1200 platform.

IV. COMPARISON OF SOFT-CORE PROCESSORS

TABLE 1 below shows a comparison of the features and characteristics of several open-source soft-core processors that we have inspected. The first column indicates the grounds on which the comparison is done followed by the available features of subsequent soft-core processors. The performance of AEMB appeared to be very high. While consuming only few logic elements the clock frequency is around 279 MHz when the multiplier and barrel shifters are disabled. However, only FPGA implementations are taken into consideration.

Table 1 Comparison of Soft-Core Processors

Category	SecretBlaze	LatticeMico32	LEON 3	OpenRISC 1200	OpenFire 0.3b	AeMB
Maximum MHz	90.9	85-115	183	185	198	279
Compatibility	Wishbone	Wishbone	AMBA 2.0	Wishbone	OPB,FSL	Wishbone
Pipelining	5-stages	6-stages	7-stages	5-stages	3-stages	3-stages
Architecture	DLX Processor	-	Sparc V8	ORBIS	MicroBlaze EDK 7.1	MicroBlaze EDK 6.2
Registers	-	32*32 bits	24*(2-32) bits	16/32*16/32 bits	-	32*32 bits
Language	VHDL	Verilog	VHDL	Verilog	Verilog	Verilog
Implementation	FPGA	FPGA	FPGA/ASIC	FPGA/ASIC	FPGA	FPGA
Flip Flop's	638	-	1133	1577	207	711
LUT's	1563	2370-2497	3448	3802	752	926
Address/Data Bus	32-bits	32-bits	32-bits	32/64-bits	32-bits	32-bits

Research states that LEON 3 and AEMB are the most complete and efficient implementations until so far. OpenRISC 1200 is too large for the amount of features it offers. And OpenFire 0.3b is too limited since there is neither solid data bus nor interrupt. The SecretBlaze though have a low clock frequency but still has a high level of flexibility, which balances computing performances and area cost to meet embedded system requirements.

V. CONCLUSION

In this paper inspection of six open-source soft-core processors and their comparison on various grounds is done. In many applications it would be convenient to have both a microprocessor and an FPGA array. Of course, one can have a separate RISC CPU and FPGA chips. But they can be also combined in one chip, leading to less power consumption, simpler board layout and fewer problems with signal integrity and EMI (electromagnetic interference). Soft-core processors are usually used to create an FPGA based system-on-chip (SoC).

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