IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 2, Issue 4 (May. – Jun. 2013), PP 53-56
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Design and Implementation of Feasible Direct Digital Synthesizer to Eliminate Manual Tweaking

Snehal Gaikwad[1], Kunal Dekate[2]
1 (E&TC, D.M.I.E.T.R., Wardha, Nagpur University, India)
2 (Electronics, G.H.R.C.E., Nagpur, Nagpur University, India)

Abstract: *This paper presents design and simulation of the programming model of optimal and feasible Direct Digital Synthesizer that eliminates the need for the manual tuning and tweaking related to component aging and temperature drift in analog synthesizer solutions. A Direct Digital Synthesizer is a measure part o Digital Down Converter where the DDC (Digital Down converter) has become a cornerstone technology in communication systems. Digital Down Converter (DDC) is key component of RF systems in communications, sensing, and imaging. This paper also evaluates the performance of DDS under various programming parameters and finally performs the realization of DDS using Virtex II Pro.*

***Keywords*:** *Theory of DDC, Direct Digital Synthesizer (DDS), Performance of Direct Digital Synthesizer and Simulation Results.*

I. Introduction

Digital down Converter (DDC) is key component of RF systems in communications, sensing, and imaging. Digital radio receivers often have fast ADC converters to digitize the band limited RF or IF signal generating high data rates; but in many cases, the signal of interest represents a small proportion of that bandwidth. To extract the band of interest at this high sample rate would require a prohibitively large filter. A DDC allows the frequency band of interest to be moved down the spectrum so the sample rate can be reduced, filter requirements and further processing on the signal of interest become more easily realizable. A fundamental part of many communications systems is Digital Down Conversion (DDC). A Digital down Converter is basically complex mixer, shifting the frequency band of interest to baseband. The DDC is typically used to convert an RF signal down to baseband. It does this by digitizing at a high sample rate, and then using purely digital techniques to perform the data reduction.

1.1. Overview of the DDC implementation

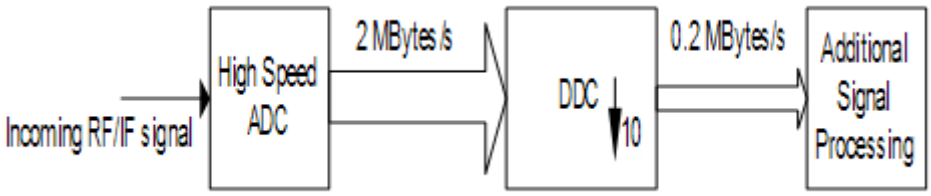

Fig. 1: Overview of the DDC Function

Consider a signal lying in the range 10-20 KHz. The signal bandwidth is 10 KHz. However, it is often digitized with a sampling rate over 1 M samples per Second, representing in the region of 2Mbyte/second. The DDC allows us to select the 10-20 KHz band, and to shift its frequency down to base-band and in doing so reduce the sample rate, with a 10 KHz bandwidth, a sample rate of 100 KHz would be fine - giving a data rate of only 0.2Mbyte/second. This is shown in Fig.1.

II. DDS (Direct Digital Frequency Synthesizer)

The DDS (Digital Direct Synthesizer) is an implementation of a direct digital frequency synthesizer (DDS) (also called Number Controlled Oscillator, NCO) which produces a sine wave at the output with a specified frequency and phase (adjustable at run time). The resolution of the Frequency Tuning Word (FTW), the phase and the amplitude are defined separately. While the FTW resolution can be set by the generic ftw_width, phase and amplitude resolution are defined as constants phase_width and ampl_width in the separate package sine_lut_pkg. This is generated by a Matlab script (sine_lut_gen.m), the m-files are described in their headers.

The nomenclature of the files is sine_<phase_width>_x_<amplitude_width>_pkg. hd. By adding one of these files to the project, the resolution of phase and amplitude is automatically defined. The function of the DDS is to generate the frequency equal to the sampling frequency of the first stage. The figure 2 shows the implementation of the DDS. A direct digital synthesizer operates by storing the points of a waveform in digital format, and then recalling them to generate the waveform. The rate at which the synthesizer completes one waveform then determines the frequency [1], [2].

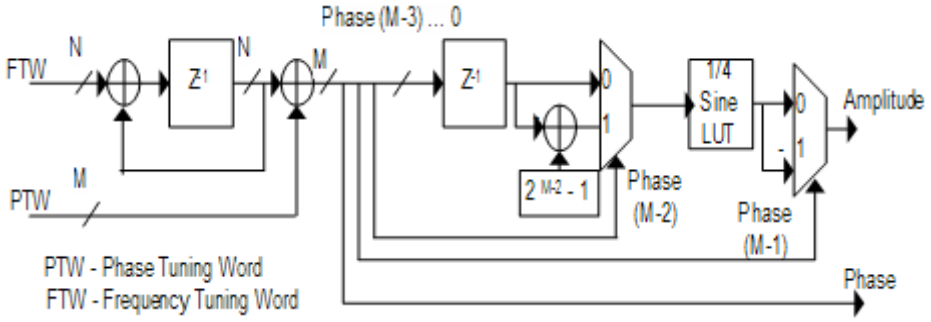

Fig.2: Direct Digital Frequency Synthesizer

2.1. Performance Details of DDS

The frequency and phase of the DDS can be controlled using the FTW (Frequency Tuning Word) and PTW (Phase Tuning Word).

The output frequency will be determined by the FTW.

$\mathbf{F_{dds}} = (FTW/2^{(N-M)})*(F_{clk} / (2^{M}))$ or

$\mathbf{F_{dds}} = FTW*F_{clk}/2^{N}$

Where F_{clk} = Clock Frequency

The initial phase can be controlled by PTW.

$\mathbf{\Phi_{dds}} = (PTW/2^{M})*2*pi$

Match the DDS frequency to the sampling frequency so that the spectrum gets shifted towards DC (0 Hz).

III. Results

3.1. Simulation results for DDS

Sampling Frequency : 60 MHz

TABLE 1: Parameters used for DDS module:

Parameter	Parameter Name	Data Types	Value	Units
Frequency Tuning Word	FTW_WIDTH	Integer	11	Bits
Phase Tuning Word	PHASE_WIDTH	Integer	9	Bits
Output Amplitude Word	AMPL_WIDTH	Integer	16	Bits

TABLE 2: VHDL simulation results are shown below:

Frequency Required	FTW	FTW actual	Frequency Generated	Actual Frequency from Simulation
5MHz	170.66	171	5.00MHz	5.00MHz

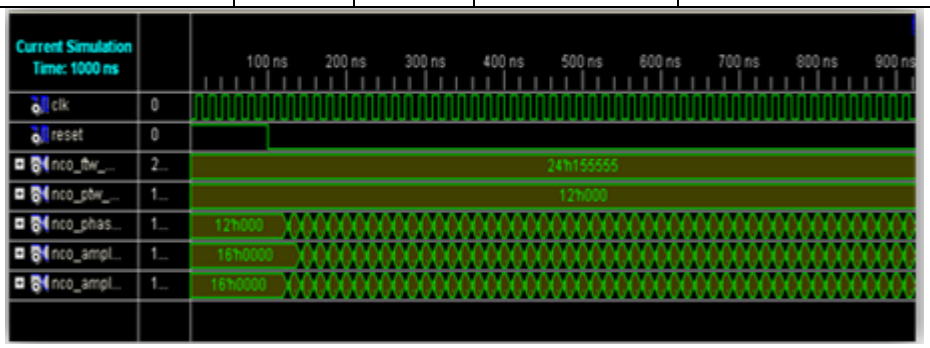

Fig. 3: Simulated output of DDS

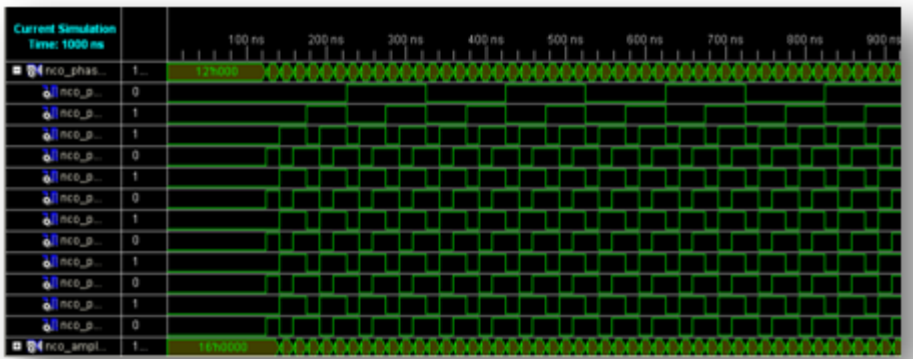

Fig. 4: Phase Simulation of DDS

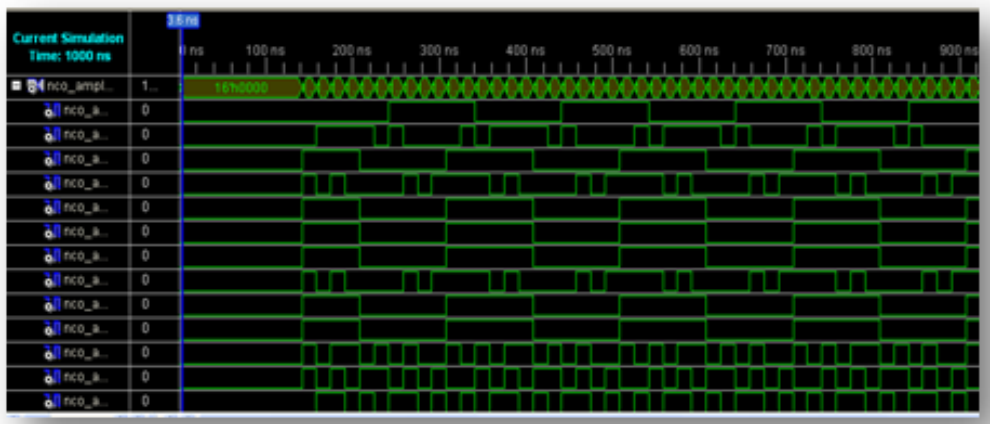

Fig. 5: Amplitude Simulation of DDS

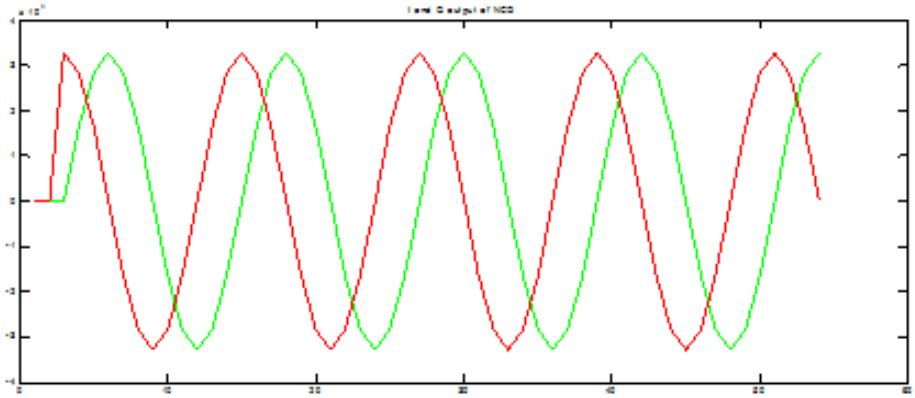

Fig. 6: Simulated Output of DDS

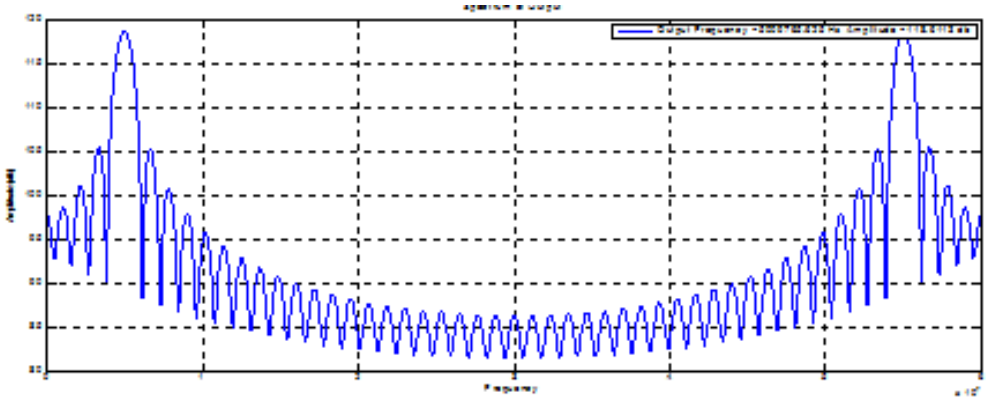

Fig. 7: Spectrum of DDS

IV. Conclusion

The performance of Direct Digital Synthesizer is done at tuning frequency which is specified as normalized value relative to clock rate given. Since it is dual Oscillator, hence it support variable Width, Phase modulation inputs and user defined frequency resolution. Here, the outputs of DDS can be adjusted over a wide range of frequencies with high degree of resolution.

V. Future Work

With a DDS, if the system operates at all, it works perfectly – there's never any tuning or component tolerance to worry about. As rate is programmable, it supports logic functions that would be extremely difficult to emulate with discrete logic gates. The design of code requires hardware with more resources as it exceeds the capacity of lower FPGA devices.

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