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High performance DA-Based DWT with High Accuracy Error-Compensated Adder Tree

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Abstract: *Image compression is one of the major image processing techniques that are widely used in medical, automotive, consumer and military applications. Discrete wavelet transforms is the most popular transformation technique adopted for image compression. In this brief, by operating the shifting and addition in parallel, an error-compensated adder-tree (ECAT) is proposed to deal with the truncation errors and to achieve low-error and high-throughput discrete wavelet transform (DWT) design. Instead of the 12 bits used in previous works, 9-bit distributed arithmetic-precision is chosen for this work so as to meet peak-signal-to-noise-ratio (PSNR) requirements. Thus, an area-efficient DWT core is implemented to achieve 1 Gpels/s throughput rate with gate counts of 22.2 K for the PSNR requirements outlined in the previous works. This design is twice faster than the reference design and is thus suitable for applications that require high speed image processing algorithms.*

Key words: *Distributed arithmetic (DA)-based, error-compensated adder-tree (ECAT), 2-D Discrete wavelet transforms (DWT).*

I. Introduction

Technological growth of semiconductor industry has led to unprecedented demand for low power, high speed complex and reliable integrated circuits for medical, defence and consumer applications. Today's electronic equipment comes with user friendly interfaces such as keypads and graphical displays. As images convey more information to a user, it is many of the equipment today have image displays and interfaces. Image storage on these smaller, handled devices is a challenge as they occupy huge storage space; also image transmission requires higher bandwidth. Hence most of the signal processing technologies today has dedicated hardware that act as co-processors to compress and decompress images. In this work, a reliable, high speed, low power DWT-IDWT processor is designed and implemented on FPGA which can be used as a co-processor for image compression and decompression. The Discrete Wavelet Transform (DWT) is being increasingly used for image coding. This is because the DWT can decompose the signals into different sub-bands with both time and frequency information. It also supports features like progressive image transmission, compressed image manipulation, and region of interest coding [1]. Recently several VLSI architectures have been proposed to realize single chip designs for DWT [2]-[7]. Traditionally, such algorithms are implemented using programmable DSP chips for low-rate applications, or VLSI application specific integrated circuits (ASICs) for higher rates. In wavelet transforms, the original signal is divided into frequency resolution and time resolution contents. The decomposition of the image using 2-level DWT is shown in Figure 1.

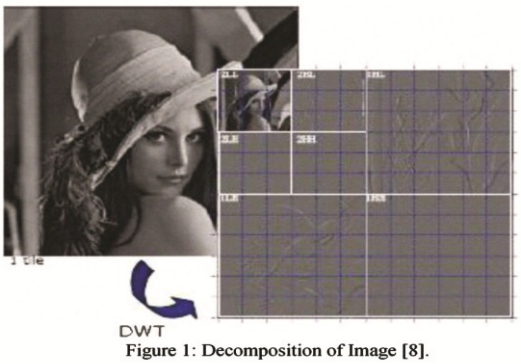


Figure 1: Decomposition of Image [8].

II. DWT Architecture

Figure 1: Decomposition of Image [8].

This brief addresses a DA-based DCT core with an error-compensated adder-tree (ECAT). The proposed ECAT operates shifting and addition in parallel by unrolling all the words required to be computed. Furthermore, the

error-compensated circuit alleviates the truncation error for high accuracy design. Based on low-error ECAT, the DA-precision in this work is chosen to be 9 bits instead of the traditional 12 bits so as to achieve the peak-signal-to-noise-ratio (PSNR) [13] requirements. Therefore, the hardware cost is reduced, and the speed is improved using the proposed ECAT.

This brief is organized as follows. In Section II, DWT architecture and the proposed ECAT architecture is discussed.Finally the proposed 8 X 8 2-D DWT core is demonstrated also discussed in this section. The comparisons and results are presented in Section III, and conclusions are drawn in Section IV.

II. System Design Model

A. Dwt Architecture

Image consists of pixels that are arranged in two dimensional matrixes, each pixel represents the digital equivalent of image intensity. In spatial domain adjacent pixel values are highly correlated and hence redundant. In order to compress images, these redundancies existing among pixels needs to be eliminated. DWT processor transforms the spatial domain pixels into frequency domain information that are represented in multiple sub-bands, representing different time scale and frequency points. Human visual system is very much sensitive to low frequency and hence, the decomposed data available in the lower sub-band region and is selected and transmitted, information in the higher sub-bands regions are rejected depending upon required information content. In order to extract the low frequency and high frequency sub-bands DWT architecture shown in figure below is used. As shown in the figure, input image consisting rows and columns are transformed using high pass and low pass filters. The filter coefficients are predefmed and depend upon the wavelets selected. In this work, 9/7 wavelets have been used for constructing the filters. First stage computes the DWT output along the rows, the second stage computes the DWT along the column achieving first level decomposition. Low frequency sub-bands from the first level decomposition is passed through the second level and third level of filters to obtain multiple level decomposition as shown in Figure 2.

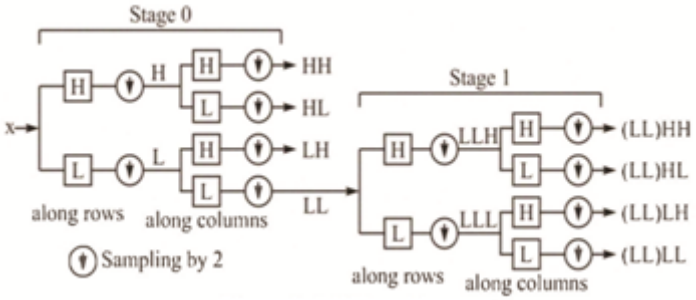


Figure 2: DWT architecture

There are several architectures for realizing the DWT shown in Figure 2, paper [11] summarizes various schemes. Most popular one is the DA-DWT scheme that is suitable on FPGA, as it consumes fewer resources and has high through put. DA-DWT architecture based on pipelining and parallel processing logic is realized and implemented on FPGA [12]. In this work, a modified DA-DWT architecture is designed based on the work reported in [12]. The number of LUTs and number of shift registers are reduced by exploiting the symmetric property of the 917 wavelet filters. Efficient fixed point number representation scheme is identified to accurately represent the 917 filter values and are stored in the LUT memory space on FPGA. A control logic designed loads the input data into the FPGA from the external memory, LUT contents are read out based on the input samples as address to LUT. After 8clock cycles of initial latency, DWT outputs are computed every clock cycle. A detailed discussion of the proposed architecture is presented in section IV. Software reference model for DWT-IDWT processor is built using MATLAB. Multiple image test vectors are used in analyzing the performances of the software reference model. A detailed discussion of the software reference model results are presented in section III.

B. Distributive Arithmetic Based 2D DWT/IDWT Architecture

In this section, we first outline how to perform multiplication by using memory based architecture. Following this, we briefly explain architecture for DWT filter bank. Using this we show complete design for block based DWT. The memory based approach provides an efficient way to replace multipliers by small ROM tables such that the DWT filter can attain high computing speeds with a small silicon area as shown in Figure 3. Traditionally, multiplication is performed using logic elements such as adders, registers etc. However, multiplication of two n-bit input variables can be performed by a ROM table of size of 22n entries. Each entry stores the pre-computed result of a multiplication. The speed of the ROM lookup table is faster than that of hardware multiplication if the look-up table is stored in the on-chip memory. In DWT, one of the input variables

in the multiplier can be fixed. Therefore, a multiplier can be realized by 2n entries of ROM. Distributed arithmetic implementation of the Daubechies 8-tap wavelet FIR filter consists of an LUT, a cascade of shift registers and a scaling accumulator [12].

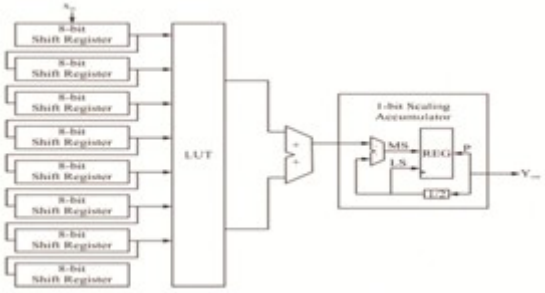


Figure 3 Distributive Arithmetic

To speed up the process parallel implementation of the Distributive Arithmetic (DA) architecture shown in Figure 4 is realized in [12]. In parallel implementation, the input data is divided into even samples and the odd samples based on their position. This scheme reduces the memory size to half due to the symmetric property of the filter coefficients. This increases the through put as the input samples are simultaneously used to read the data from two LUTs and hence speed is increased.

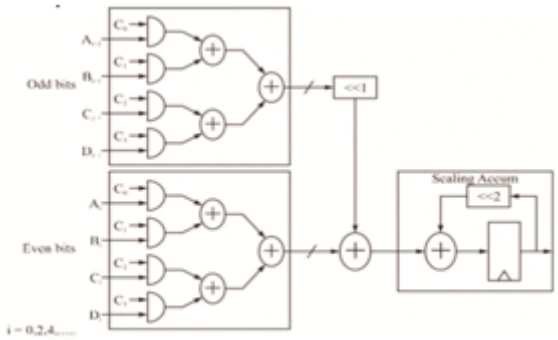


Figure 4 Parallel implementation of DA technique

In order to further increase the speed and reduce the area, the LUT can be further split into four stages, and can be accessed by the input values for data read.

C. ECAT Architecture

In general, the shifting and addition computation uses a shift-and-add operator in VLSI implementation in order to reduce hardware cost. However, when the number of the shifting and addition words increases, the computation time will also increase. Therefore, the shift-adder-tree (SAT) presented in previous words operates shifting and addition in parallel by unrolling all the words needed to be computed for high-speed applications. However, a large truncation error occurs in SAT, so ECAT architecture is presented to compensate for the transaction error in high speed applications

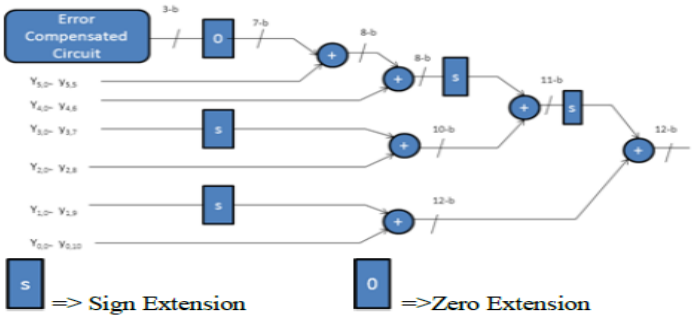


Figure: 5. ECAT Architecture

The ECAT has the highest accuracy with a moderate area delay product. The shift and add method has the smallest area, but the overall computation time is equal to is the longest. Similarly, the SAT is the best area-delay product performance. However, for system accuracy, the SAT is the worst option. Therefore, the ECAT is suitable for high-speed and low-error application. This ECAT operates shifting and addition in parallel by unrolling all the words required to be computed. Furthermore, the error- compensated circuit alleviates the

truncation error for high accuracy design. Based on low-error ECAT, the DA-precision in this work is chosen to be 9 bits instead of the traditional 12 bits so as to achieve the peak-signal-to-noise-ratio (PSNR) requirements. The proposed ECAT has the highest accuracy with a moderate area delay product. The previous method shift and add method has the smallest area, but the overall computation time is equal to 10.8(=1.8x6) ns that is the longest. Similarly, the SAT, which truncates the TP and computes in parallel, takes 3.72 ns to complete the computation and uses 406 gates, which is the best area-delay product performance. However, for system accuracy, the SAT is the worst option. Therefore, the ECAT is suitable for high-speed and low-error applications.

D. 8x8 2D DWT CORE DESIGN

The DWT implemented using a tree-structured filter bank, where the M wavelet coefficients are computed through $\log 2M$ octave levels. At each octave level j, an input sequence is fed into the low-pass filter $h(m)$ and the high-pass filter $g(m)$. A number of filter banks are cascaded to produce a multi-resolution wavelet analysis. Figure 6 shows the analysis stage of three-level wavelet decomposition in binary tree. Here, the filters $H(z)$, $G(z)$ satisfy the PR property [14].

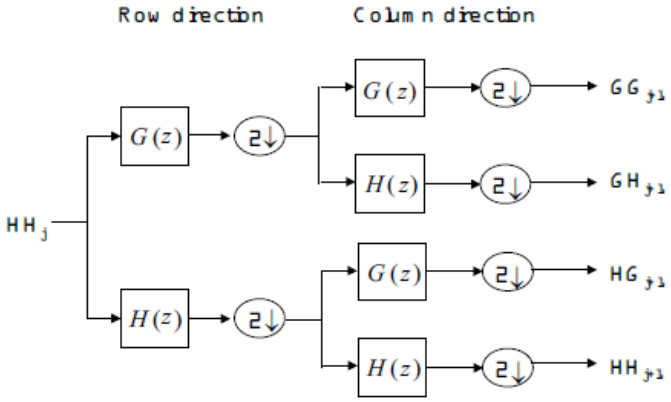
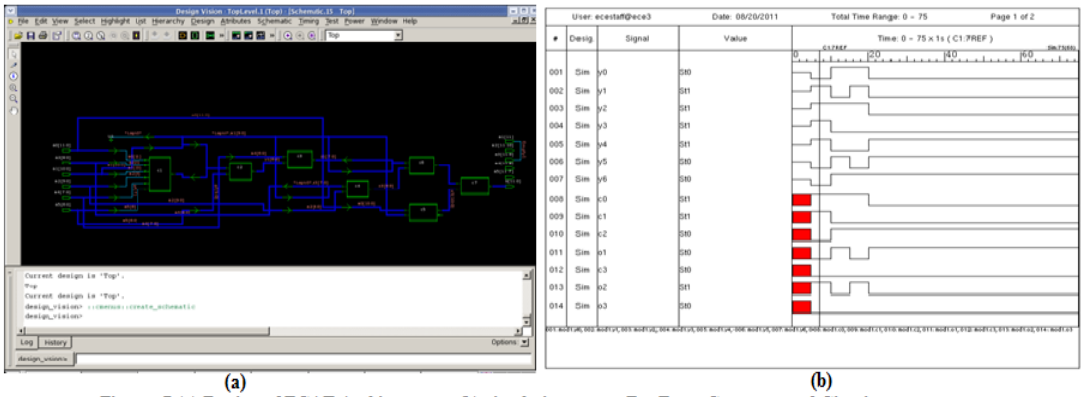


Figure: 6 One level of 8x8 2D DWT (Analysis stage)

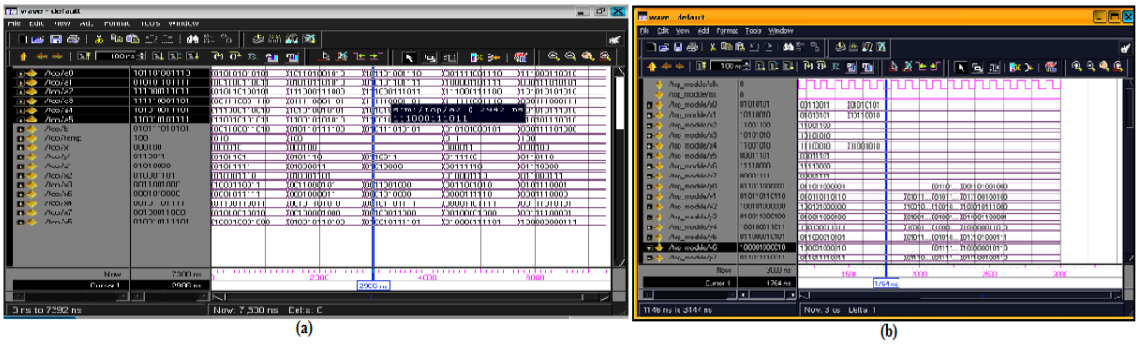
III. Simulation Results

Error Compensated Circuit which will helpful in reducing truncation error and its design shown in fig.7(a). The ECC will be introduced in ECAT architecture Thus the ECAT architecture designed using design compiler is shown in fig.7(b) and its simulation result shown in fig. 8(a). This ECAT Architecture will be helpful in increasing throughput rate also it reduce the truncation error occur in DWT core design. The proposed DWT core uses low error ECAT to achieve a high-speed design, and the DA-precision can be chosen as 9 bits to meet the PSNR requirements for reducing hardware costs After ECAT architecture is designed it is implemented in the DCT architecture. The simulation result of implementing ECAT on 1D 8 point DCT architecture is shown in fig.8(B). Furthermore, the proposed work of 2-D DCT core synthesized by using Xilinx ISE 9.1, and the Xilinx XC2VP30 FPGA can achieve 792 mega pixels per second (M-pels/sec) throughput rate.



(a) (b)

Figure: 7 (a) Design of ECAT Architecture , (b) simulation output For Error Compensated Circuit



(a) (b)

Figure:8 (a) simulation output For ECAT Architecture , (b) Simulation Result of 1D 8 point DWT Architecture

IV. Conclusion

In this paper, Error Compensated Adder Tree is proposed for the DWT to improve the throughput rate significantly at high compression rates by operating the shifting and addition in parallel. Furthermore, the proposed Error-Compensated Circuit alleviates the truncation error in ECAT. In this way, the Distributed Arithmetic precision can be chosen as 9 bits instead of 12 bits so as to meet the PSNR requirements. Thus, the DWT core will have the highest hardware efficiency than those in previous works for the same PSNR requirements. Finally, an area-efficient 2-D DWT core can be implemented using a TSMC 0.18 µm process and the maximum throughput rate is 1 Gpels/s. In summary, the proposed ECAT architecture for the DWT is suitable for high compression rate applications in VLSI designs.

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