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Intelligent High Performance Memory Access Technique in Aspect of DDR3

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Abstract: *The uninterrupted development of memory market has experienced a new face since the beginning of the 21st century due to the emergence of pc markets such as Laptop, Server PC, Tablet and Smart phones. This paper demonstrates the implementation of intelligent high performance memory access technique of DDR3 SDRAM. This paper discusses the full architecture of DDR3 SDRAM controller with minimum accessible time. It is designed to achieve high performance memory access with faster read and write.*

Keywords - *Architecture of DDR3 controller, DDR3, High geared access, RAM Controller, SDRAM*

I. INTRODUCTION

DDR3 SDRAM is the third generation of DDR family which is a high speed dynamic random access memory. It transfers the data at twice the rate of DDR2 SDRAM which enables higher bandwidth while DDR2 SDRAM uses 4n-prefetch; DDR3 SDRAM uses 8n-prefetch [1]. The interface techniques of DDR3 SDRAM are not adapted by other DDR family due to different signaling voltages, timings, and other parameters [2].SDRAM controller is a digital circuit which manages the flow of data going to and from the memory. Thus for the compatibility issue it is necessary to have a DDR3 compatible SDRAM Controller.

The DDR3 SDRAM Controller accepts commands using a simple local interface and translates them to the command sequences required by DDR3 SDRAM devices. The core also performs all initialization and refresh functions. It uses bank management techniques to monitor the status of each SDRAM bank. Banks are only opened or closed when necessary, minimizing access delays. Up to eight banks can be managed at one time [4]. A command pipelining interface is used enabling multiple, random address requests to be queued up, each with lengths as short as 4 DDR3 data cycles. This architecture provides optimal bandwidth utilization both for cases of short transfers to highly random address locations as well as cases of longer transfers to contiguous address space.

II. ARCHITECTURE

DDR3 SDRAM Controller is designed with three stage queue depth command Pipeline Module, Bank Status Module, Full functional State Machine, Controller Core and Data Control.

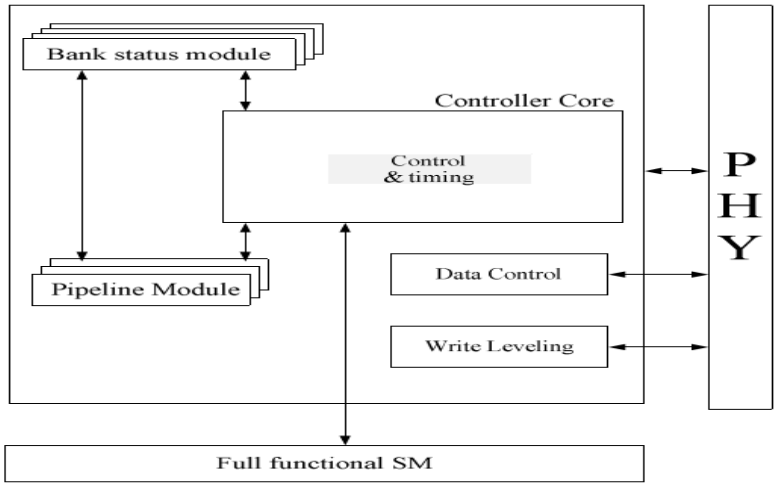

Figure 1: Architecture of DDR3 SDRAM controller

2.1 DRAM controller

DRAM Controller handles the timing and controlling of DDR3 SDRAM Controller. It also generates command address logic. DRAM Controller interconnects the Pipeline Module and Bank Status Module. This is the primary address command generation logic.

2.2 Pipeline Module

Local Interface of DDR3 Controller Core is implemented as a pipeline which enables the memory access request in each clock as long as pipeline is not full. That means memory access request is queued until it is not full.

2.3 Bank Status Module

The DDR3 SDRAM Controller integrates Bank organizing techniques to minimize processing time required by a SDRAM Controller prior to the execution of a command. The controller records the status of each bank whether the last opened row and bank has been closed or not.

2.4 Full Functional State Machine

DDR3 SDRAM Controller Core handles the initialization of the SDRAM when system leaves the reset state. It also handles the periodic refresh operations to the SDRAM after initialization. SDRAM Controller provides an interface that allows an external process or logic to drive the SDRAM memory device initialization sequence.

2.5 Data Control

Data Control Handles the tri-state controls of data, data strobes and data strobe switching enable signal. Phy output enables, data phase signaling and ODT enables are also controlled by this module.

2.6 Write Leveling

As speed increase signal integrity is really a matter of issue in DDR3 SDRAM devices. For this purpose, DDR3 utilizes fly-by topology for connection of the command. Each data, data mask, data strob signals must be calibrated independently in order to maintain the timing requirements. This calibration process is known as write leveling.

III. OVERVIEW

SDRAM is high-speed Dynamic Random Access Memory (DRAM) with a synchronous interface. This architecture is fully pipelined which allows fast data rates. SDRAM is formed with banks and banks are addressed with rows and columns. The no of rows and column depends on the configuration of the memory and size.

There are several bus commands to control DDR3 SDRAM. Bus commands are formed with the combination of ras_n(row address strobe), cas_n(column address strobe), and we_n(write enable) signals.[3&4]

Table

SDRAM bus commands

Command	ras_n	cas_n	we_n
No Operation(NOP)	H	H	H
Active	L	H	H
Read	H	L	H
Write	H	L	L
Precharge	L	H	L
Refresh	L	L	H
ZQ Calibration	H	H	L
Mode Register Set	L	L	L

DDR3 SDRAM Controller is divided into eight banks. These banks are opened when addresses are written or read from. Row and bank is opened by issuing Active command. When a new row on a bank is accessed it may necessary to close the first bank and then reopen the bank to the new row. Closing bank is performed using the Precharge command.

When write command is issued, data is presented after 5 to 8 clocks [5]. This is known as CAS write latency. For reads, data is presented 5 to 11 clocks after read command [5]. This is known as CAS read latency. These latencies are depended on the speed grade of DDR3.

To maintain the integrity of store data, DDR3 SDRAM devices required periodic refresh. This DDR3 SDRAM Controller automatically issues the refresh command periodically.

The Mode Register Set (MRS) command is used to program four mode registers that are exist in DDR3 SDRAM devices [3]. Mode registers are used to define various modes of programmable operation.

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IV. FUNCTIONAL DESCRIPTION

The DDR3 SDRAM Controller handles the initialization of the memory devices, manages the banks, and keeps the devices refreshed at regular intervals [3]. The controller translates read or write requests from local interface into all the necessary SDRAM commands.

The state diagram gives a description of different state transitions and commands to control DDR3 SDRAM.

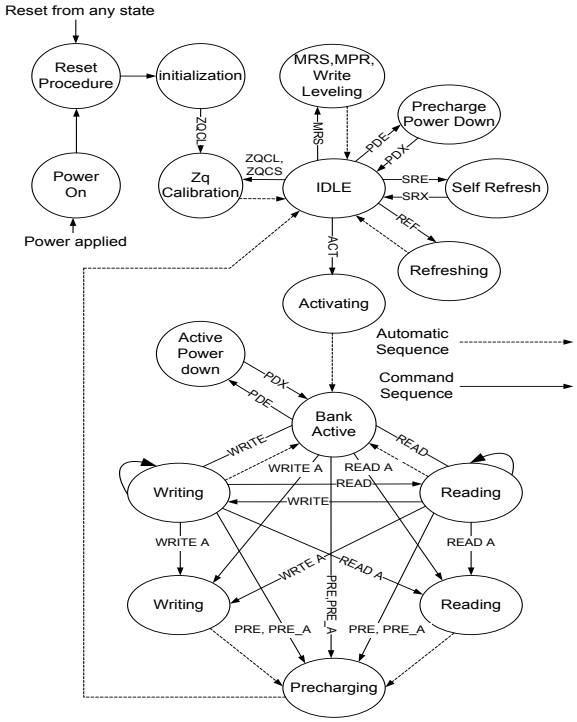

Figure 2: State diagram of DDR3 SDRAM controller

4.1 Initialization

The initialization sequence of DDR3 SDRAM controller is automatic. It starts with the start up delay and involves different mode registers set commands write leveling if configured and ZQ calibration. The sequence of initialization follows the JEDEC specifications and described below:

1. Hold reset_n and cke_n (clock enable) low for 200 us.
2. 'reset_n' is set to high with additional 600us low of cke_n.
3. Wait tXPR (exit reset from CKE high to valid command).
4. Issue Mode Register Set command to MR2.
5. Issue Mode Register Set command to MR3.
6. Issue Mode Register Set command to MR1.
7. Issue Mode Register Set command to MR0.
8. Issue ZQCL command to starting ZQ calibration.
9. Wait 512 clocks to finish calibration.
10. Automatic write leveling is performed upon configuration.
11. The DDR3 SDRAM Controller is now ready to do normal operation.

The snapshots below show the different steps of initialization process of our designed DDR3 SDRAM controller which is written by Verilog HDL.

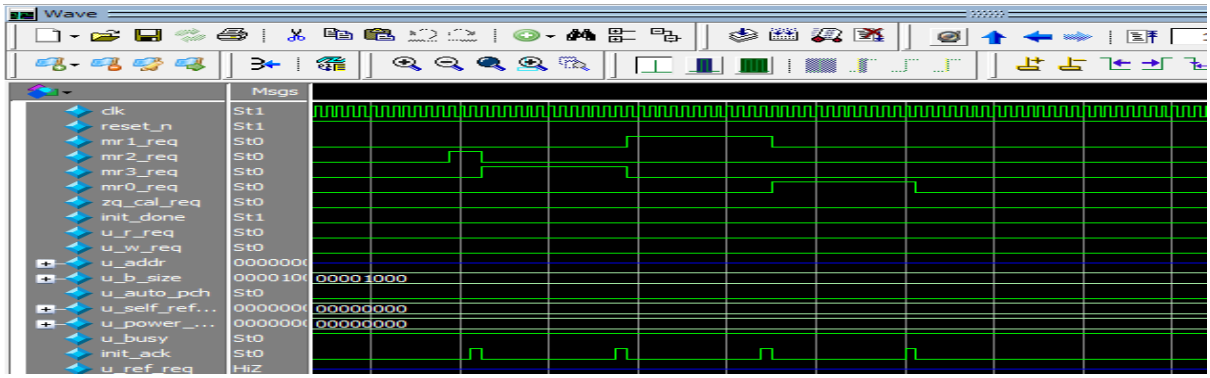

Figure 3: Mode registers set commands in different mode registers

After tXPR time, in Fig. 3 MRS is requested to MR2, MR3, MR1 and MR0 respectively. After that ZQ Calibration is requested by the controller and depending on the configuration of write leveling controller request 'wlvl' unless after certain time 'init_done' goes to high to show the status that initialization is done which is shown in Fig. 4.

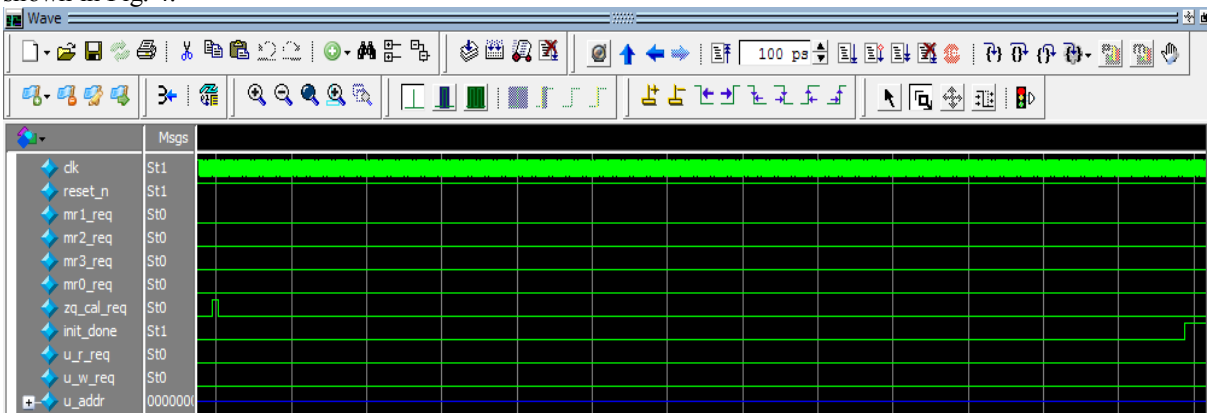

Figure 4: ZQCL request and initialization done sequence

Now controller is ready to do operation refresh and can accept any read, write, precharge, read with auto precharge or write with auto precharge commands.

4.2 Refresh

To maintain data integrity, DDR3 SDRAM Controller issue periodic refresh automatically to SDRAM devices. Without user intervention DDR3 SDRAM Controller issue periodic refresh.

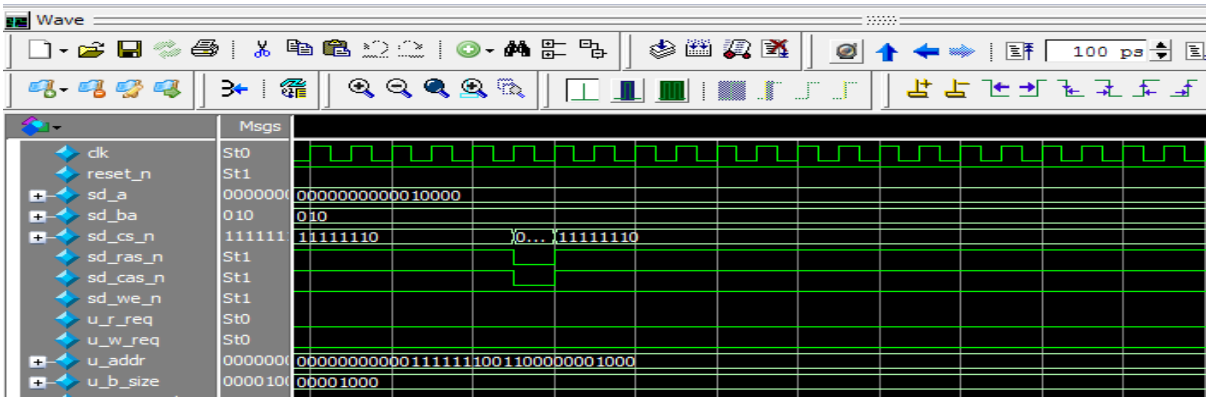

Figure 5: Automatic refresh issued by controller

Fig. 5 shows an automatic refresh command by setting ras_n, cas_n low and we_n high. Each refresh is issued by controller after tRFC (refresh count time) time which is configured by a refresh configuration (cfg_ref) port. The refresh never interrupts read or write command at the middle of the read or write burst. On the other hand, if the controller determines that a refresh command comes up concurrent with read or write, the request is held off until after the refresh is performed.

4.3 Write

The user requests writes by asserting 'u_w_req' high and driving the starting address and burst size on 'u_addr' and 'u_b_size' respectively. If 'u_auto_pch' asserts with 'u_w_req' then write with auto-precharge is performed by the controller. The Fig. 6 is an example of write operation and the sequence is briefly described below:

1. In Fig. 6 write request ('u_w_req') signal is asserted along with the starting address ('u_addr') and burst size ('u_b_size') of eight.
2. 'u_busy' is not high which indicates controller can accept another request. However, in this example another write is not requested.
3. As a result of the write request controller asserts the row address ('sd_a'), bank address ('sd_ba') and chip select ('cs_n') with the active command to open requested bank to the requested row.
4. Then the controller issues a write command with appropriate column address.
5. After satisfying some delay controller request to user to put data by 'u_d_req' high via 'u_datain' signal.
6. The controller starts strobing data to the SDRAM devices.

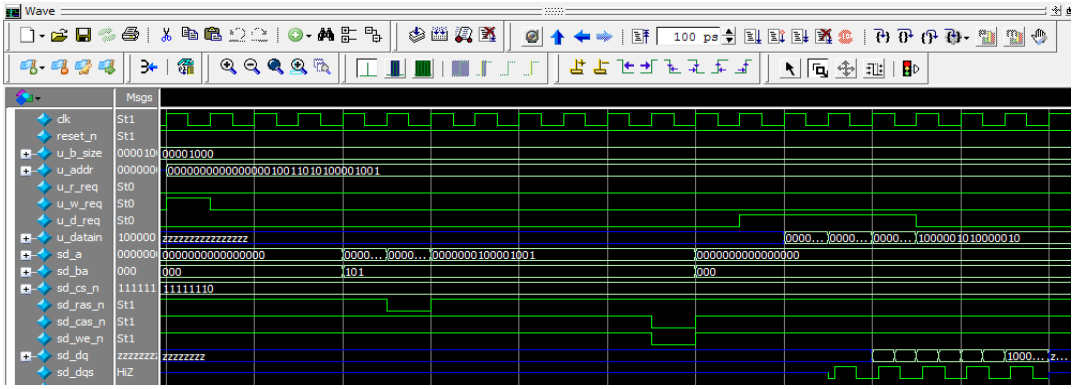

Figure 6: Write operation of DDR3 SDRAM controller

In this sequence, a write is requested; another two read or write operation can be requested until 'u_busy' is not goes to high. In two consecutive read or write commands, if these commands are in different banks, it is necessary to close the 1st requested bank by precharge command. On the other hand, if the commands are in same bank does not need to close the banks.

4.4 Read

The user requests read by asserting 'u_r_req' high and driving the desire address 'u_addr' user wants to read. If 'u_auto_pch' asserts with 'u_r_req' then read with auto-precharge is performed by the controller. The Fig. 7 illustrates an example of read operation without auto-precharge.

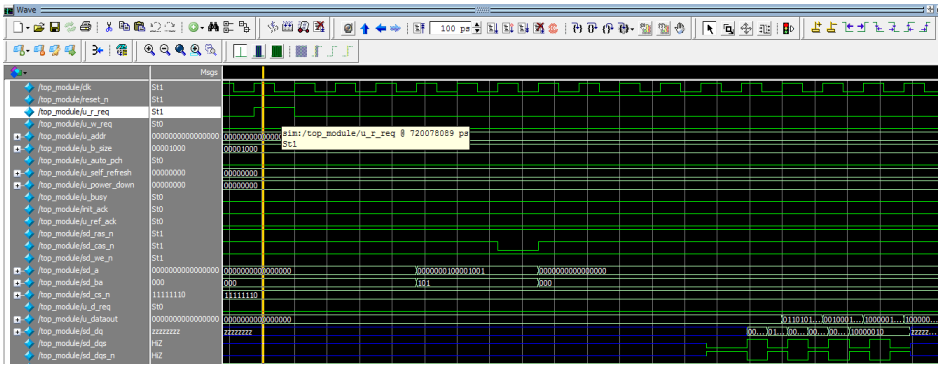

Figure 7: Read operation of DDR3 SDRAM controller

1. In Fig. 7 read request ('u_r_req') signal is asserted along with the starting address ('u_addr') and burst size ('u_b_size') of eight.
2. 'u_busy' is not high which indicates controller can accept another request. However, in this example another read is not requested.
3. As a consequent of read request controller asserts the row address ('sd_a'), bank address ('sd_ba') and chip select ('cs_n').

4. Then the controller issues a read command.
5. The read data valid ('u_r_valid') signal is asserted while valid data is available at the 'u_dataout' bus.

In this sequence, same as write only a read is requested, another two read or write can be requested.

V. ANALYSIS AND SYNTHESIS

The DDR3 SDRAM controller is written by Verilog HDL and synthesized by Design Compiler (Synopsis EDA tools). In order to validate the controller architecture, different simulation model of Micron DDR3 RAM is used. A physical Interface (simulation model) is designed to interface the simulation model with DDR3 RAM. The architecture is validated with 2GB, 4GB micron RAM with different(x8, x16) architectures. This architecture is completely pipelined and can support several frequencies like 667MHz, 800MHz, 933MHz and 1066MHz. To automate the testbench and simulation, Perl script was used. There are many synthesis report generated by Synopsis Design Compiler and those are area synthesis report, cells synthesis report, check synthesis report, max timing synthesis report, min timing synthesis report, reference synthesis report and resources synthesis report . The top module area synthesis report is given bellow:

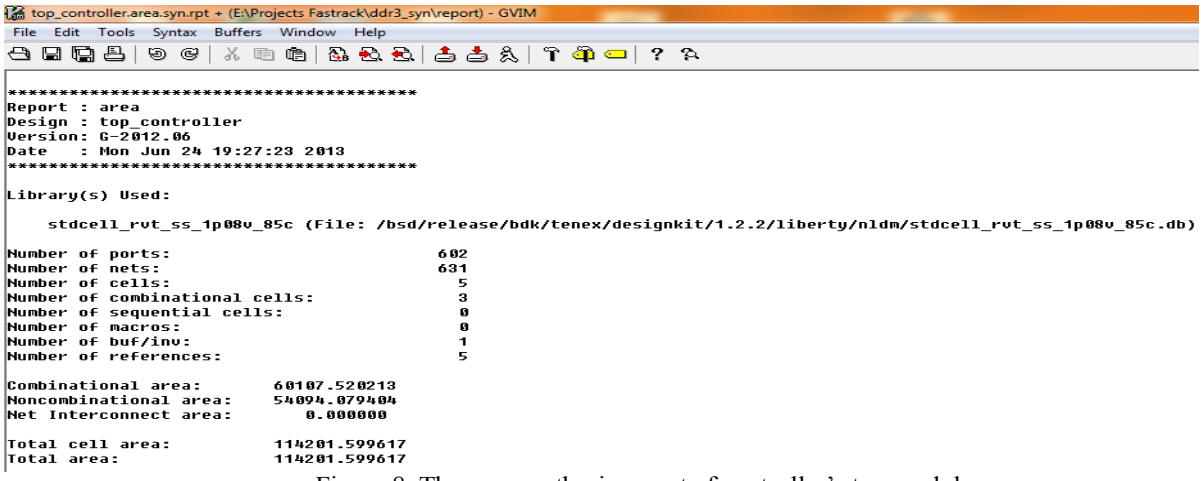

Figure 8: The area synthesis report of controller's top module

VI. CONCLUSION

The proposed architecture is implemented and verified successfully. The library we used is 65nm process technology. The functionality is fully compatible with DDR3 RAM, which is also verified. The three stage pipelined architecture ensures that it can accept three requests before completed any task that means it can access comparatively faster in RAM.

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