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A Digital multiple beam forming for phased array RADARs with parallel array processing

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Abstract: *Phased array radar is very important in modern radar development, and multiple digital beams forming technology is the most significant technology in phased array radar. Beam forming is a signal processing technique used in antenna arrays for directional signal transmission or reception. Digital multiple beam forming on each antenna element about large phased array radar is impossible in processor based digital processing units, because it needs simultaneous processing many A/D channels. In this project we resolve this problem by using a multi array based beam forming technique with multiplexed signal processing unit on FPGA. The conventional technique of completely duplicated hardware and also dynamic reconfiguration does not yield the real time parallel beam processing. The proposed technique employs multiplexed signal processing unit which is time shared for various beam formers. This technique provides simultaneous beams without any compromise on functionality.*

I. Introduction

In antenna theory, a **phased array** is an array of antennas in which the relative phases of the respective signals feeding the antennas are varied in such a way that the effective radiation pattern of the array is reinforced in a desired direction and suppressed in undesired directions.

An antenna array is a group of multiple active antennas coupled to a common source or load to produce a directive radiation pattern. Usually, the spatial relationship of the individual antennas also contributes to the directivity of the antenna array. Use of the term "active antennas" is intended to describe elements whose energy output is modified due to the presence of a source of energy in the element (other than the mere signal energy which passes through the circuit) or an element in which the energy output from a source of energy is controlled by the signal input. One common application of this is with a standard multiband television antenna, which has multiple elements coupled together.

Digital multiple beam forming on each antenna element about large phased array radar is impossible in processor based digital processing units, because it needs simultaneous processing many A/D channels. In this project we resolve this problem by using a multi array based beam forming technique with multiplexed signal processing unit on FPGA. The conventional technique of completely duplicated hardware and also dynamic reconfiguration does not yield the real time parallel beam processing. The proposed technique employs multiplexed signal processing unit which is time shared for various beam formers. This technique provides simultaneous beams without any compromise on functionality.

II. Phased Array Antenna

Electronically-steered phased array radar is an array of antennas in which the relative phases of the respective signals feeding the antennas are varied in such a way that the effective radiation pattern of the array is reinforced in a desired direction and suppressed in undesired directions.

Phased array transmission was originally developed in 1905 by Nobel Laureate Karl Ferdinand Braun who demonstrated enhanced transmission of radio waves in one direction. During World War II, Nobel Laureate Luis Alvarez used phased array transmission in a rapidly-steer able radar system for "ground-controlled approach", a system to aid in the landing of aero planes in Britain. At the same time GEMA in Germany built the PESA Mammut. The design is also used in radar, and is generalized in inter-ferometric radio antennas. In 2007 DARPA researchers announced a 16 element phased array integrated with all necessary circuits to send at 30–50 GHz on a single silicon chip for military purposes.

These antenna arrays completely consist of singles radiating elements and each of it gets an own phase shifter. The elements are ordered in a matrix array. The planer arrangement of all elements forms the complete phased array antenna. One of the advantages is the Beam forming in two planes are digital Beam forming is possible.

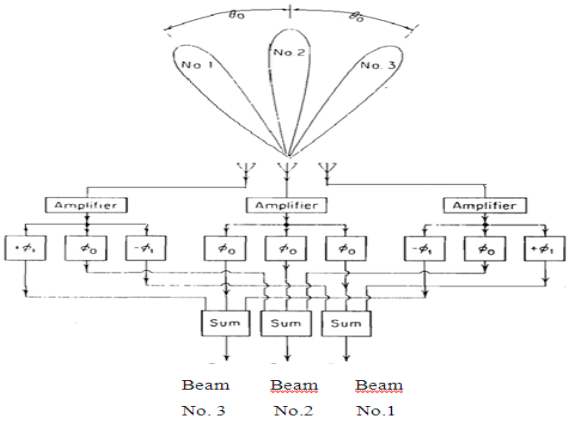

Fig 2.1: Electronic phased array beam formation

III. Hardware Specifications

1 RF Translator

Radio frequency (RF) is a rate of oscillation in the range of about 3 kHz to 300 GHz, which corresponds to the frequency of radio waves, and the alternating currents which carry radio signals. RF usually refers to electrical rather than mechanical oscillations, although mechanical RF systems do exist.

In order to receive radio signals an antenna must be used. However, since the antenna will pick up thousands of radio signals at a time, a radio tuner is necessary to tune in to a particular frequency (or frequency range).This is typically done via a resonator – in its simplest form, a circuit with a capacitor and an inductor forming a tuned circuit.

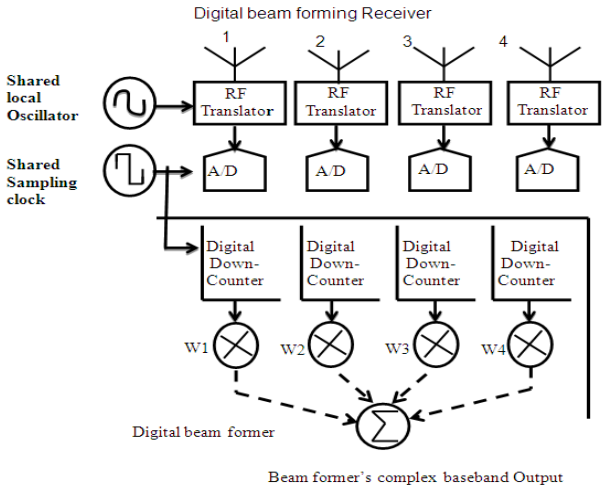

Fig 3.1 Digital Beam Forming

The circuit amplifies oscillations within a particular frequency band, while reducing oscillations at other frequencies outside the band.

III. Digital Down-Counter

The principle of Digital Down-Counter which is taking the input from RF Translator that is given to the input of Fast ADC .The output of Fast ADC block which is given to the DDC block. The DDC (Digital Down-Counter) consists of NCO (Numerically Controlled Oscillator), Multiplier, low pass filter and Decimator.

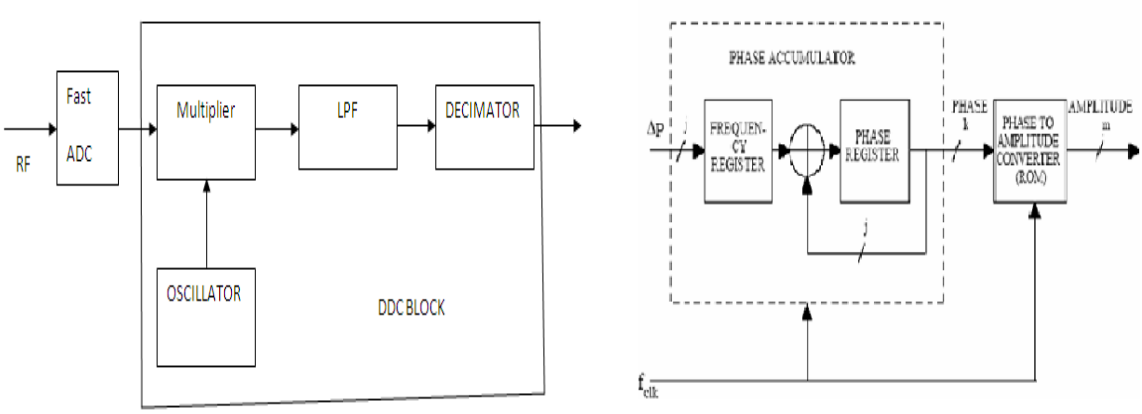

Fig.2.2 Digital down Counter

Fig.3.3. NCO (Oscillator)

IV. Oscillator (NCO)

The NCO main purpose is to generation the carrier signals (cosine).The main advantage is ROM based techniques will be used for area optimization.

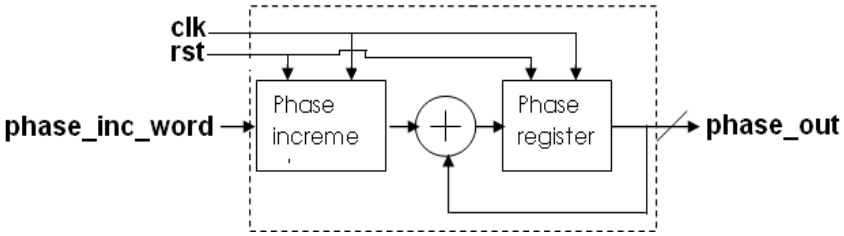

Fig.3.4 phase accumulator

The output of phase accumulator when the phase increment value is 0000001000000000. It can be observed that the resulting phase value after each clock pulse is four added to the previous phase value. In the following figure initial phase is 0 and further with clock pulses resulting in 4, 8, 12, and 16 ...The output of phase accumulator is added with multiplier output. That output is given to NCO block.

All the blocks are connected with common clock and reset signals. The delta phase value decides the phase increment for each clock pulse. Hence decides the resulting signal frequency. The Frequency modulating instantaneous value is added to the delta phase value which causes instantaneous change in frequency. Due to the digital nature of the modulator only at each clock tick the modulating signal value shall affect the resulting frequency. If the modulating signal is analog then an Analog Digital converter must be used to digitize the modulating signal which can be used in NCO.

4 Low Pass Filter

A low-pass filter is an electronic filter that passes low-frequency signals but attenuates (reduces the amplitude of) signals with frequencies higher than the cutoff frequency. The actual amount of attenuation for each frequency varies from filter to filter. It is sometimes called a high-cut filter, or treble cut filter when used in audio applications. A low-pass filter is the opposite of a high-pass filter. A band-pass filter is a combination of a low-pass and a high-pass.

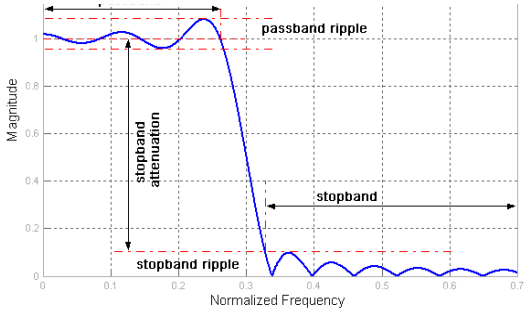

Fig 3.5: Low Pass Filter

V. Decimator (Filtering & Decimation)

There are two main classes of DDC – wideband and narrowband, differentiated by their decimation ratios. As a rough guide, if the decimation ratio is less than 32 consider the DDC wideband; if 32 or more, the DDC is narrowband.The filtering we will perform is different for narrowband or wideband, so is tackled separately. However, the decimators can be treated identically for wideband or narrowband systems.

VI. Designing the Filters

There can be several tools by which the filter coefficients can be finalized for implementing the required FIR filters. In this project the MATLAB's filter design analysis tool (FDA) will be used for designing.

An FIR filter is one whose impulse response is of finite duration. In this filter, the current output (y_n) is calculated solely from the current and previous input values (x_n, x_{n-1}, x_{n-2}...). This type of filter is also said to be non-recursive.

The difference equation, which defines how the input signal is related to the output signal

$$y(n) = b_0 x(n) + b_1 x(n-1) + \cdots + b_P x(n-P)$$

Where P is the filter order, x (n) is the input signal, y (n) is the output signal and b_i are the filter coefficients. The previous equation can also be expressed as

$$y(n) = \sum_{i=0}^{P} b_i x(n-i)$$

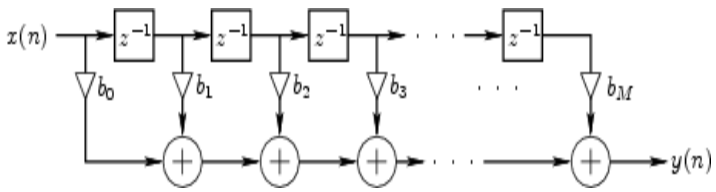

Fig 3.6 Finite Impulse Response Digital Filters

The transfer function allows us to judge whether or not a system is BIBO stable. To be specific the BIBO stability criterion requires all poles of the transfer function to have an absolute value smaller than one. In other words all poles must be located within a unit circle in the *z*-plane.

VII. Multiplier & adder

Here, The output generated by DDC which is multiplied with the generated weights. This output is given to next module as adder which will add all the 16 signals to generate a beam.

VIII. Specifications

Table 1 Beam forming specifications

Parameter	Value	Comments
Input signal type	Band pass signal	Coming from typical superhytrodyne receiver
Input signal frequency range	1.5-3.5 MHz	2 MHz BW and 2.5 Mhz IF frequency value
Sampling rate	10 MHz	
DDC filter size	16 taps	
DDC decimation	4	DDC output sampling rate 2.5 Msps
NCO values: COS	1 0 -1 0	As fo=fs/4
NCO value : - SIN	0 -1 0 1	As fo=fs/4
Number of array elements	16	Linear array as shown in below figure.
Element spacing	3 meters	d as shown in below figure

Table 2 True Angle values of beam

DDS Value	Angle
8	11.25
20	28.125
80	112.5
128	180

IV. Spatran 6e

The Spartan®-6 families provides leading system integration capabilities with the lowest total cost for high-volume applications. The thirteen-member family delivers expanded densities ranging from 3,840 to 147,443 logic cells, with half the power consumption of previous Spartan families, and faster, more comprehensive connectivity. Built on a mature 45 nm low-power copper process technology that delivers the optimal balance of cost, power, and performance, the Spartan-6 family offers a new, more efficient, dual-register 6-input lookup table (LUT) logic and a rich selection of built-in system-level blocks. These include 18 Kb (2x9 Kb) block RAMs, second generation DSP48A1 slices, SDRAM memory controllers, enhanced mixed-mode clock management blocks, SelectIO™ technology, power- optimized high-speed serial transceiver blocks, PCI Express® compatible Endpoint blocks, advanced system-level power management modes, auto-detect configuration options, and enhanced IP security with AES and Device DNA protection. These features provide a low- cost programmable alternative to custom ASIC products with unprecedented ease of use. Spartan-6 FPGAs offer the best solution for high-volume logic designs, consumer-oriented DSP designs, and cost-sensitive embedded applications. Spartan-6 FPGAs are the programmable silicon foundation for Targeted Design Platforms that deliver integrated software and hardware components that enable designers to focus on innovation as soon as their development cycle begins.

The design is functionally verified by simulating the code in ModelSim from Mentor Graphics. The FPGA synthesis is done using Xilinx ISE tool. The synthesis results of ISE are analyzed for timing and area. The hardware output i.e. SPARTAN 6E FPGA output shows on Chip scope pro analyzer.

V. Results

The simulation and chip scope waveforms of beam forming which will show the maximum gain in desired direction and minimum gain in the unwanted direction.

1. **Device utilization summary**

Selected Device	:	6slx16csg324-3
Slice Logic Utilization		
Number of Slice Registers	:	2840 out of 18224 15%
Number of Slice LUTs	:	8139 out of 9112 89%
Number used as Logic	:	7450 out of 9112 81%
Number used as Memory	:	689 out of 2176 31%
Number used as RAM	:	180
Number used as SRL	:	509
Number of unique control sets	:	183
IO Utilization		
Number of IOs	:	58
Number of bonded IOBs	:	58 out of 232 25%
IOB Flip Flops/Latches	:	28
Specific Feature Utilization:		
Number of Block RAM/FIFO	:	28 out of 32 87%
Number using Block RAM only	:	28
Number of BUFG/BUFGCTRLs	:	8 out of 16 50%
Number of DSP48A1s	:	12 out of 32 37%
Total REAL time to execution completion	:	45.00 secs
Total CPU time to execution completion	:	44.47 secs
Total memory usage is 191484 kilobytes		
Number of errors	:	0 (0 filtered)
Number of warnings	:	526 (0 filtered)
Number of infos	:	37 (0 filtered)

2. Simulation results of antenna array module

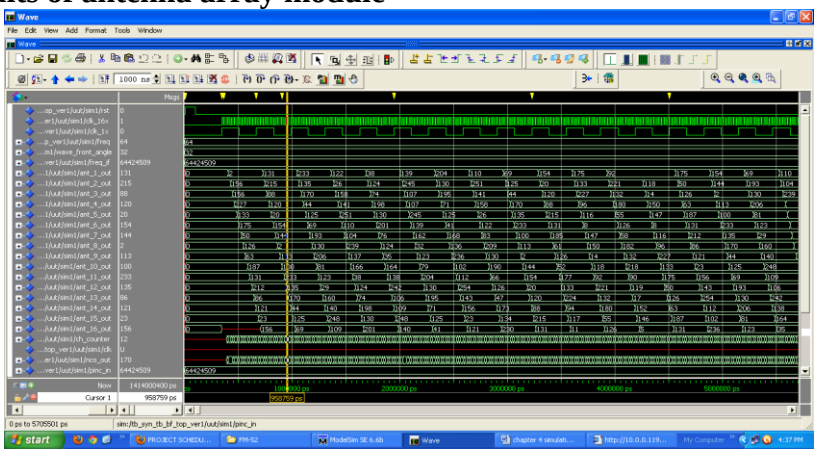

Fig 5.1 Antenna Array Digital outputs

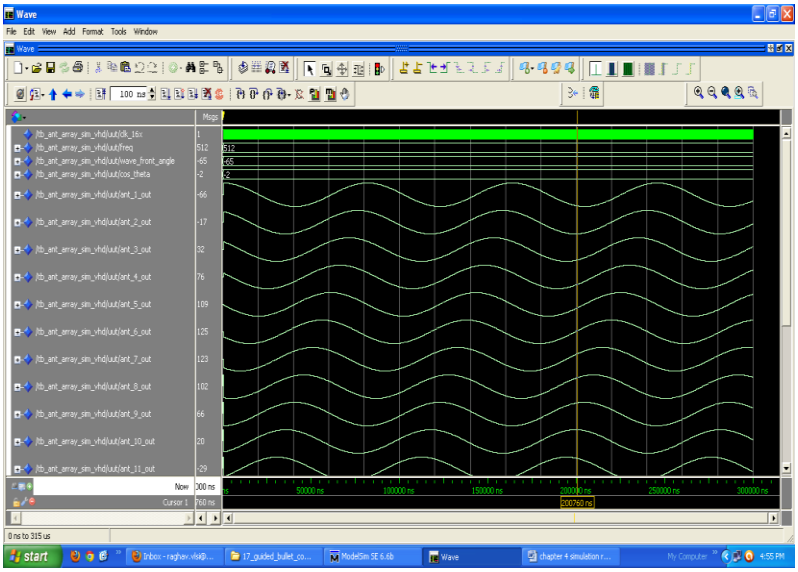

Fig 5.2 antenna array outputs with phase shifts

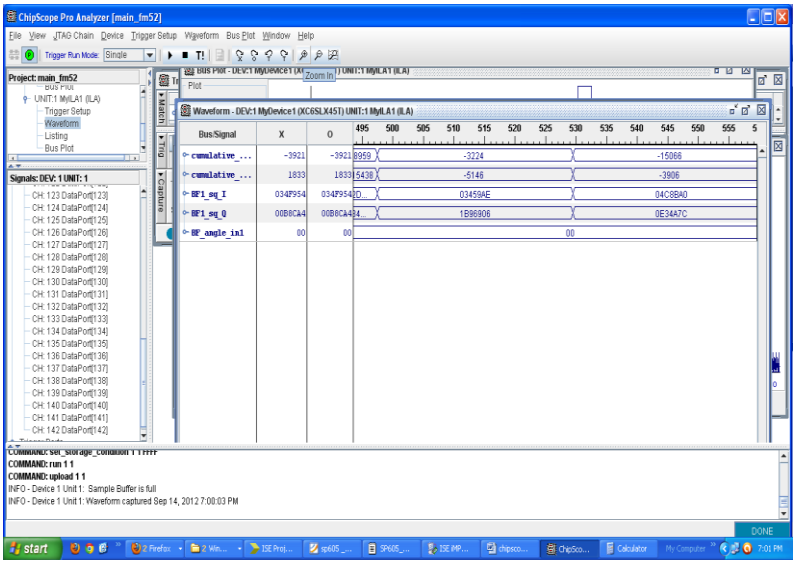

Fig 5.3 Beam forming digital I & q square signals

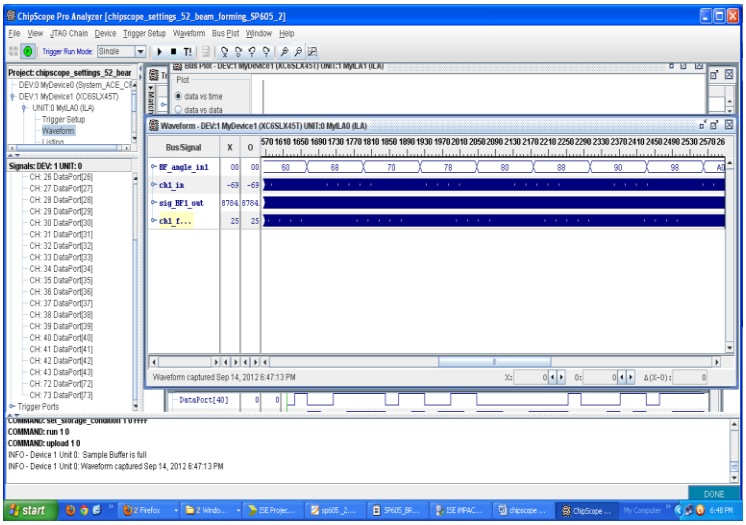

Fig 5.4 Beam forming digital output

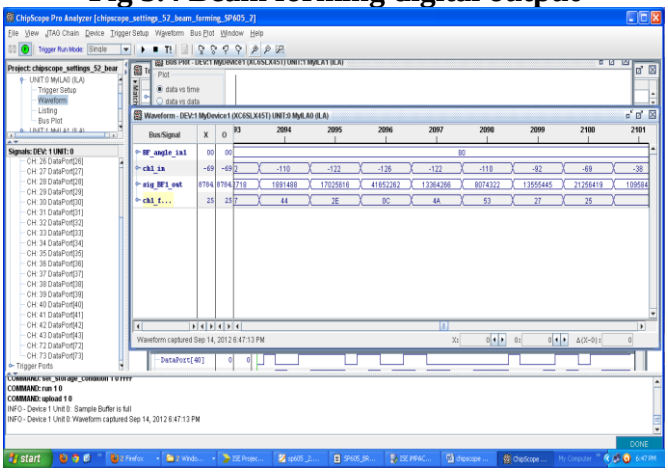

Fig 5.5 Chip scope digital output

VI. Conclusion

In this project has explored the design and implementation of a low-cost digital beam forming platform. The proposed technique employs multiplexed signal processing unit which is time shared for various beam formers. This technique provides simultaneous beams without any compromise on functionality. The low cost of the system facilitates its easy integration into phased array radar systems. The process of beam forming implies weighting these digital signals. In this project, by using 16 antenna input signals we generated digital multiple beams with parallel array processing and we can implement more than 16 antenna input signals. Here we designed the digital beam forming by using the sampling frequency and the digital baseband signals then represent the amplitudes and phases of signal received at each element of the array. The process of beam forming implies weighting these digital signals.

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