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Implementation of Circuit Optimization Technique for Digital CMOS Comparator Using Parallel Prefix Tree Architecture

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Abstract: *The digital comparator using CMOS cells that adopts the parallel prefix tree architecture. This comparator begins from most significant bit towards bit-wise least significant bit when two compared bits are equal. Using circuit optimization technique it reduced by 642 transistors from total area of 768 and also maximum fan-in and fan-out drives of five and four respectively and 1.78mW dynamic power dissipation for 16-bit (N) with 7 CMOS gate delay. The tanner EDA tool simulation for 16-bit is realized using 0.18-µm CMOS process technology with minimum supply voltage of 2.45V.*

I. INTRODUCTION

The digital comparator place an important role which compares two input voltage and generates which is greater/lesser or equal.

A. Types

1) Static Type: a combinational circuit which process input and generates its output without any global signal.

Example: Prefix tree architecture binary comparator

2*) Dynamic Type*: a sequential circuit which process input by any initiative signals like clock, reset etc., and generates its output.

Example: Single clock-cycle binary comparator

B. Applications

Scientific computations, BIST, CPU argument comparison blocks.

C. Existing Systems

Dynamic type comparators will result in heavily loaded clock with number of gated transistors and also no power efficient

- *Two phase clocking scheme* needs large driver for a clock signal routing,
- *Single phase clocking scheme* results in clock skew and more delay and high power consumption. *Static type* comparators slow high transistor count and more data dependencies
- *Prefix tree structure* perform only greater and lesser not for equality,
- *Parallel prefix tree* perform for all comparison result but takes more transistor count.

II. IMPROVED PPT ARCHITECTURE

A. Static type

A minor modification of [1] is done in implememtation structure proposed by Parhami et.al., by using X-NOR with invertor Table 2.and reason for why moving to transmission gate for 2:1 multiplexer by other logic combinations Table 3.are realized here with tanner EDA simulation tool V.7.0.

The basic 8-bit comparison in Figure 1. States that bit-wise competition logic used here from MSB to LSB and stores the compared result in left and right OR network it results in the A or B greater or lesser if any one network is high or if both result not high then 2-input gate shows high that is both bit-width are equal.

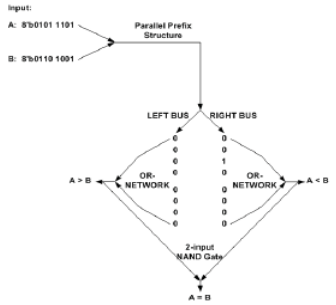

FIGURE 1. 8-B COMPARISON

B. Modification done

Common signals are to be design first that is invertor for all 16-bit obtained and also outputs of various CMOS cells also to be design paralleled and supplied to the logic gates. VLSI DSP architectures techniques like un-folding, re-timing concepts also applied here for circuit optimization.

C. Model Used

The improved system is realized as [2] using tanner EDA simulation tool V7.0 1.25µm technology model file ml2_125.md with minimum supply voltage of 2.5V.

D. Equations

$$\text{Log}_4 N + \text{Log}_{16} N + 4 \text{ CMOS gate delays.} \quad (1)$$

$$\text{Log}_4 16 + \text{Log}_{16} 16 + 4 = 7 \text{ CMOS gate delays.} \quad (2)$$

E. Area, Power, Delay Report

Compared to ppt this improved system reduce 126 transistors and total power consumption of 2.27mW and it has total delay of 7 CMOS gate delay shown in Eqn. (2).

III. SIMULATION RESULTS

```
Including "C:\Users\vijay\Desktop\Final Phase I VV PPT\Tanner\models\models\ml2_125.md"

Device and node counts:
            MOSFETs - 642              MOSFET geometries - 2
               BJTs - 0                          JFETs - 0
            MESFETs - 0                         Diodes - 0
          Capacitors - 0                     Resistors - 0
          Inductors - 0                Mutual inductors - 0
 Transmission lines - 0       Coupled transmission lines - 0
    Voltage sources - 34              Current sources - 0
               VCVS - 0                          VCCS - 0
               CCVS - 0                          CCCS - 0
   V-control switch - 0              I-control switch - 0
      Macro devices - 0       Functional model instances - 0
        Subcircuits - 0             Subcircuit instances - 0
  Independent nodes - 289               Boundary nodes - 35
        Total nodes - 324


Parsing                     0.07 seconds
Setup                       0.14 seconds
DC operating point          1.14 seconds
Transient Analysis          0.04 seconds
-----------------------------------------
Total                       1.39 seconds
```

FIGURE 2. TRANSISTOR COUNT

```
*WEDIT: .tran   1e-008   1e-007
TRANSIENT ANALYSIS
Time<s>              v(AG)<V>      v(BG)<V>      v(EQ)<V>
    0.0000e+000   1.9559e-007   1.9559e-007   2.4995e+000
    1.0000e-010   1.9559e-007   1.9559e-007   2.4995e+000
    1.0000e-008   1.9559e-007   1.9559e-007   2.4995e+000
    2.0000e-008   1.9559e-007   1.9559e-007   2.4995e+000
    3.0000e-008   1.9559e-007   1.9559e-007   2.4995e+000
    4.0000e-008   1.9559e-007   1.9559e-007   2.4995e+000
    5.0000e-008   1.9559e-007   1.9559e-007   2.4995e+000
    5.9999e-008   1.9559e-007   1.9559e-007   2.4995e+000
    7.0000e-008   1.9559e-007   1.9559e-007   2.4995e+000
    7.9999e-008   1.9559e-007   1.9559e-007   2.4995e+000
    8.9999e-008   1.9559e-007   1.9559e-007   2.4995e+000
    1.0000e-007   1.9559e-007   1.9559e-007   2.4995e+000

* BEGIN NON-GRAPHICAL DATA

Power Results
vs from time 0 to 100
Average power consumed -> 2.343513e-003 watts
Max power 2.343513e+006 at time 0
Min power 2.343513e+006 at time 0

* END NON-GRAPHICAL DATA
```

FIGURE 3. POWER CONSUMPTION

IV. RESULT COMPARISON

TABLE 1. X-OR CELL DETAILS

X-OR	X-OR	X-NOR WITH
TRANSISTOR COUNT	12	14
POWER	1.73×10^{-7} µW	2.07×10^{-7} µW

TABLE 2. 2:1 MUX DIFFERENT LOGIC COMPARISON

2:1 MUX	PASS	NAND	NOR	TG
TRANSISTOR COUNT	4	14	14	6
POWER DISSIPATION	4.13×10^{-8} µW	2.27×10^{-7} µW	2.03×10^{-7} µW	7.09×10^{-8} µW

TABLE 3. LOGIC SET REPRESENTATIONS

CMOS CELLS	SET 1	SET 2&3	SET 4	SET 5
MAX. FAN-IN & FAN-OUT	2/4	4/3	5/1	3/2
TRANSISTOR COUNT	14	8	20	12
POWER DISSIPATION	2.07×10^{-7} µW	2.99×10^{-8} µW	2.24×10^{-8} µW	7.09×10^{-8} µW

TABLE 4. NO. OF CELLS COMPARISON

16-BIT	SET 1	SET 2	SET 3	SET 4	SET 5
IMPROVED	16	3	3	16	16
EXIST	16	4	4	16	16

TABLE 5. NO. OF TRANSISTOR COUNT COMPARISON

16-BIT	IMPROVED	EXIST
TRANSISTOR COUNT	642	768

TABLE 6. AREA AND POWER REPORT TABLE

16-BIT	1.25µm 2.5V
TRANSISTOR COUNT	642
POWER DISSIPATION	2.27mW

V. CONCLUSION & FUTURE WORK

The architecture reduces power dissipation and total area consumed for 16-bit digital comparator than existing system. Simulation based analysis conclude that low power system and area consumption is less.

Future work will include circuit optimization like high speed zero detector, etc., to reduce power and delay and to implement the structure in 180 & 150 nm CMOS and TSMC technology with minimum supplied voltage.

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