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Multiple Word Length based low power digital base band receiver

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Abstract: *In recent years power consumption in CMOS VLSI circuits has become a major design constraint. This is in particular important for mobile wireless communication systems, due to the limited life time of the batteries to power wireless communication equipment. The circuit designers came with suitable low power strategies to achieve low power design. These circuit level techniques are readily available in the form of standard cells to the Register Transfer Level (RTL) designer. Currently designers are exploring the algorithm level and architecture level techniques towards arriving at low power communication Integrated Circuits (ICs). The Word Length Optimization (WLO) is an algorithmic approach with promising power saving levels, suitable for communication applications. The work presented here demonstrates power optimized RTL design for wireless base band receiver using Quadrature Phase Shift Keying (QPSK) modulation scheme. The novel method of arriving at suitable word lengths based on system level parameters at each signal stage is demonstrated. The Symbol Error Rates (SER) for given energy per symbol are analyzed. The Xilinx Zynq-7 Family FPGA is used for area, power and performance analysis. The peak power optimization of 40% is reported for Es/No = 8 dB, in comparison to the normal design.*

Keywords: *Base band receiver, Low power VLSI, Multiple word length optimizations, SNR degradation, Word Length Optimization*

I. Introduction

The low power Very Large Scale Integration (VLSI) is the most important technology area for development of modern mobile communication system design. The circuit designers came with suitable low power logic families such as Complementary metal Oxide Semiconductor (CMOS), and further adopted clock gating type of techniques to achieve low power design. The continuous research in the device and circuit design techniques resulted in several low power topologies suitable for wide category of applications.

These circuit level techniques are readily available in the form of standard cells to the Register Transfer Level (RTL) designer. As the VLSI ICs are becoming complex, designers are preferring to move to higher abstraction level. Towards exploring low power options, designers are seeing potential advantages while working at algorithm level and architecture level. For example at circuit level to perform 8 bit addition, the designer attempts best methods for implementing 8 bit addition by using low power logic gates. When the designer can work at algorithm level, the necessity for 8 bit addition will be examined. Considering the algorithmic performance or system level requirements if the addition can be made 6 bit instead, this can result in considerable power saving. This example explains the key principle in Word Length Optimization (WLO) based techniques.

The present day communication system related algorithms are complex and require great attention to achieve low power implementation, with graceful degradation in system performance. Currently designers are exploring the algorithm level and architecture level techniques towards arriving at low power communication Integrated Circuits (ICs). The Word Length Optimization (WLO) based techniques are promising and being attempted by several researchers.

In a typical communication system the distance between receiver and transmitter can range anywhere between, few meters to few hundreds of kilometers. The input signal received is very large when the receiver is close to transmitter and very small when it is far. Hence number representation with high dynamic range is required. Typically 80 dB dynamic range is processed in communication receivers. A practical ADC of 16 bit is used for this purpose in receiver digital front end.

As the channel is noisy, the signal available at receiver has noise energy mixed in it. In a typical receiver chain there are several stages of amplification and frequency translation. The signal to noise ratio (SNR) available at receiver decides the performance of communication system. The blocks in receiver chain either improve the SNR or reduce. Usually amplifiers, mixers and attenuators which are found in receiver front end reduce the SNR, which is accounted through noise figure. As a result, the signal at ADC output in receivers has high dynamic range (hence higher word length) but less SNR.

The dynamic range of a system is the ratio of the maximum signal power to minimum signal power that is of interest. The dynamic range determines the signal levels over which the receiver need to be sensitive for processing the signal. As this number is larger in value usually it is expressed in dB scale as given in (1).

$$\text{Dynamic Range (DR) } in\ dB\ scale = log_{10}\left(\frac{P_{max}}{P_{min}}\right) \quad (1)$$

Usually the ADCs are designed to accept input with certain dynamic range and produce output binary words. The input analog circuit which performs signal conditioning (amplification or attenuation and adding offset) decides the true power level over which the ADC can function. The number of ADC bits decide the granularity level at which the analog voltage can be measured. The resolution defines the smallest signal change that can be measured. The accuracy with which the analog to digital conversion takes place is decided by the resolution. The values of accuracy and dynamic range can be either computed in voltage levels or in power scale by considering the input impedance of ADC (which is 50Ω or 75Ω in most of the cases).

For a given application, the signal processing requirements demand a certain dynamic range and accuracy. The number of bits selected from ADC bits and further word lengths in every stage of processing need to consider these requirements, while achieving the optimization. This dynamic range is generally smaller than the total dynamic range offered by system. As the system is supposed to accept input right from lowest power level to highest power level, the system level dynamic range is higher.

Taking the ratio of Root Mean Square (RMS) value of full scale input to RMS value of quantization noise [1] and all other harmonics the resultant maximum Signal to noise (SNR) ratio can be given through the equation. Where N is the number of ADC output bits, q is quantization noise.

$$\text{SNR(dB)} = 20\log\frac{\text{rms signal}}{\text{rms noise}} = 20\log\left(\frac{\left(2^{N-1}\times\frac{q}{\sqrt{2}}\right)}{\frac{q}{\sqrt{12}}}\right) = 6.02N + 1.76 \quad (2)$$

Since the beginning IC design for digital communication applications, several researchers attempted the problem of low power VLSI in different dimensions. The relevant research articles, which emphasize either on low power receiver design through higher abstraction algorithm level techniques or word length based optimization (WLO) methods are discussed in this section. These two are the related dimensions for the proposed optimization technique, in the context of low power communication system design. However the literature and also the proposed technique can be generalized to implementation of any digital signal processing (DSP) algorithm.

The effort towards handling the run time changing signal energy levels with adaptive word selection by employing dynamic scaling of ADC digital data is presented at [2]. The present work is continuation of this research towards complete receiver's optimization. The work given at [3] discusses the usage of ROM less architecture, with single path delay feedback method for low power FFT implementation in OFDM based wireless communication applications. The method doesn't propose a generalization of such optimization for other communication applications.

The power reduction techniques in radio receiver design at higher abstraction levels considering the system level parameters is attempted by several designers in different dimensions. The work published at [4] presents a low IF based design for given signal and interference conditions. The work given at [5] discusses wake up scheme for receiver in wireless sensor network applications. However it is to be noted that, in most of the applications the required performance is well known in advance and embedding SNR estimation logic at runtime results in additional power consumption.

In realizing communication applications majority of the silicon is occupied by the signal processing operations which are highly computational intensive and influence the total power dissipation considerably. Most arithmetic operations implemented on ASIC/FPGAs are based on fixed-point arithmetic representations as they occupy less area and burn less power. Whereas floating-point representation based arithmetic circuits are considerably larger and slower than their fixed-point counterparts for a given bit-width.

In communication applications, where signals with large dynamic range need to be processed, the fixed-point representation with wider word length is used. However due to the presence of noise in the signal, the full accuracy levels of signals represented with long word lengths do not contribute for improvisation of algorithms. More over the higher word length result in higher power dissipation. The power optimization is possible by optimum word length selection [6][7] either in FPGAs or ASICs.

The number of bits used to represent the signal, at various stages of algorithms decides the resolution of system. In a typical communication system the bit size grows with each arithmetic operation (addition, multiplication, accumulation etc.) resulting in wider buses.

The Word Length Optimization (WLO) problem is traditionally considered as, the selection of bit widths based on the interval growths after each arithmetic operation of data path. The word length allocated at each signal stage directly affects two parameters; maximum representable value and accuracy.

The HLS approach for RTL generation is one of the emerging VLSI front end design approach, which is aimed to cut down the VLSI front end design cycle time considerably. However the optimization of generated RTL for power and speed are critical aspects for the success of the HLS based approach. The word length optimization in HLS based approach is under research from last two decades. Several approaches [8][9][10][11][12] were evolved and further optimization is under research. Existing optimization algorithms established methods for floating point to fixed point mapping under given constraints. The computation time to arrive at optimum word length is also concern in the HLS tool chain. Few recent works published towards WLO are discussed in this section. Considering all the approaches the WLO methods can be classified in to two categories.

(1) Analytical
(2) Simulation based approach

The analytical methods utilize selected analytical properties of the operations comprising the given algorithm [13]. Analytical methods usually result in more conservative word lengths, as they use worst case ranges and error models of operators in a design. They are often faster and can guarantee a lower bound for the error. However these methods directly cannot result in optimal hardware.

The simulation based methods simulate the design with a set of input stimuli and track the minimum and maximum values attained by each signal in the data path. Based on these values the suitable word length can be computed. This leads to designs that are close to the optimum [14] but no error bound can be guaranteed. If the tight word lengths are selected based on simulation, then overflows may occur. Hence usually additional few bits will be considered for deciding the worst case signal values. In algorithm transformation from DSP to ASIC [15] this is the popular method.

The estimator presented at [8] uses Affine Arithmetic (AA) to provide a Signal-to-Quantization Noise-Ratio (SQNR) estimation for differentiable non-linear algorithms with and without feedbacks. The estimation is based on the parameterization of the statistical properties of the noise at the output of fixed-point algorithms. In paper [16], a simulation-based technique based on the relaxation of the confidence requirements of the simulations in some stages of the evaluation is presented. This work is aimed to reduce the simulation time. A WLO technique to handle constants and variables in Linear Time Invariant (LTI) systems for given range and precision is given at [7]. However the paper doesn't propose generalized approach to optimize the bit length against given SNR values.
The paper given at [17], depicts specification of arithmetic circuits and explains the techniques for verification and bit optimization in arithmetic circuit designs. An algorithm given at [10] minimizes the hardware resources of fixed-point operations for a given accuracy constraints. The work uses weighted search algorithm, which can minimize the hardware resources for a specific FPGA by using weights.

The problem of WLO in realizing specific DSP blocks is also addressed by several researchers. The work published at [18] reduces the area for FFT implementation by varying the fixed-point length of the phase factors using phase angle error percentage as criteria. The paper at [11] exploits the Gaussian nature of OFDM signals to predict the bit-growth of the signal through the various stages of the FFT and propose a technique to scale the signal appropriately. The Sardana [12] tool optimizes the arithmetic expressions present in source codes. The optimization is done by synthesizing automatically new mathematically equal expressions, given ranges of values for the variables. The tool minimizes the number of bits required to represent without overflow the integer parts of the fixed-point numbers possibly occurring at any stage of the evaluation of an expression. However the tool do not propose any optimization criteria based on SNR values at various stages.

The work presented in this article, demonstrates power optimized RTL design for wireless base band receiver of Quadrature Phase Shift Keying (QPSK) modulation type. Three different architectures are compared for demonstrating the proposed method. The normal architecture implements uniform word length based data paths with 16 bit signal widths. The second architecture is WLO based design for input signal with Energy per symbol to Noise power spectral density ratio (Es/No) equals to 12 dB. The third architecture is WLO based design for input signal condition with Es/No value equal to 8 dB. The section II, discusses the high level architecture and module level details of implemented QPSK digital base band receiver. The section III, gives details of proposed WLO algorithm. The section IV has details of simulation and synthesis results. The last section concludes the work.

II. QPSK Digital Base Band Receiver

The present radio, broadcast and mobile communication system design is built around the principles and architectures of software defined radio (SDR). In SDR design approach, the signal is digitized after translating the signal from radio frequency (RF) band to intermediate frequency (IF) band, with superheterodyne approach. The ADC digitizes this signal at base band. In this paper the Zero IF signal is considered as input for the receiver.

In current mobile standards, popularly used digital modulation schemes are phase shift keying (PSK) and Quadrature amplitude modulation (QAM) variants. Both of these two come under linear modulation category, which can be represented in quadrature form as given in equation (3).

$$s(t) = I(t)\cos(2\pi f_0 t) - Q(t)\sin(2\pi f_0 t) \tag{3}$$

This is the general form for input to the base band receiver, where the I and Q correspond to inphase and Quadrature phase values. The COS and SIN components are resultant due to carrier residue, which will be removed in carrier recovery stage. Optimization principles while processing base band I and Q components applicable to one linear modulation type are applicable to all other variants. Considering these aspects, the QPSK base band receiver architecture is considered for illustrating the proposed optimization method.

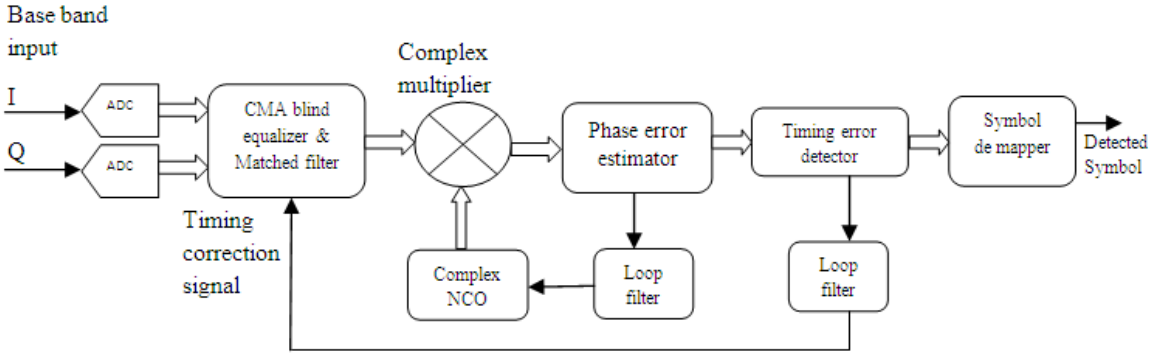


Figure 1. High level architecture of Digital base band receiver for QPSK

The blind adaptive channel equalizer is built with constant modulus basis is implemented here.. The algorithm in its complex form (I + jQ) is implemented here for demonstrating the principles of proposed WLO scheme. The WLO is applied on the I and Q values and optimum bit widths are computed and used in the data path implementation.

The Constant Modulus Algorithm (CMA) is stochastic gradient-descent type, which adjusts the equalizer filter coefficients in the direction of the negative gradient. The algorithm can be defined as given in (4). Where μ is the step size, ∇_W is the gradient with respect to the equalizer tap coefficients, J is the cost function of the algorithm, and e(n) is the error signal of the algorithm, while (.)* denotes complex conjugation. The iterative computations of filter coefficients w(n+1) from previous cycle coefficient values w(n) is described in (4).

$$\begin{aligned} w(n+1) &= w(n) + \mu(\nabla_W J) \\ &= w(n) + \mu e(n) x^*(n) \end{aligned} \tag{4}$$

As the e and x are complex, the equation will have real and imaginary components. Elaborating the (4) with real and imaginary parts results in (5). The error at each step is computed as given in (6). The filter coefficients are updated after every clock cycle.

$$w(n+1) = w(n) + \mu\, e_R(n)\, x_R(n) + \mu\, e_I(n)\, x_I(n) + j\,(\mu\, e_I(n)\, x_R(n) - \mu\, e_R(n)\, x_I(n)) \tag{5}$$

$$e(n) = y_R(n)\,(C - y_R^2(n) - y_I^2(n)) + j\, y_I(n)\,(C - y_R^2(n) - y_I^2(n)) \tag{6}$$

The phase error estimation is performed with inverse tan function implemented with look up table. The loop filter for phase correction and timing correction consists of Proportional-Integral (PI) loop control. The proportion term and integral term gains can be modified at run time, by using external ports of RTL modules. The Square Root Raised Cosine (SRRC) filter is used for matched filtering. The zero crossing timing error detector is used for timing error detection.

The total design is implemented using Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL) and instantiated in Simulink using blackbox component. The Generic feature in VHDL is used to alter the bus widths at each stage based on the WLO algorithm.

III. Proposed WLO Algorithm

The proposed algorithm considers the computational graph as general form for representation of given VLSI implementation of signal processing algorithm. The quantization noise resulting with bit truncation is considered along with noise present in signal to define signal to quantization noise ratio (SQNR). The proposed approach uses SQNR as the basic metric to decide the required number of bits at each signal stage. From the system level specification, such as expected symbol error rate (SER) the final output signal stage SQNR is computed. From output stage the WLO algorithm back traverses to compute SQNR after each node. The node contribution to the increase or decrease in SQNR is pre-computed in the form of processing gains. From the

SQNR values at each stage the word length are computed. All the word lengths in the forward paths of the receiver are computed with this method.

The recursive paths are present in equalizer and timing error adjustment blocks. Considering the maximum equalization requirements, the word length of coefficient's are pre-computed. Based on this the processing gains of even these recursive blocks are made available for the WLO algorithm. Similarly considering the worst case timing error detection requirements ,the word lengths in these paths are decided. With these approaches the circular dependencies of the recursive paths are resolved.

ALGORITHM. MULTIPLE WORD LENGTH (MWL) BASED ALGORITHM

Input: Data Flow Graph G(V, S), and required performance factors of total system (CNR, SNR, DR, BER, SER). Also the tables for performance factors link up to implementation parameters (Es/No Vs SER)
Output: Word length values at each signal $j \in S$ (n_j, q_j)

INITIALIZE : initial processing gain = 0, n_j to maximum value
FOR EACH i = $V_I \rightarrow V_O$ (INPUT NODE $V_I \rightarrow$ OUTPUT NODE V_O)
IF RECURSIVE // such as adaptive filter
Processing Gain $PG_i = PG_{i-1} + MAX\_EXPECTED\_PG_V$
ELSE
Processing Gain $PG_i = PG_{i-1} + PG_V$
END
END

FOR EACH i = $V_O \rightarrow V_I$ (OUTPUT NODE $V_O \rightarrow$ INPUT NODE V_I)
$SQNR_O$ = f (required system level performance aspects at output) // Compute SQNR at output node

INITIALIZE : $WL_O = SQNR2BIT(SQNR_O)$
WHILE V_i ~= input node // until we reach input node

$SQNR_i = SQNR_{i+1} - PG_{Vi}$
$WL_i = SQNR2BIT(SQNR_i)$
END
END

CNR=Carrier to Noise Ratio
SNR=Signal to Noise Ratio
DR=Dynamic Range
Es/No=Energy per symbol to Noise power spectral density ratio

The RTL code modules of base band receiver along with additional Simulink blocks are simulated using Xilinx System Generator (XSG) tool and results are presented in next section. To prove the area and power optimization of WLO algorithm, the input SNR and targeted SERs are varied over steps and results are analyzed.

IV. Simulation And Synthesis Results

The functional validation of the design is carried out using Xilinx ISE simulator invoked under Xilinx System Generator (XSG) and resulting symbol error rates (SER) are observed. The total setup for generating the QPSK test signal at base band level is shown at Fig. 2.

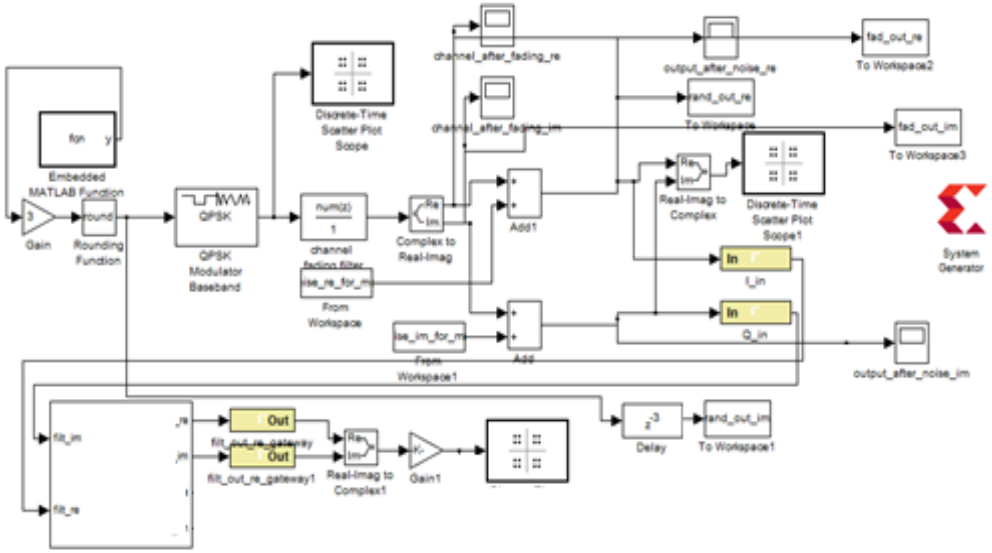
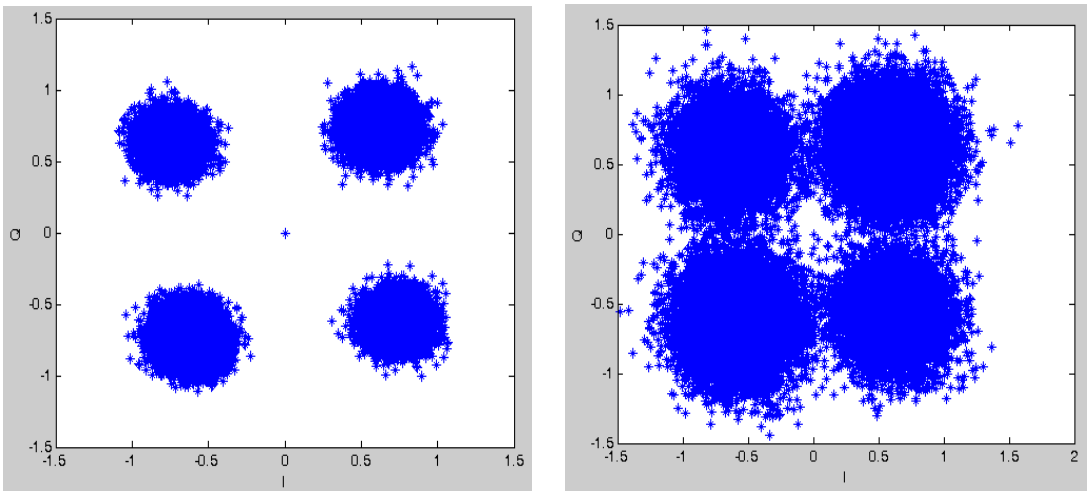


Figure 2. Xilinx system generator top level test bench

The Fig. 3, and Fig 4 has output constellation results for Es/No =12 dB condition and Es/No = 8 dB condition respectively. Since the Es/No is more relevant specification for SER analysis the SNR values are converted to Es/No scale.



for Es/No =12 dB for Es/No =8 dB

Figure 3. QPSK demodulator result (constellation).

From above graphs it is clear that when the low SNR signal is applied the bit widths in receiver architecture are reduced with graceful degradation of bit detection capabilities. It can be seen that at Es/No level set to 8 dB the received constellation points are highly spreaded due to the noise present in input signal and also the quantization noise resulting due to reduced bit widths. Since in QPSK only the sign of I and Q are sufficient to decode the bits, the detection is possible even for 8 dB level.

The Xilinx 7 series Zynq XC7Z020 FPGA considered for synthesis and power analysis. The Xilinx Xpower analysis tool is used to analyze the design for power analysis. The power reported for un-optimized design is 752 mW. Whereas after optimization for Es/No 12 dB the power reported is 587mW. In the full optimization case for Es/No 8 dB, the power reported is only 443mW. This shows 40% power saving when compared to normal design, with uniform word length based approach consisting 16 bit data paths.

V. Conclusion

A method and algorithm based on word length optimization and communication system performance aspects are presented for wireless base band digital receiver. The architecture consists of blind adaptive equalizer with constant modulus algorithm, with recursive data paths in it. The proposed algorithm demonstrates the multiple word length based optimization for both direct and recursive type data paths. The Xilinx System

Generator (XSG) environment is used for simulation and symbol error rate analysis. The Xilinx's ISE tool suite is used for synthesis and power analysis. The 7-series Zynq SOC is used for benchmarking the performance of the proposed method. The peak power optimization of 40% is reported for Es/No = 8 dB, in comparison to the normal design. The demonstrated method shows promising direction of low power optimization of wireless receiver design which can used in mobile communications, wireless sensor networks and other VLSI implementation of signal processing algorithms. The work is part of ongoing research aiming to evolving WLO based low power wireless base band receiver architecture. The work is aimed to be continued for further simulation and validation for lower SNR values.

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