IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 4, Issue 4, Ver. III (Jul-Aug. 2014), PP 31-37
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Sub Threshold Shift Register Design Using Variable Threshold MOSFET Approach

Ragini. K 1[a*] , Dr. Satyam. M 2[b] , Dr. Jinaga.B.C 3[c]
[a] *G. Narayanamma Institute of Technology & Science, Department of Electronics and Communication Engineering, Hyderabad, India*
[b], *Professor, Vasavi college of Engineering, Hyderabad, India*
[c] *Former Professor, Jawaharlal Nehru Technology University, Hyderabad, India*

Abstract: *Dynamic threshold MOS (DTMOS) circuits provide low leakage and high current drive , compared to CMOS circuits, operated at lower voltages. This paper proposes a modified DTMOS approach called Variable threshold MOSFET (VTMOS) approach. The VTMOS is based on operating the MOS devices with an appropriate substrate bias, which varies with gate voltage by connecting a positive bias voltage between gate and substrate for NMOS and negative bias voltage between gate and substrate for PMOS. With VTMOS, there is considerable reduction in operating current and power dissipation, while the remaining characteristics are almost the same as those of DTMOS. Results of our investigations show that VTMOS circuits improves the power up to 50% when compared to CMOS and DTMOS circuits, in sub threshold- region. The performance characteristics of VTMOS shift register- The Power dissipation, Propagation delay and Power delay product have been evaluated through simulation using H spice. The dependency of these parameters on frequency of operation has also been investigated.*

Keywords: *Sub threshold, Dynamic threshold MOS Inverter, Propagation delay, Noise-margin ,Variable threshold MOS Inverter, Power dissipation.*

I. Introduction

Over the past two decades, semi conductor industry emerged considerably and demand for VLSI has grown all over the world. During the recent years. there is a great demand for portable devices like cellular phone , palm top computers, GPRS receivers, pocket calculator, and pacemakers. They all demand for low power. Hence low power design has emerged as a very attractive and fast development field. The limited battery life time demands for the reduction of power consumption of portable devices. High performance digital systems such as DSP, microprocessor's, and other applications insists for low power design. Besides this, the environment also demands for low power design. As the electronic equipment usage increases, the power consumption and the cost for excessive cooling system increases.

In view of this it is essential to minimize the power dissipation. The various techniques that are employed to reduce the power dissipation are recycling the energy that might be stored in nodal capacitances, reduction in transitions (0 to 1 or 1 to 0), reduction in voltages and currents , and so on. The techniques based on operation at very low currents usually below the normal conduction region, especially in FET based circuits is known as sub threshold operation [1,2]. This has attracted several investigators, as it has flexibility to choose their own logic levels and power dissipation .Driving CMOS circuits with sub threshold leakage current can provide order's of magnitude power reduction over standard strong inversion CMOS circuits [3,4]. Many researchers focused on achieving low power with high speed [5,6, 7,8]. They have proposed different circuits to improve current drive and showed that delay has come down compared to CMOS circuits Assaderaghi.F[9], I..Chung[10] , A.Drake[11] and M.R.Casu [12] has proposed circuits to improve the current drive and showed that the delay has come down compared to CMOS inverters. This in turn has resulted in some increase in the power dissipation .The additional transistor's lead to more complexity in the above case. Hence Soleimani [13] proposed a new inverter scheme, with drains connected to substrate. He claims that he achieved better power delay product compared to other circuits.

This article is only an attempt to modify the normal sub threshold operating condition to reduce the power dissipation without affecting the performance. The modified operation that is suggested is based on biasing the substrate of FET dynamically in tune with the gate voltage. This we termed as variable threshold MOS operation. It has been shown that VTMOS operation can result in power saving of up to 50% compared to CMOS operation and can be used in cascadable circuits like CMOS circuits. The article describes this effort in the following sections. First the structure of CMOS,DTMOS and VTMOS configurations are given .current-voltage characteristics of the MOS devices under VTMOS operation have been obtained through simulations in the next section .Later using these characteristics VTMOS Serial-in-serial-out Shift Register has been

constructed and its performance has been measured through simulations .At the end it has been concluded that the VTMOS circuits can provide the benefits of DTMOS and also results in low power dissipation with marginal increase in propagation delay.

2.0 STRUCTURE OF CMOS, DTMOS AND VTMOS CONFIGURATION

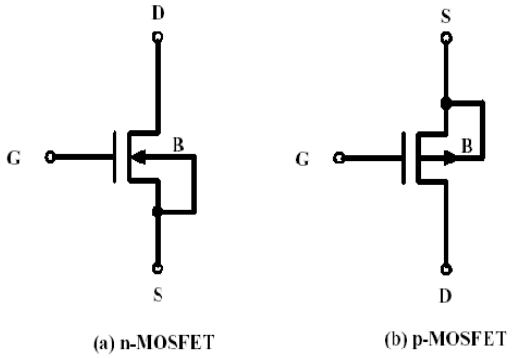


Fig 1(a) - CMOS Structure

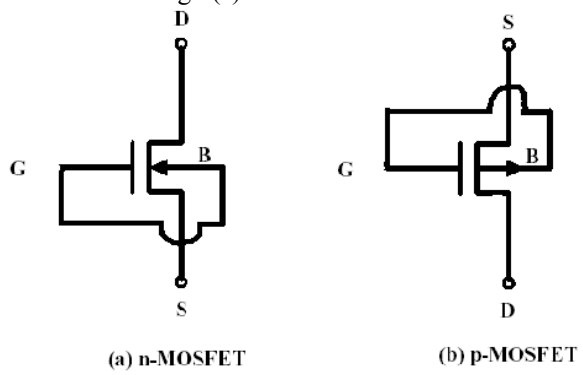


Fig 1(b) - DTMOS Structure

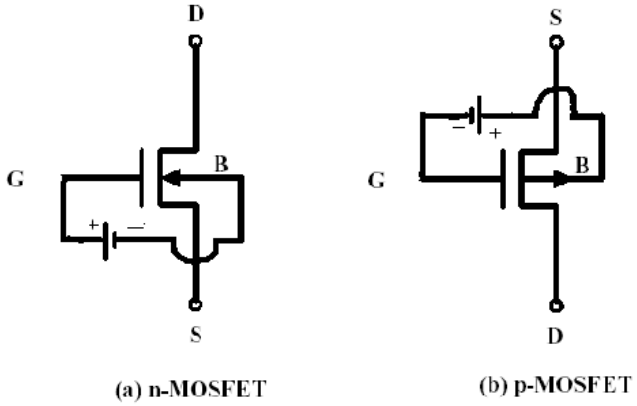


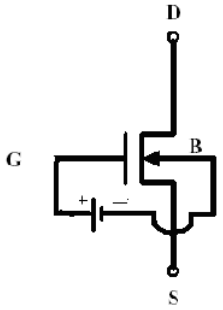
Fig 1(c) - VTMOS Structure

Typical schematic structures of CMOS, DTMOS and VTMOS are given in Fig 1(a), 1(b) and 1(c). In conventional NMOS circuit, Fig 1(a), the substrate is normally connected to ground or lowest potential in the circuit and in PMOS circuits, the substrate is connected to supply voltage or the highest potential in the circuit. In DTMOS, Fig 1 (b), the substrate is always kept at gate potential. So when gate potential is varied, substrate potential also varies [14].Variation in substrate potential results in variation in threshold voltage and hence the transfer characteristics of DTMOS are different from that of conventional CMOS devices [15].VTMOS is nothing but an extension of DTMOS in the sense that the substrate voltage differs always by a constant voltage from the gate voltage as shown in Fig 1(c).With VTMOS approach, there is a considerable reduction in operating current and power dissipation, compared to CMOS and DTMOS approach.

II. Current Voltage Characteristics Of NMOS Transistors Under VTMOS Operating Conditions In Sub-Threshold Region:

To evaluate the behavior of NMOS and PMOS devices under VTMOS operating conditions, the current voltage characteristics are measured and plotted using H spice simulation tool. The transistor's are chosen from 65nm technology. The threshold voltage for NMOS and PMOS devices are 0.22v and -0.22v respectively. The width of NMOS (Wn) and PMOS(Wp) is chosen as 200nm and 400nm respectively. The supply voltage is taken as 0.2v which is below the threshold of both the devices.

2.1 Current voltage characteristics of NMOS devices under VTMOS operating conditions:



(a) n-MOSFET

Fig 2

As shown in Fig 2, the NMOS transistor is connected to gate through $V_{AN,}$ which bias the substrate negative with respect to gate. For different values of V_{AN} starting from 0 to 0.2v, the current voltage characteristics of NMOS, i.e Id verses Vgs are plotted and given in Fig 3.

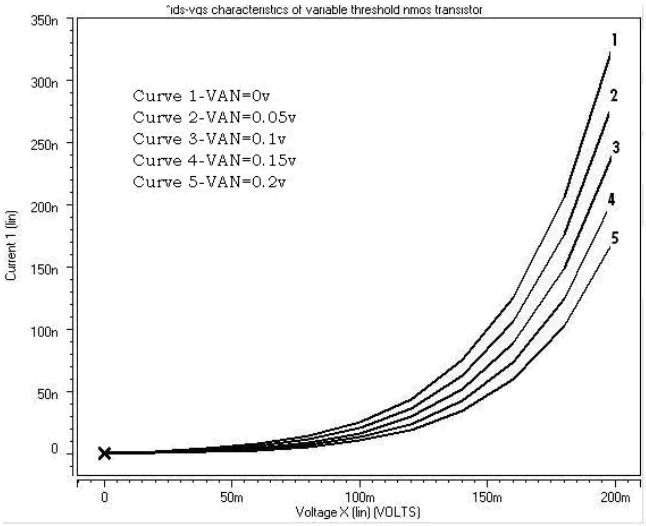


Fig: 3 Ids-Vgs curves of Variable Threshold NMOS Transistor (V_{AN} varying from 0(top)to 0.2v(bottom))

When V_{AN} is varied from 0 to 0.2v, the transistor substrate bias is dynamically adjusted, depending on the gate voltage, causing the threshold voltage of the device to adjust dynamically. The variation in threshold voltage causes variation in leakage currents and power dissipation. The VTNMOS transistor is operated in two modes i.e ON mode and OFF mode .As the entire operation is limited to sub threshold region , for a given $V_{AN,}$ the 'ON' condition is defined for NMOS transistor when Vgs=0.2v.Similarly for a given $V_{AN,}$ 'OFF' condition is defined for NMOS transistor when Vgs=0v. In the 'ON' mode ,when V_{AN}=0.2v and Vgs=0.2v,then the substrate bias of NMOSFET transistor is switched to 0v. In this condition, the VTNMOS transistor is similar to NMOS ON transistor operation. Hence the drain current of VTNMOS is same as NMOS transistor under normal conditions and is found to be 171nA . For the condition ,that V_{AN}=0v and Vgs=0.2v(DTNMOS condition),the source and substrate of MOSFET is forward biased, which implies that the effective threshold voltage of the device is reduced. hence one expects much higher current than the current that flows under normal NMOS operation(Vgs=0.2v).This current has been found to be 334nA from the Fig (3).The OFF condition of the transistor in this article is defined as the condition in which Vgs = 0 and V_{AN} is varied from 0 to 0.2v.when Vgs=0v and V_{AN}=0V,the condition corresponds to normal NMOS transistor .when V_{AN}=0.2v,the substrate is

biased negative w.r.t source by -0.2v and hence the threshold voltage increases and the current decreases further .From the Fig(3),the value of current for Vgs=V_{AN}=0 is measured as 1.4nA and for Vgs=0v and V_{AN}=0.2v it is 550pA, which is about one-third of the leakage current ,when the substrate is biased at 0v.

III. 3.0 VTMOS Serial In Serial Out Shift Register

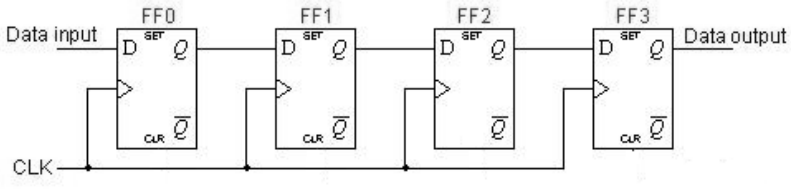


Fig 4-VTMOS Serial in Serial out Shift Register-circuit diagram

The VTMOS logic approach is applied for Serial in Serial out Shift Register, which is shown in Fig 4 .The construction and operation of the circuit is given below.

3.1 Circuit operation of Serial in Serial out Shift Register

A basic four-bit shift register can be constructed using four VTMOS D flip-flops. The circuit operation can be explained in this section. The input data is applied sequentially to the D input of the first flip-flop on the left (FF0).The process of entering the digital word starts with the data input corresponding to the least significant bit(0)at the serial input and first clock pulse. The input corresponding to each bit is applied till the most significant bit is reached and the bits go on shifting from left to right at the falling edge of each clock pulse .Thus during each falling edge of clock pulse, one bit is transmitted from left to right .This is continued until all the input bits are applied. The operation of VTMOS Serial in Serial out Shift Register has been verified by giving a typical input pattern and is described below in the following section.

3.2 Input output wave forms for VTMOS Serial in Serial out Shift Register

The performance of VTMOS Serial in Serial out Shift Register has been studied and verified with the inputs taken in the form of pulses varying between 0 and 0.2v, with a rise and fall time of 25ns, and also compared with that of conventional CMOS Shift Register circuit. The width of VTNMOS and VTPMOS transistors are chosen as 200nm and 400nm respectively . As in the case of combinational circuits, the supply voltage is 0.2v and load capacitance is 10fF. The input pattern chosen for analysis of performance parameters is D=101101 at a pulse period of 10 μ seconds and clock is applied at a pulse period of 5 μ seconds .The output wave forms are plotted for all Serial in Serial out Shift Registers (VTMOS Serial in Serial out Shift Register for VAN=VAP=0v, VTMOS Serial in Serial out Shift Register for VAN=VAP=0.2v, and CMOS Serial in Serial out Shift Register) for a period of 200 μ seconds and is shown in Fig 5(a), Fig 5(b) and Fig 5(c).

In the above figures 5(a), 5(b) and 5(c), J corresponds to D input and cp corresponds to clock input and v8, v8a, v8b and v8c corresponds to flip flop outputs, FF0, FF1, FF2 and FF3.

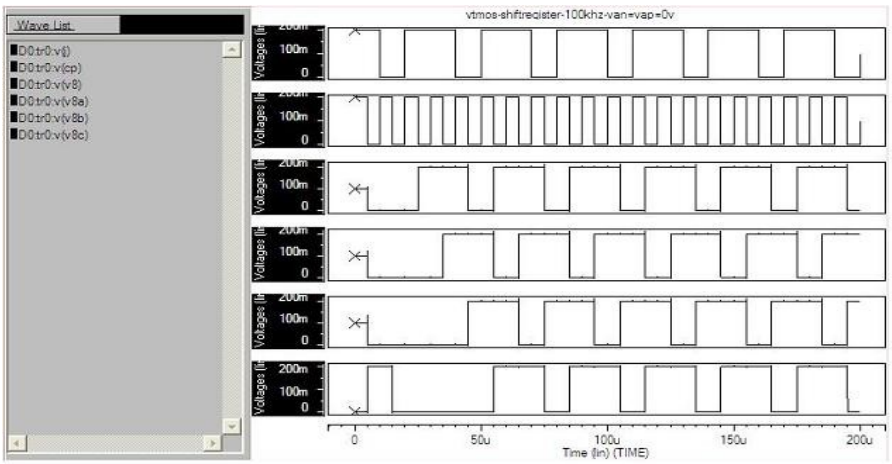


Fig5(a) : Input and Output waveforms of VTMOS Serial in Serial out Shift Register (|VAN|=|VAP|=0V)-100KHZ

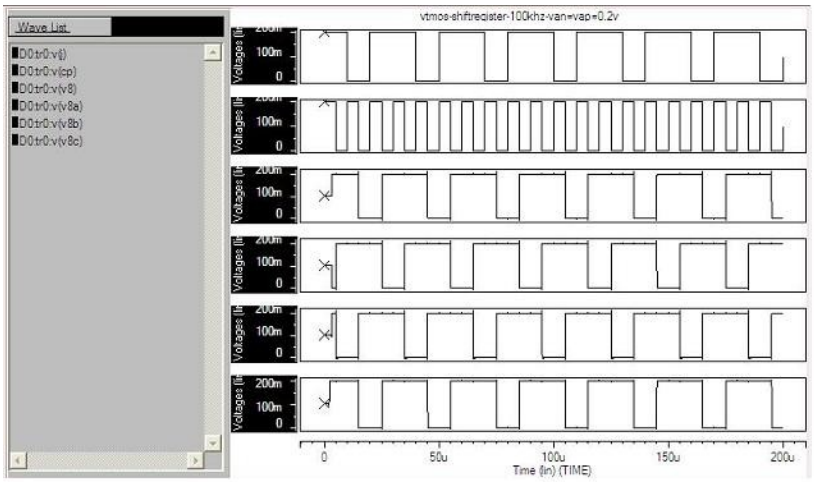


Fig5(b) : Input and Output waveforms of VTMOS Serial in Serial out Shift Register (|VAN|=|VAP|=0.2V)100kHz

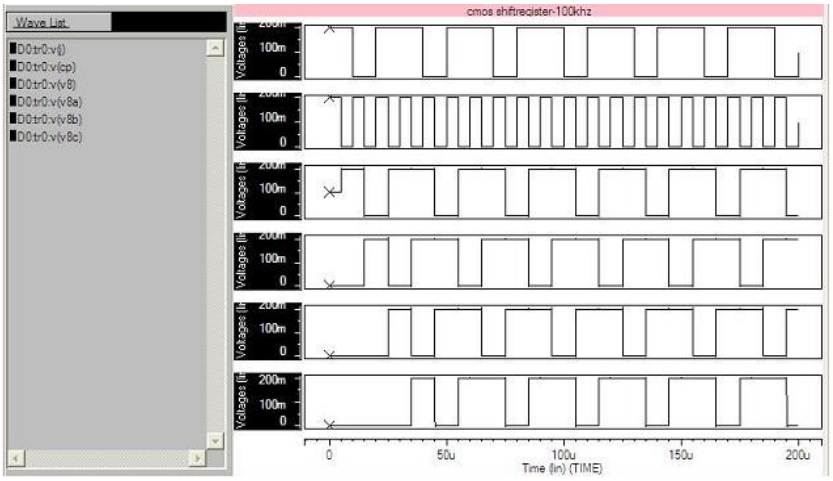


Fig 5(c) : Input and Output waveforms of CMOS Serial in Serial out Shift Register -100KHZ

3.3 Performance analysis of VTMOS Serial in Serial out Shift Register

The propagation delay, the rise and fall time delay, average power dissipation and power delay product are measured for VTMOS Serial in Serial out Shift Register (for |VAN|=|VAP| varying from 0 to 0.2v) at a particular input signal frequency of 100 kHz for performance evaluation .The performance results of VTMOS Serial in Serial Out Shift Register are also compared with the conventional CMOS Serial In Serial Out Shift Register in this section. Fig 6(a), 6(b) and 6(c) shows the variation of propagation delay, average power dissipation and power delay product for VTMOS Serial in Serial out Shift Registers with |VAN|=|VAP| varying from 0 to 0.2v at 100 kHz frequency. The following section deals the result discussion of the VTMOS Serial in Serial out Shift Registers.

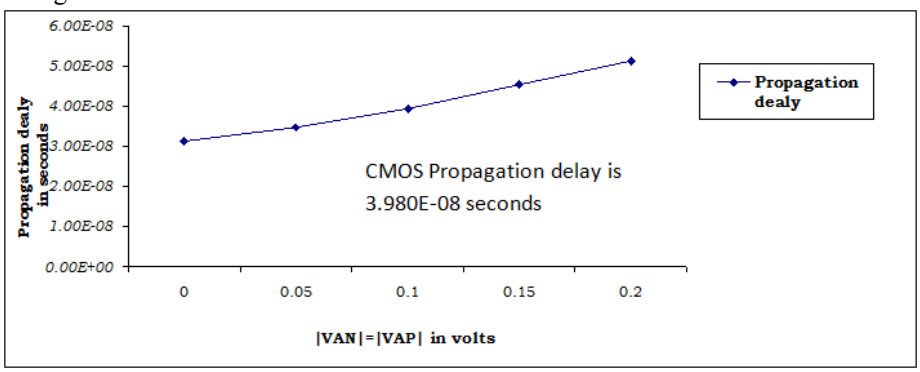


Fig 6(a) : Variation of propagation delay for VTMOS Serial in Serial out Shift Registers (|VAN |=|VAP| varying from 0 to 0.2v)

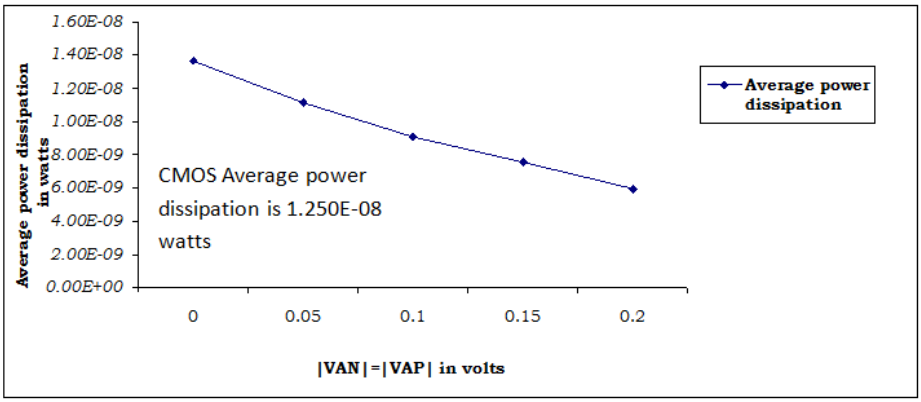


Fig 6(b) : Variation of Power dissipation for VTMOS Serial in Serial out Shift Registers (|VAN |=|VAP| varying from 0 to 0.2v)

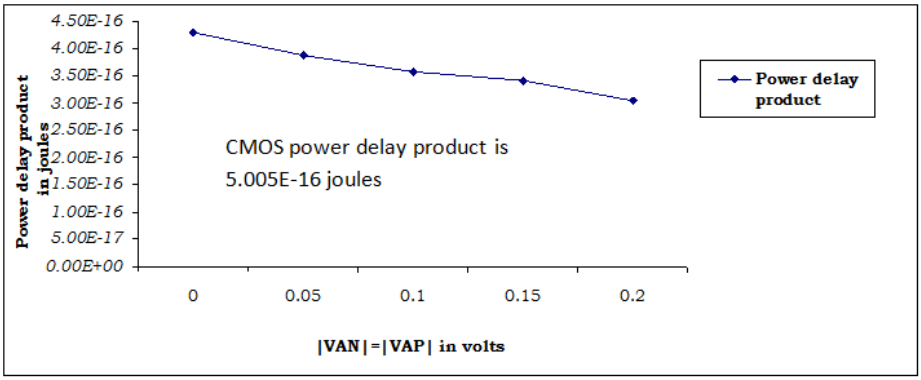


Fig 6(c) : Variation of Power delay product for VTMOS Serial in Serial out Shift Registers (|VAN |=|VAP| varying from 0 to 0.2v)

3.4 Discussion on Results of VTMOS Serial in Serial out Shift Register

Fig 6(a) gives the variation of propagation delay with |VAN|=|VAP| at 100 kHz frequency for sub threshold VTMOS Serial in Serial out Shift Register circuit. From Fig 6(a) it may be observed that propagation delay increases with increase in |VAN|=|VAP| and the propagation delay of sub threshold VTMOS Serial in Serial out Shift Register at |VAN|=|VAP|=0.1V, almost approaches the propagation delay of sub threshold CMOS Serial in Serial out Shift Register . The increase in propagation delay from |VAN|=|VAP| varying from 0 to 0.2v is 3.140E-08 seconds to 5.129E-08 seconds .Whereas for CMOS Serial in Serial out Shift Register, the propagation delay is 3.980E-08 seconds. Fig 6(b) gives the variation of average power dissipation with |VAN|=|VAP| at 100 kHz frequency, for sub threshold VTMOS Serial in Serial out Shift Register. From Fig 6(b), the average power dissipation may be seen to decrease from 1.363E-08 watts to 5.938E-09 watts, with increase in |VAN|=|VAP| varying from 0 to 0.2v.The power dissipation in CMOS Serial in Serial out Shift Register, however is almost the same as VTMOS Serial in Serial out Shift Register with (|VAN|=|VAP|=0v).From this it is very clear that the highest power dissipation and highest delays in VTMOS Serial in Serial out Shift Register is similar to the one in power dissipation and delays in CMOS Serial in Serial out Shift Register and one can achieve lower delays or lower power dissipations compared to CMOS in VTMOS circuits. Overall 54% reduction in power can be achieved at frequency= 100 KHz in VTMOS Serial in Serial out Shift Register for |VAN|=|VAP|=0.2v compared to CMOS Serial in Serial out Shift Register. This reduction in average power dissipation is because of low off state leakage current and low standby power in VTMOS circuits with |VAN|=|VAP|=0.2v.

In order to achieve the optimum delay and optimum power dissipation in VTMOS Serial in Serial out Shift Register, one may have power delay product which is described in Fig 6(c).In this it may be seen that the power delay product in VTMOS Serial in Serial out Shift Register decreases with maximum |VAN|=|VAP|=0.2V.This clearly shows that one can achieve lower power dissipation with reasonable delay in VTMOS circuits.

3.5 Effect of frequency on performance characteristics of Serial in Serial out Shift Register

In order to get the effect of frequency on performance characteristics, the frequency of sub threshold VTMOS Serial in Serial out Shift Register's is varied from 100 KHZ to 8 MHZ.. However the power

dissipation increases with frequency and the variation of power dissipation with frequency for sub threshold CMOS Serial in Serial out Shift Register's and sub threshold VTMOS Serial in Serial out Shift Registers (|VAN|=|VAP| varying from (0 to 0.2v) is shown in Fig 7. Propagation delay and logic levels remain almost constant with frequency. It can be observed that as frequency is increased, the power dissipation of VTMOS Serial in Serial out Shift Register's increases much more rapidly than in the case of CMOS Serial in Serial out Shift Registers. This trend can be explained based on various sources of power dissipation in MOS based circuits and dynamic power dissipation component predominates at higher frequencies as given for inverter circuits.

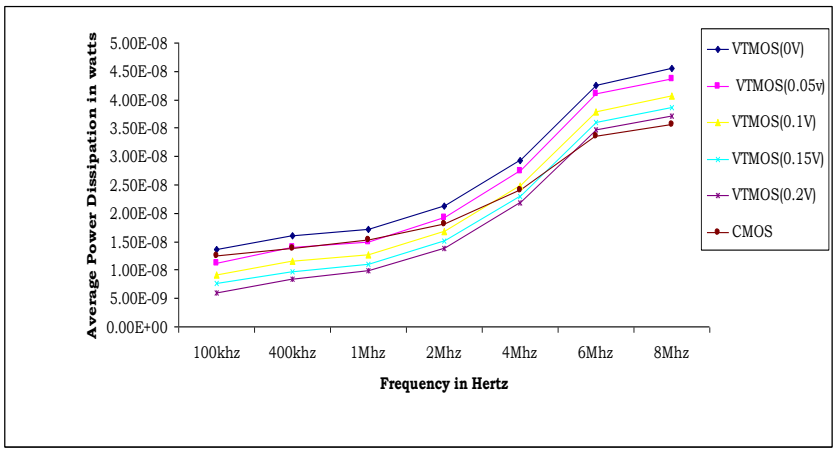


Fig 7: Variation of Average power dissipation with frequency for 4 bit Serial in Serial out Shift Register

IV. Conclusions

This paper reports a modified DTMOS approach which is called VTMOS approach. In these circuits the substrate is operated with a fixed bias (V_{AN} /V_{AP}) which results in further reduction in the operating currents compared to DTMOS circuits. The Proposed scheme shows improved power efficiency of 50% compared to CMOS and DTMOS circuits , up to a frequency of 8 M h z (for the specific devices used in this Investigation).The complex digital circuits like Serial in Serial out Shift Register were realized using the basic VTMOS family. The study has shown that VTMOS circuits are superior to the conventional CMOS and DTMOS techniques in terms of power efficiency. It is also proved that VTMOS circuits provide good cascadability and work satisfactorily up to 8 MHz frequency

References

[1]. H.Soeleman , K.Roy, and B.C.Paul. : "Robust Sub threshold Logic for Ultra Low Power Operation" ,IEEE trans VLSI system, Feb 2001,Vol. 9, PP. 90-99.

[2]. Jabulani: Nyathi and Brent Bero: "Logic Circuits Operating in Sub Threshold Voltages" , ISLPED 06, October 4-6, 2006, Tegernsee, Germany.

[3]. C.Hyung, - 11 Kim, H.Soeleman, and K.Roy: "Ultra-Low Power DLMS Adaptive Filter for Hearing Aid Applications" ,IEEE transactions on very large scale integration (VLS1) system, vol. 11, No.6, December, 2003. PP 1058-1067.

[4]. H. Soeleman and K. Roy,"Ultra-low power digital subthreshold logiccircuits", in Int. Symp. Low Power Electron. Design, 1999, pp. 94–96.

[5]. Fariborz Assaderaghi, Stephen Parke, Dennis Simitsky, Jeffrey Bokor, Ping K. KO. Chenming Hu:"A Dynamic Threshold Voltage MOSFET (DTMOS) for Very Low Voltage Opertaion" ,IEEE Electron device letters, vol. 13, No.12, December 1994.

[6]. Tae-Hyoung Kim, Hanyang Eom, John. Keane and Chris Kim: "Utilizing Reverse Short Channel Effect for Optimal Sub Threshold Circuit Design" ,ISLPED 06, October 4-6, 2006. Tegern see, Germany.

[7]. H. Soeleman, K. Roy, B. Paul :"Robust ultra-low power sub-threshold DTMOS logic", in Int. Symp. Low Power Electron. Design, 2000 ,pp.25 – 30.

[8]. J. Gil, M. Je, J. Lee and H. Shin:"A High Speed and Low Power SOI Inverter using Active Body-Bias", in Int. Symp. Low Power Electron.Design , 1998 , pp.59-63.

[9]. F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. K. Ko, and C. Hu: "A dynamic threshold voltage MOSFET (DTMOS) for ultra-low voltage operation", in IEDM Tech. Dig., 1994, pp. 809–812.

[10]. I.Chung, Y.Park, and H. Min: "A new SOI inverter for low power applications", in Proc. 1996 IEEE Int. SOI Conf., 1996, pp. 20–21.

[11]. A.Drake, K. Nowka, R. Brown: " Evaluation of Dynamic-Threshold Logic for Low-Power VLSI Design in 0.13um PD-SOI" ,VLSI-SOC 2003,pp. 263-266.

[12]. M.R. Casu, G**.** Masera, G. Piccinini, M. Ruo Roch, M. Zamboni:"Comparative Analysis of PD-SOI Active Body-Biasing Circuits," Proc. IEEE International SOI Conference, pp. 94-95, Oct. 2000.

[13]. S.Soleimani,A.Sammak,B.Forouzandeh "A Novel Ultra-Low-Energy Bulk Dynamic Threshold Inverter Scheme",Proceedings of the International Multi Conference Of Engineers and Computer Scientists 2009 Vol 1 IMECS 2009,March 18-20,2009,Hong Kong