

## **FPGA Based Reconfigurable Memory Interface Design for EEG Data Acquisition**

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**Abstract:** *There is a great need and demand for high throughput biomedical data display system in every clinical study and diagnostic labs in Hospitals. To cater to this demand, we have designed FPGA-based memory architecture suitable for use in displaying low frequency EEG data. Memory architecture is designed to acquire up to 32 channel EEG data. An Instrumentation amplifier suited for EEG signals has also been designed and tested for a single channel bipolar configuration. The implemented memory architecture has fast retrieval time and a large data storage capacity. The efficient cache memory implementation on FPGA achieves low complexity and low power consumption in terms of FPGA resource usage. The system is a modular design that relies on a USB 2.0 connections for data transfer. Each element on the array has a dedicated 8 bit, ADC to digitize the data. 4 ADCs were placed on a single board interfacing with a dedicated Spartan 3 FPGA to process and buffer the data before transfer through the USB link to the computer. The Designed System using Spartan 3 FPGA utilises 44% of 4 input LUT's, 100% of Slice utilization, and 80% of Boundary IOBs. The system clock frequency reported by the Place and Route tool is 77.6 MHz. The portability and reconfigurability properties of the designed hardware offers much promise for deployment in a Neuro feedback application.*

**Keywords:** *amplifier, shield, electroencephalography, FPGA memory architecture*

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### **I. Introduction**

In the late 1800s, Richard Carton first reported the presence of bio potentials on the surface of the human skull. The electroencephalography (EEG), pioneered by Hans Berger, measures the electric potentials on the scalp and provides continuous measurement of cortical activity. EEG has played an important role due to its non-invasiveness and the capability of long term measurement in the field of epilepsy, sleep disorders, and in various neurological conditions. Also work has been done to study the effect of meditation through EEG. The design of a Low-Cost Stand-Alone Multichannel Data Acquisition, Monitoring, and Archival System was proposed by Mohammed Abdullah et al. for medical applications [1]. Arshak E. et al. designed a Low-power wireless smart data acquisition system [2]. J. M. Cardoso et al. have suggested a high performance reconfigurable hardware processing system. Croft RJ and Barry RJ in their work have shown how to remove the artefacts in EEG signals [3]. Custódio F. M. et al. presented a design of Innovative Modular High-Speed Data-Acquisition Architecture [4]. The drawback found in these work is EEG acquisition systems used as well as the proposed methods are expensive. The EEG signal amplitude is in the range of 1-100 micro volts. The design of an amplifier is a challenging task. Also if the number of channels to be studied is more, then storing of the EEG data requires large memory. An efficient Memory management needs to be addressed. These drawbacks found from the survey of the earlier work done are addressed in our work.

In the present work we have designed a low cost EEG acquisition system and reconfigurable memory architecture to store data up to 32 channels. In this work, we describe a custom-designed EEG amplifier. The amplifier has the following features:

1) Differential amplifier with driven shield inputs, which makes it workable even in electrically unshielded environments, 2) high input impedance to allow recordings of small signals through high signal source impedance, and 3) gain controller and a DC offset circuit to make the signals compatible for A/D converter circuit. We compared its performance with a “biopac” amplifier and “pomtrons” amplifier. Even without any electrostatic shield, it recorded clear electromyo-graphic activity with little interference from other electric appliances. The designed amplifier is made compact, portable and Battery operated. This amplifier can be used to build a computer-controlled stimulation and measurement system for electro-encephalographic recordings. We successfully recorded various sensory evoked potentials with clarity that otherwise would have required costly instruments. This amplifier is a low-cost yet reliable instrument for electro-physiological recording both in education and research.

In biomedical laboratories, every student experiences recording of EEG activity. Yet most commercially available equipment is not amenable to meeting this ideal. First, the high cost of commercial

amplifiers often precludes obtaining sufficient number of units for students' training. This is not a desirable situation because, in group teaching, only a limited number of students have the chance to record neural and/or muscular activity directly. Second, commercial amplifiers are designed for use in electrically shielded environment, which necessitates the use of Faraday cages during recording. For recording from small animals such as rats, shielding is not a major problem. On the other hand, for human subjects, this requires large Faraday cages or shielded room, thereby restricting the place where recording is done. Some manufacturers offer "active electrodes" with a built-in unity gain amplifier to reduce the noise. Yet these electrodes come as surface electrodes, which restricts their application, e.g., recording of EEG, surface EMG. Moreover, most of the commercially available active electrodes are designed to work with specifically designed amplifiers which are again expensive. Therefore, with affordability and noise attenuation as major requirements, we developed a relatively simple and inexpensive amplifier for researchers. It features differential amplification which cancels common mode noise, and driven shield technology that protects the inputs against electrostatic interference. We found that these features ensured stable recording in noisy environment, and thus made this amplifier a useful instrument for research students.

This paper is organized as follows: In section II, EEG Amplifier Design and Data Acquisition concepts are presented. Memory Architecture Design Using FPGA is presented in section III. Simulation Results are presented in section IV. Conclusions drawn are made in the last section.

## II. EEG Amplifier Design and Data Acquisition

In this work, a Data Acquisition System has been designed to acquire up to 32 channels of EEG signals. Fig. 1 illustrates the circuit diagram of EEG acquisition system. It comprises 1) Isolation Amplifier, 2) Instrumentation Amplifier, 3) Second Order Low Pass Filter, 4) Inverting Amplifier and 5) Null adjust circuit. Details of these are presented in the following.

### 1) Isolation Amplifier

It is the most critical and important stage since overall performance of the amplifier depends on this amplifier. For the first stage of amplification as well as for isolation, we have used two LM324 integrated circuits. It takes inputs from the reference and the active electrode (monopolar) or from two active electrodes (bipolar). This circuit is used mainly for isolation of the subject from the power supply side and have a RC circuit at the input end which allows signals up to 30 Hz. It amplifies two inputs difference, thus subtracting out the noise common to both the inputs.

### 2) Instrumentation amplifier

The Instrumentation amplifier is designed using three LM324 ICs. The differential output of the Isolation amplifier is fed to the first two ICs of the amplifier. Variable resistor R28 value ranging from 220 ohm to 2.2 K will provide an overall gain ranging between 102 dB to 82 dB. The Third IC is used as a differential amplifier and has a gain of about 100, which will amplify the differential input.

### 3) Second Order Low Pass Filter

Second order Butterworth filter is used with a gain of 1.5 and with a cut off frequency of 300 Hz, thus limiting the frequency range which is enough for diagnostic purposes.

### 4) Inverting amplifier

This Amplifier is used at the output stage to provide a gain of 1 to 1.2. DC offset adjustment circuit is used to provide a zero value when no input signal is applied. The R27 potentiometer variable point of the DC offset circuit is connected to the inverting input of the output stage amplifier in order to enable the Null offset adjustment.



Figure 1: EEG Acquisition System

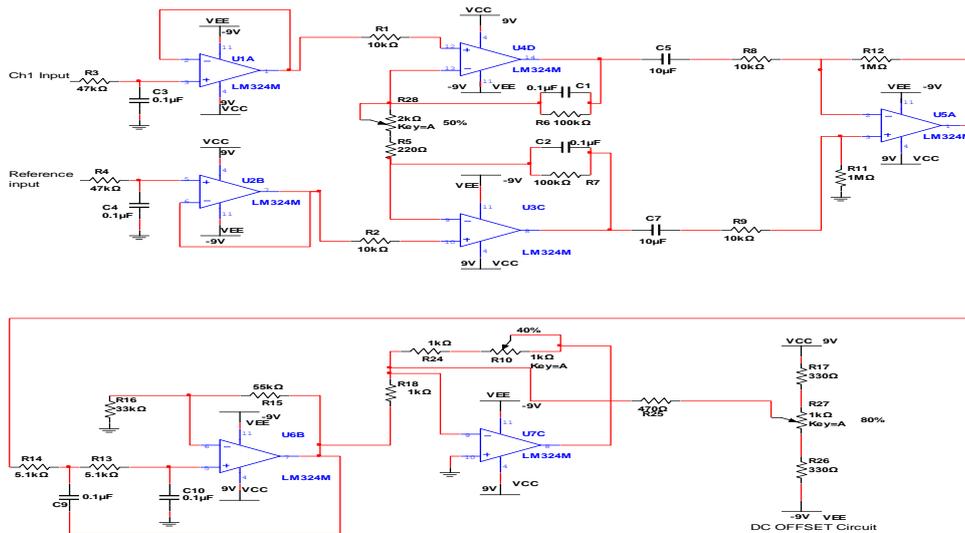


Figure 2: Circuit Diagram for Amplifying EEG Signals Using Instrumentation Amplifier

The complete EEG acquisition system is shown in Fig 2. The Amplifier circuit can be operated with Battery supplies as well as Fixed DC supplies. The Circuit is tested with Multisim software (Version11). If the circuit is operated with fixed DC supplies, EEG Output is found to be contaminated with 50 Hz noise. In order to eliminate this line interference, a 50 Hz Notch Filter is used. Notch filter circuit is shown in Figure 3 and its frequency response simulation result is presented in Figure 4. The EEG outputs from the subject are shown in Fig. 5 and Fig 6. In this case, outputs are free from the line interference. Output from the Amplifier for Eyes closed and open conditions is shown in Fig. 5 and Fig. 6.

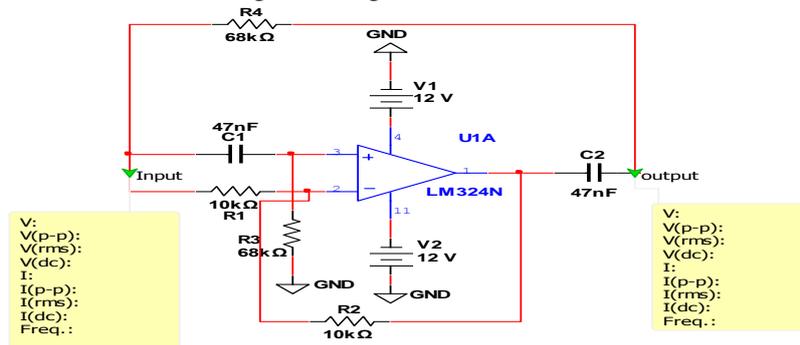


Figure 3: Circuit Diagram of Notch Filter

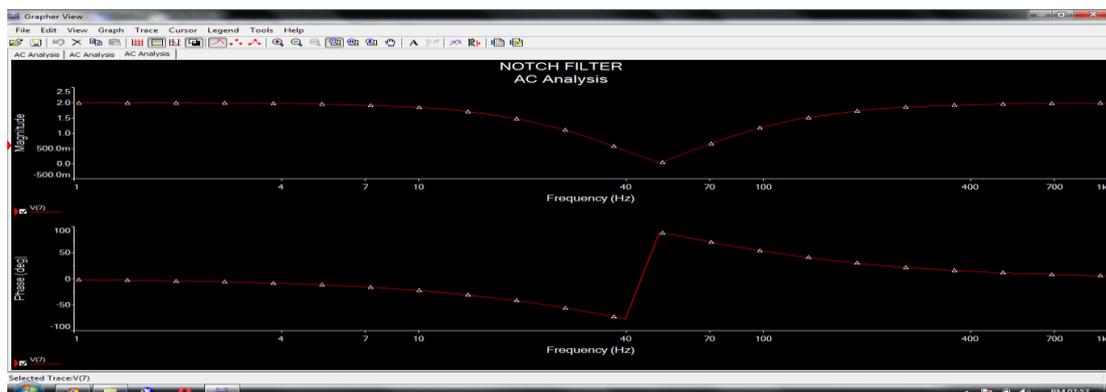


Figure 4: Simulation output of Notch Filter

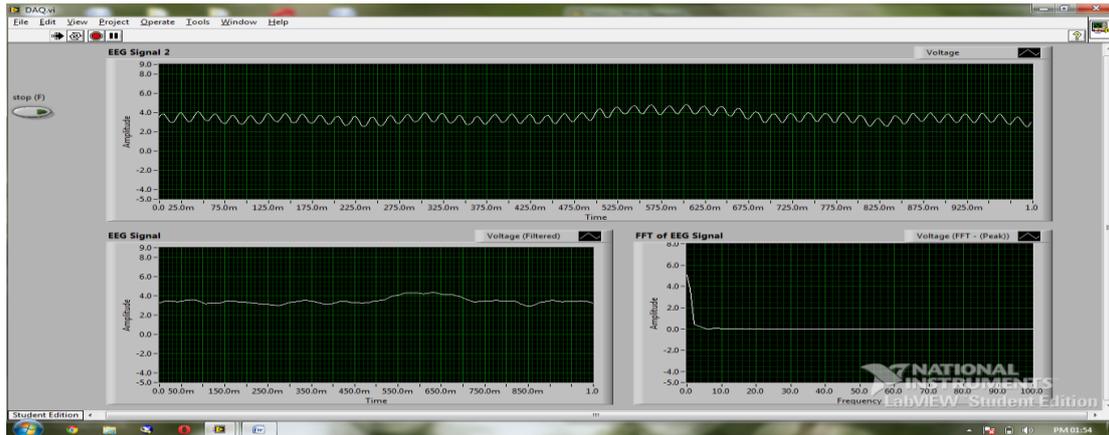


Figure 5: EEG Amplifier Output with Eyes Closed



Figure 6: EEG Amplifier Output with Eyes Open

### III. Memory Architecture Design Using FPGA

The analog output from the EEG amplifier is digitized using AD8089 8 bit ADC. Then the signals are fed to FPGA Board for storage. Through RS232, data is transferred to PC for Display. The purpose of the present work is to design a neuro feedback system in order to acquire and analyze EEG signals. The complete system level architecture of designed neuro feedback system is shown in Fig 7. The system comprises of three main modules, viz, the signal acquisition and conditioning module, analog to digital converter module and the signal analysis and display module. The EEG sensors capture the differential signals from the subject and feed to the signal conditioning module and then to the ADC module for digitization. The ADC circuit converts the analog signals into corresponding 8 bit digital signals with a clock frequency of 640 KHz. The ADC Board comprises four ADC's where in each ADC is configured to acquire 8 channels of EEG data. The FPGA controller can read digitized signals from all the four ADCs simultaneously and store them into Static RAM for further processing. The stored data are further retrieved and communicated to the LabVIEW application through serial communication for analysis and display of the signals. The current design can capture and store 32 channel signals for a maximum period of two minutes at the rate of 256 samples per second. However, for neuro feedback system, 4 channels only are adequate and for which the system is capable of storing the EEG data up to 16 minutes. The system can be easily scaled up to a higher number of channels by changes in the coding and hardware [5].

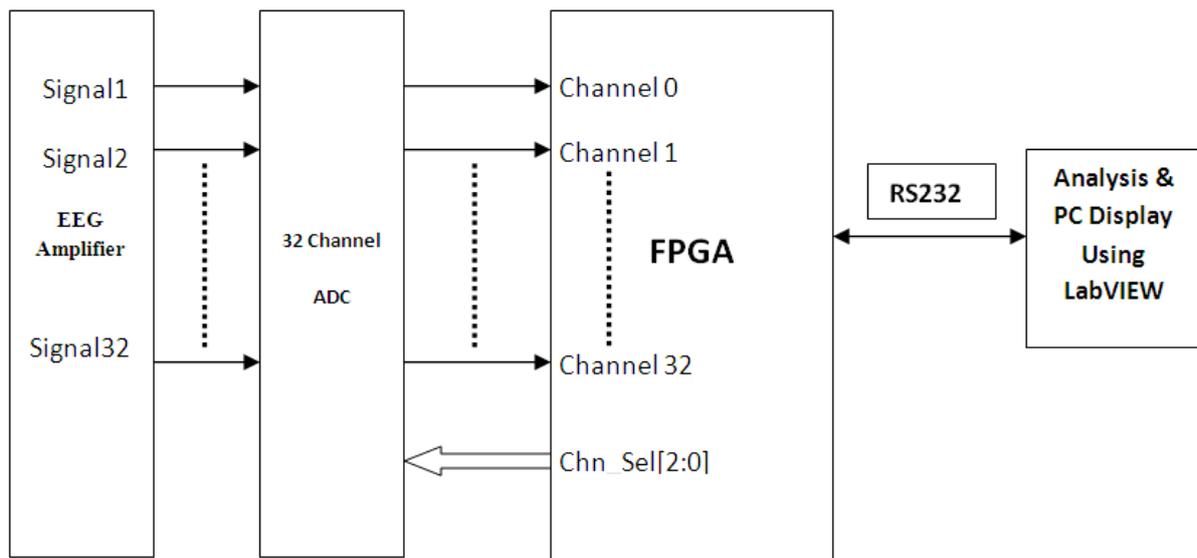


Figure 7: Real time EEG Data Acquisition and Display System

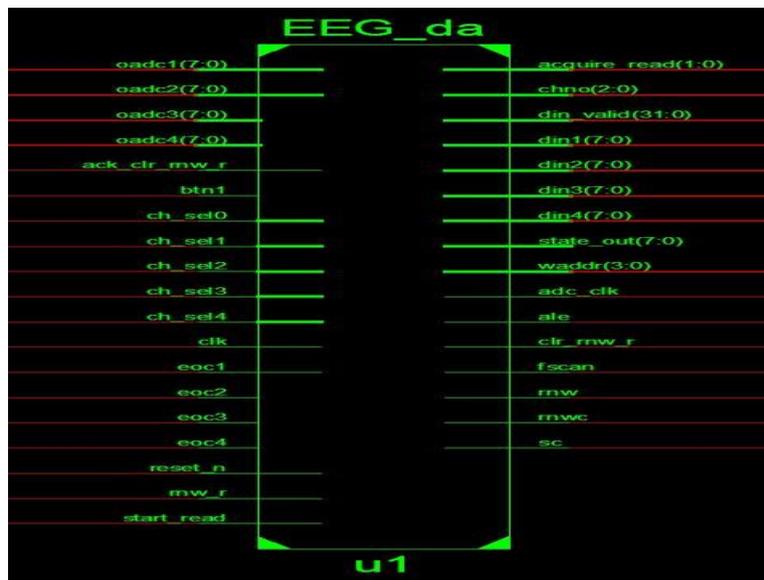


Figure 8: RTL View of EEG Data Acquisition System

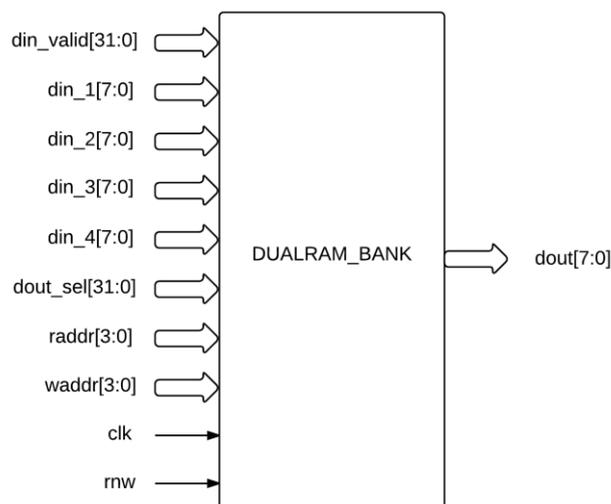
The RTL view of the top level for the EEG data acquisition system obtained using Xilinx ISE tool 13.4 is shown in Figure 8. It instantiates EEG\_da block which reads signals from four ADCs, Dual RAM (dualram\_bank), SRAM controller (SRAM\_controller) and UART sub modules.

The “EEG\_da” sub module block diagrams with all the input and output signals are explained in the following sections. This module controls the digitized EEG signal acquisition from the ADC board. The design is capable of acquiring signals from four channels concurrently. Signal acquisition is done at the rate of 256 samples per second. Each ADC can cater up to eight channels. So, four ADCs are used to digitize analog signals from 32 EEG channels. The ‘clk’ is the system clock and ‘reset\_n’ is the global reset signal in order to reset the system during power on conditions. ADC channel selection is done using signal chn0[2:0] and adc1[7:0]-adc4[7:0] are the digital data outputs from the ADCs received by the “EEG\_da” module. After conversion, the signals ‘eoc1, eoc2, eoc3 and eoc4’ representing End of Conversion are sent from all four ADCs. The data is stored in the output register ‘din’ from which it is transferred to the intermediate Dual RAM memory bank of size 16 bytes each. The user can set the total number of channels to be read (anything between 1 and 32) using the “chn\_sel[5:0]” signal. Based on the value set, the module reads the corresponding channels. ‘ale’ is address latch enable and ‘sc’ is Start of Conversion for the ADC to begin the conversion.

The Dual RAM bank (dualram\_bank) module, shown in Figure 9, comprises 32 numbers of dual RAMs (dualram) module, each of size 16 bytes, to store 16 bytes of digitized signals in one cycle. Each dualram

is subdivided into two RAMs namely RAM1 and RAM2. Data acquisition from each channel is done in packs of 16 bytes. While the next bunch of 16 bytes are being written in the next set of RAMs in the dual RAM modules, the previous 16 bytes data already stored are transferred into SRAM memory of size 1 MB through the output signal 'dout[7:0]'. The two RAMs are configured in write only mode and read only mode alternatively by the input signal 'rnw' from "EEG\_da" module, where a 'high' configures RAM1 in write mode and RAM2 in read mode and vice versa. The design is thus pipelined to provide a higher processing speed. Once one set of data from 32 ADC channels is written into the "dualram", the "dualram\_read" transfers the dualram data into SRAM memory for final storage so that the dualram can be used to load fresh data from ADC [6-7].

The data storage unit is a 1 MB SRAM which can be dynamically divided equally based on the total number of channels read by the user. The minimum memory available for each channel is approximately equal to 16 KB of memory in case the user uses all 32 channels. The SRAM memory stores the digital data obtained from ADC through the multichannel input signals. Data storage plays an increasingly essential role in data monitoring and analysis. The proposed design of data storage block provides the flexibility of continuous data acquisition and random access to the desired channel data. The "dualram\_read" module, shown in Figure 10, fetches the data from the "dualram" memory and stores it in the SRAM memory in the respective address. The "acquire\_read" signal controls the read and writes functions of the memory. In "acquire\_read = 1" mode, the module reads the data through signal "din\_SRAM[7:0]" and stores it in the appropriate location using the addr signal "waddr". The SRAM memory is split into equal portions based on the user input "ch\_sel". Once all the data has been stored in the SRAM memory, the user can access data of any channel and analyse. For EEG data analysis, an application has been developed in LabVIEW. The application utilises the data stored in the SRAM memory through a serial communication module explained in the next section. The Architecture of the Serial Communication Controller for serial communication between the FPGA/ASIC and the GUI is shown in Fig. 12.



**Figure 9:** Dual Ram Bank Inputs and Output signals

It consists of two modules, namely, "Data\_controller" for processing the incoming data, and "UART" for transmitting and receiving data [8-10].

The Universal Asynchronous Receiver/Transmitter module is the key unit of the communication controller module, which communicates with the PC application. Once the "acquire\_read" signal value is equal to "2", the "SRAM\_controller" module reads the data from the SRAM memory for the selected channel and feeds it to UART for transmission. The UART module takes a byte of data at a time and transmits the individual bits in a sequential manner conforming to USB protocol. At the destination, i.e., LabVIEW application, UART re-assembles the bits into complete byte and makes the data available to the Transreceiver module for further processing. The UART module has been configured for 115,200 bits per second baud rate, 8 data bits, one stop bit and no parity. On successful transmission of a data byte, the "UART" signals the "Data\_controller" module that the transmitter is ready, which in turn feeds the next available data and enables the "UART" to transmit the next data. The "Data\_controller" is designed to bring about the synchronization between the UART and the "SRAM\_controller". The main task of the module is to read the data output by "SRAM\_controller" and feed it to "UART" for transmission by enabling the data transmitter part of the "UART" state machine. This kind of handshaking or synchronization is very essential in order to avoid any kind of data loss [11-12].

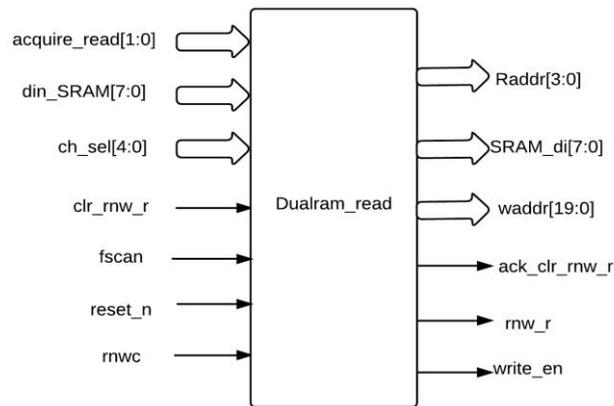


Figure 10: Dual Ram Inputs and Output signals

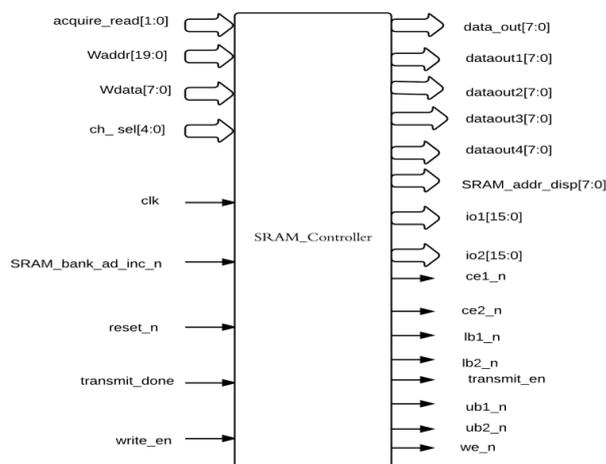


Figure 11: SRAM Inputs and Output signals

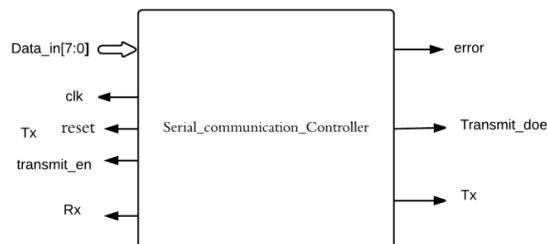


Figure 12: Serial communication module

#### IV. Simulation Results

The architecture of the designed EEG system was presented in the previous section. The present section presents the Simulation results. Fig. 13 shows the simulation waveforms for communication between FPGA and ADC and data storing flow from ADC to Dual RAM memory. For test bench, 4 channels have been selected, so data storage for four dual RAMs have been shown. Fig. 14 shows the data storage sequence from dual RAM to SRAM. Based on the total number of channels required, SRAM memory is divided into equal parts; SRAM manipulation is shown in the waveform.

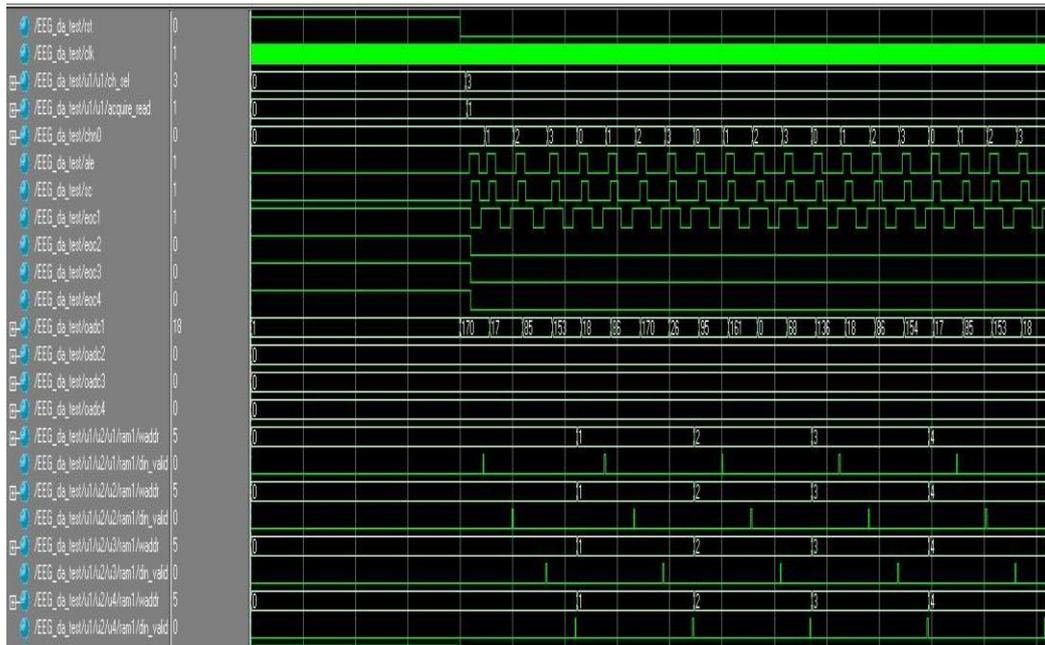


Figure 13: Simulation Result for Data Transfer from ADC to FPGA Board

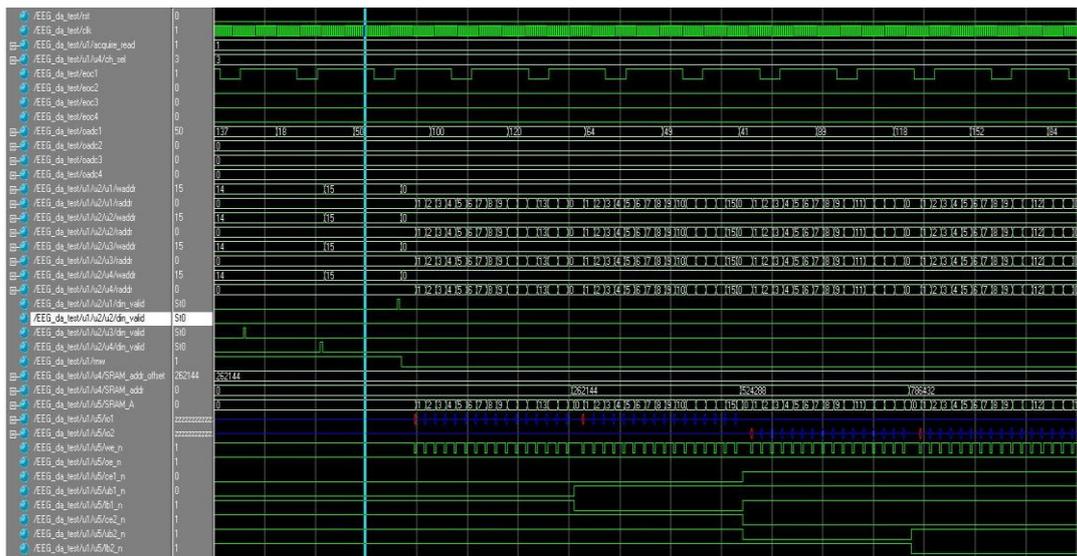


Figure 14 Simulation Result of Data Transfer from Dual RAM to SRAM

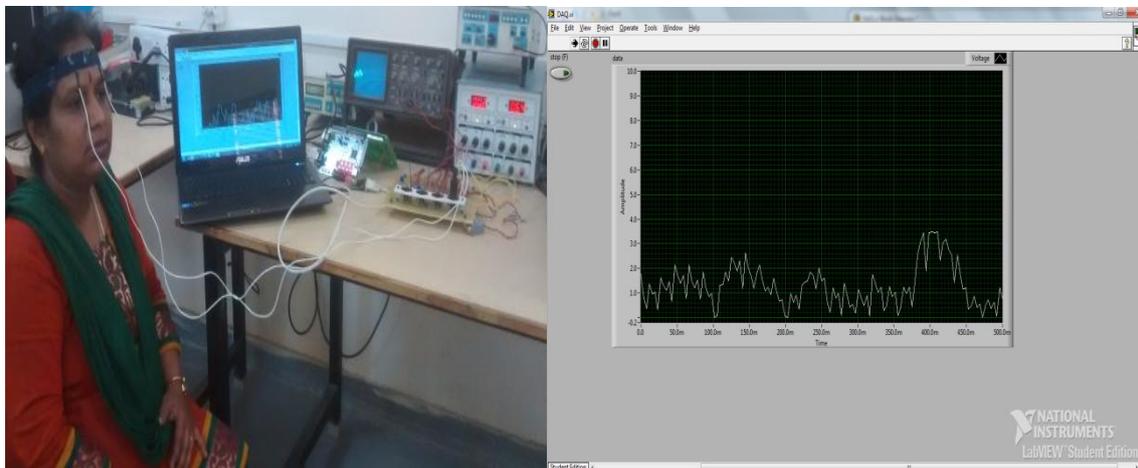


Figure 15: Signal Acquisition System Setup and Single Channel EEG Output with Eyes Open

The EEG data acquisition system Interface with FPGA board is shown in Fig. 15. The designed system performance is tested for of a subject with eyes open and eyes closed conditions [13-17].

## V. Conclusions

EEG signal is a weak signal which can be easily contaminated by noise. Accurate measurement of EEG signal can be a great challenge when strong interference noise is greater than the actual EEG signal. In this work, a complete system has been designed and fabricated for acquiring up to 32 channels of EEG data. By incorporating Noise filter, 50 Hz noise was eliminated. By using good disposable Electrodes, we could acquire noise free EEG signals. EEG data have been acquired for different subjects and verified using “biopac” EEG data acquisition system.

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