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RISC Implementation Of Digital IIR Filter in DSP

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Abstract: *This paper is base on the implementation of Reduce Instruction set computer with the application of Discrete Cosine transform (DCT) , Inverse DCT, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Digital filter are performed by DSP system. Digital filter is one of the important contents of digital signal process. The performance of the processor design is improved by using the pipeline approach. It allows the processor to work on different steps of the instruction at the same time, thus more instruction can be executed in a shorter period of time. The analysis of this processor will provide various features including arithmetic operations. The speed of operation is mainly affected by the computational complexity due to multipliers and adder modules of the digital systems. Our work will targets the computer architecture courses and presents an FPGA (Field Programmable Gate Array) implementation of a MIPS (Microprocessor without Interlocked Pipeline Stages) via VHDL (Very high speed integrated circuit Hardware Description Language) design. The latency and computational time is utmost important in microprocessor. Thus we design the multiplier and adder module with improve latency and computational time.*

Keywords: *IIR FILTER, FPGA, DSP Processor, VHDL*

I. Introduction

Conventionally, the digital filter, Discrete fourier and Z transform applications are implemented either using general purpose DSP processors (low speed, less expensive, flexible) or using Application Specific Integrated Circuits (ASIC) which offer high speed but are expensive and less flexible. An alternate approach is to use reduce instruction set computer (RISC) as they provide solutions that maintain both the advantages of the approach based on DSP processors and the approach based on microprocessor. The RISC decodes the instruction format and execute one instruction per cycle. By pipeline approach it fetches, decoded, and execute two or three instructions at the time. Instructions are of fixed number of bytes and take fixed amount of time for execution with lesser amount of circuitry.

II. Related Work

Sheikh Md. Rabiul Islam, Robin Sarker, Shumit Saha, A. F. M. Nokib Uddin publish their work on title " Design of a programmable digital IIR filter based on FPGA" at the IEEE International Conference on Infonatics, Electronics & Vision ICIEV year 2012. They design the arithmetic and logical unit, program counter, internal register, internal RAM memories etc using verilog hardware description language for the design of IIR filter base application in DSP processor. Their approach of second order IIR filter implementation gives a better performance than the common filter structures in terms of speed of operation, cost, and power consumption [1].

Amit Kumar Singh Tomar, Rita Jain present their work on title "20-Bit RISC & DSP System Design in an FPGA" IEEE international conference in year 2013. in their work they design the reduce instruction set computer architecture which executes the digital signal processor operations. It contain the DFT IDFT and Z transform base IIR filter applications. The simulation and result of this processor give different features including arithmetic operations and Fourier transform. This design is easily improved by increasing the memory of the processor and can be implemented with higher bit value. The purpose of this work is to define a methodology for designing fixed-point IIR digital filters using modeling tools using parallel structure implementation. Designing more than two transfer functions sections introduces the problem on how to go about summing the sections together. Because of the fixed-point representation, the non-linear aspect of summing could potentially be a setback [2].

Chaohua Dai, Weirong Chen, and Yunfang Zhu publish their work on title "Seeker Optimization Algorithm for Digital IIR Filter Design" in IEEE Transactions On Industrial Electronics, Vol. 57, No. 5, May 2010 pp no. 1710. In this work the nonlinear error of infinite-impulse response (IIR) filters is optimize by evolutionary method based a seeker-optimization-algorithm (SOA). In their work, an SOA-based digital filter

design method has been proposed, and the benefits of SOA for designing digital IIR filters have been studied [3].

III. Principles Of IIR Digital Filter

Digital filter is actually a linear time-invariant discrete system using finite precision algorithms, and its function is actually achieved by a large number of addition and multiplication operations [4]. IIR digital filters are recursive systems that involve fewer design parameters, less memory requirements, and lower computational complexity than finite impulse response (FIR) digital filters. It is characterized by the general linear constant-coefficient difference equation as follows:

$$y(n) = -\sum_{k=1}^{N} a_k y(n-k) + \sum_{k=0}^{M} b_k x(n-k)$$

Transforming this difference equation into the z-domain by means of the z-transform, such a class of linear time-invariant discrete-time systems is also characterized by the transfer function as follows:

$$H(z) = \frac{\sum_{k=0}^{M} b_k z^{-k}}{1 + \sum_{k=1}^{N} a_k z^{-k}}$$

Different structures of IIR filters are described by the difference equation in above. These structures are referred to as direct-form realizations. It should be noted that although these structures are different from one another by design, they are all functionally equivalent. Three prominent direct-form realizations are the Direct-Form I, the Direct-Form II, and the Transposed Direct-Form II structures. In terms of hardware implementation, the Direct-Form I structure requires M+N+1 multiplications, M+N additions, and M+N+1 memory location

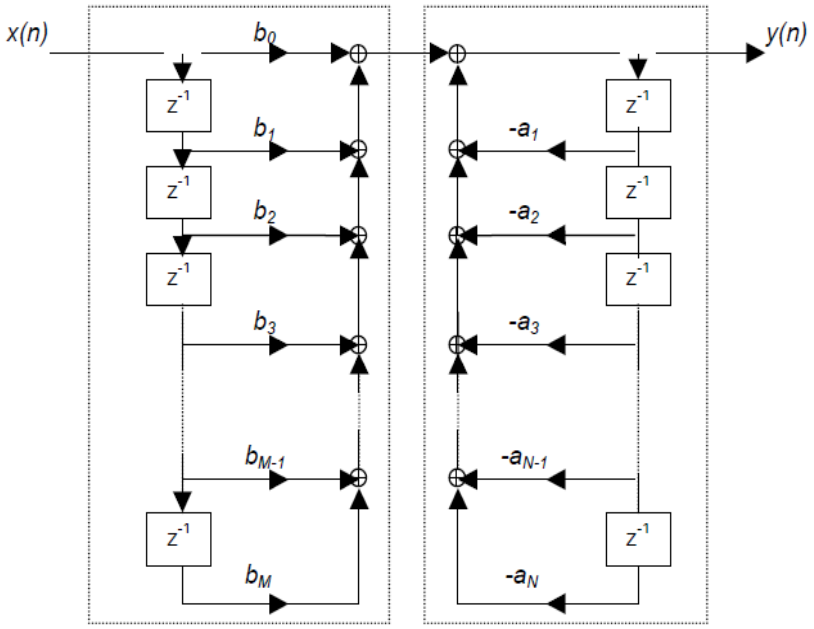

Fig Direct form realization

The Direct-Form II structures require M+N+1 multiplications, M+N additions, and the maximum of {M,N} memory locations. Because the Direct-Form II structure requires less memory locations than the Direct-Form I structure, it is referred to as being canonic. Figure above shows an IIR digital filter in Direct-Form II format [4].

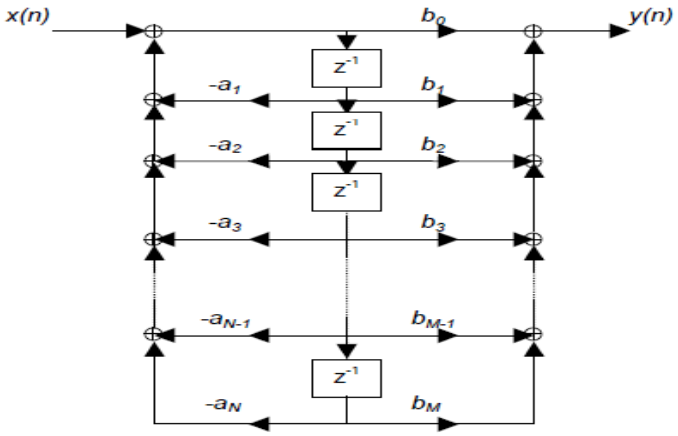

Fig Direct form II realization

IV. Modules Of Design

The module design of RISC includes the Register, Instruction Memory, Data Memory, instruction fetch unit, instruction decode unit, the control unit, and execution unit. Instruction unit fetches the instruction code as per the address pointed by program counter register. It includes the incrementer logic to increment the content of program counter after every instruction byte execution. The instruction decoder decodes the instruction provided from the instruction fetch unit. The control unit generates the control signals for the operation of the arithmetic and logical operations. The memory read and writes signals are asserted for the control unit is use to access the data or write the data in memory.

V. Multiplier Module

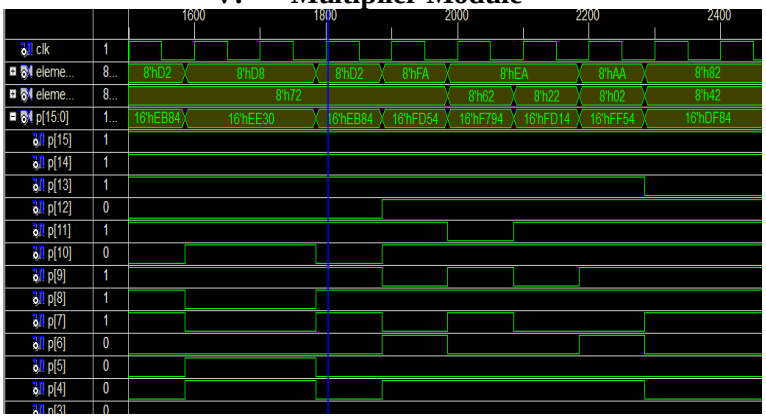

Fig Timing simulation of multiplier unit.

The multiplier module is design for coefficients multiplication in the signal flow graph of direct form structures in IIR filter design.

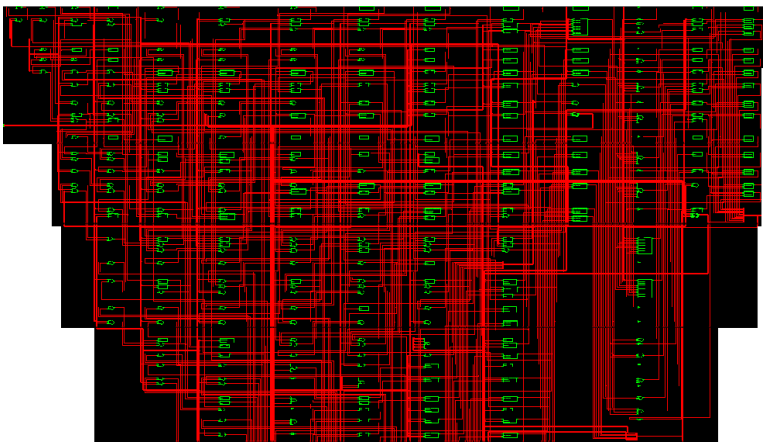

Fig RTL view of multiplier unit.

Cell Usage:

BELS	: 818
AND2	: 284
AND3	: 13
AND4	: 4
AND5	: 4
AND6	: 3
AND7	: 1
AND8	: 6
INV	: 241
OR2	: 130
XOR2	: 132
IO Buffers	: 32
IBUF	: 16
OBUF	: 16

The RTL view of the multiplier module requires 818 gate counts.

VI. Conclusion

The data memory as asserted by load and store instruction which can read or write data to memory. The VHDL language is use to design the modules like Register, Instruction Memory, Data Memory , instruction fetch unit, instruction decode unit, the control unit, and execution unit etc. Thus we design the multiplier and adder module with improve latency and computational time of 100ns.

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