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Design and Analysis of a Conventional Wallace Multiplier in 180nm CMOS Technology

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Abstract: *Multiplier is an important building block in many electronic system design. There are many available methods and techniques for designing multipliers. Wallace multiplier is important and popular multiplier architecture. In this paper, design and analysis of a conventional Wallace multiplier is presented by using Cadence virtuoso in 180nm CMOS technology. Performance analysis in terms of power, delay, and power delay product are performed for a 4-bit Wallace multiplier in 180nm CMOS technology. The power and delay of the designed multiplier are 689.3µW and 50µs respectively.*
Keywords: *Delay, Multiplier, Power delay product, Power Dissipation, Wallace multiplier.*

I. Introduction

In any signal processing system, multiplier is an important and a basic building block element [1]. The performance of these types of processing systems depends on the performance of the inbuilt multiplier [2]. So it is a challenging task for any designer to design a high performance multiplier. There are different factors that drive for high performance electronic system design in terms of low power dissipation and high speed [3-4].

The block diagram of a multiplier is shown in Fig.1. A basic multiplier consists of three stages: generation of partial product, addition of partial product and final addition.

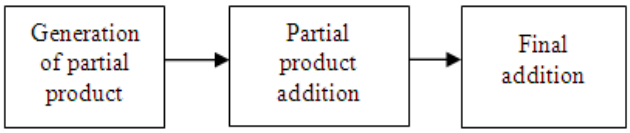

Fig.1 Block diagram of a multiplier

A multiplier based on Wallace-tree structure is called Wallace multiplier. It is substantially faster than other multiplier architecture [5]. The operation of a Wallace multiplier is carried out in three different steps [5-7]. After generating the partial product, these are accumulated in different stages.

The different steps involved in Wallace multiplier are:
Step1: Partial product generation.
Step2: (i) Accumulation of partial product in different stages by

$$R_{i+1} = 2(R_i /3) + R_i \bmod 3 \qquad (1)$$

where R_i denotes the groups or stages and R_0 =N, is the number of rows in the initial bit product array

(ii) Adjacent three rows are reduced by using the full adder and the half adder. Remaining rows are carried to the next step. The process continues until last stage contains two rows.

Step3: Remaining two rows are added by the full adder.

II. Designing A Wallace Multiplier

Fig. 2 shows a 4-bit conventional Wallace multiplier by applying all the three steps of the multiplication process. S00, S01, S02, S03, S10, S11, S12, S13, S20, S21, S22, S23, S30, S31, S32 and S33 are the partial product terms, while Z0, Z1, Z2, Z3, Z4, Z5, Z6 and Z7 are the final product.

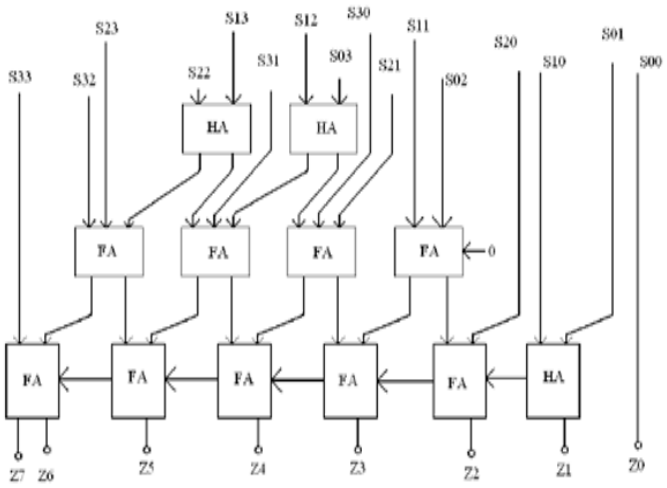

Fig.2 Architecture of a 4x4 Wallace multiplier

A Wallace multiplier is designed in three different modules:
i. Partial product generation module.
ii. Grouping of partial product module.
ii. Final addition module.

2.1 Designing Of Partial Product Module

The partial product module of a 4-bit Wallace multiplier is shown in Fig.3. For generating the partial product, AND gate is used. The total number of partial product in a 4-bit Wallace multiplier is 16. So for designing the partial product module, 16 AND gates are used. The cellview of the partial product generator is also designed and is shown in Fig.4.

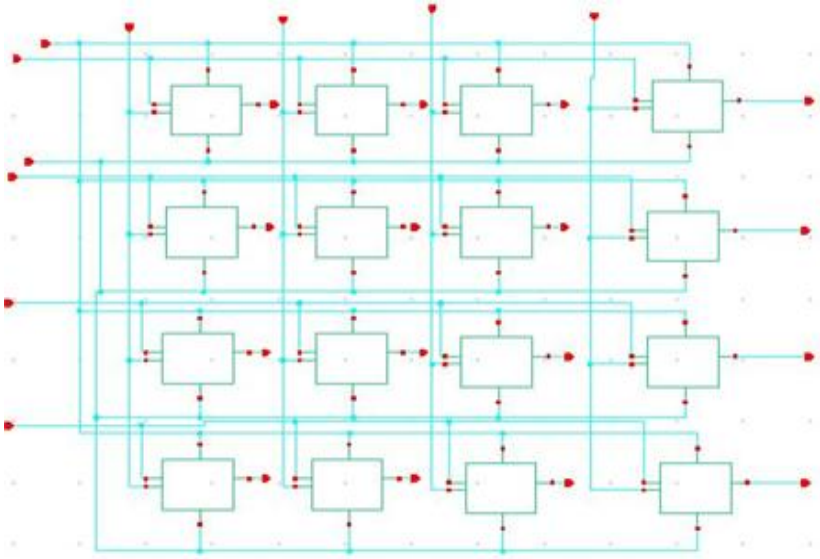

Fig.3 Partial product generation module

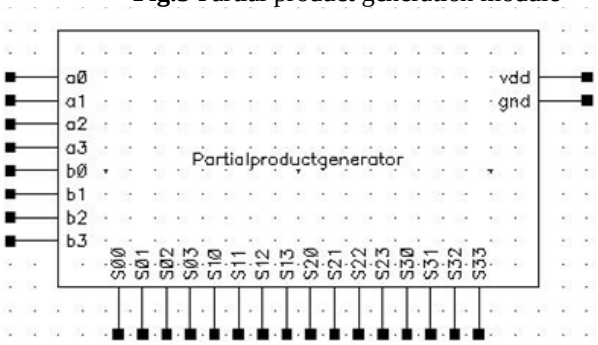

Fig.4 Cellview of partial product generator module

2.2 Grouping Of Partial Product Module

Fig.5. shows the grouping of partial product module of a 4-bit Wallace multiplier. (1) is used for grouping of the partial product. For two bit addition, half adder is used and for three bit addition, full adder is used. The cellview of grouping of partial product module is shown in Fig.6.

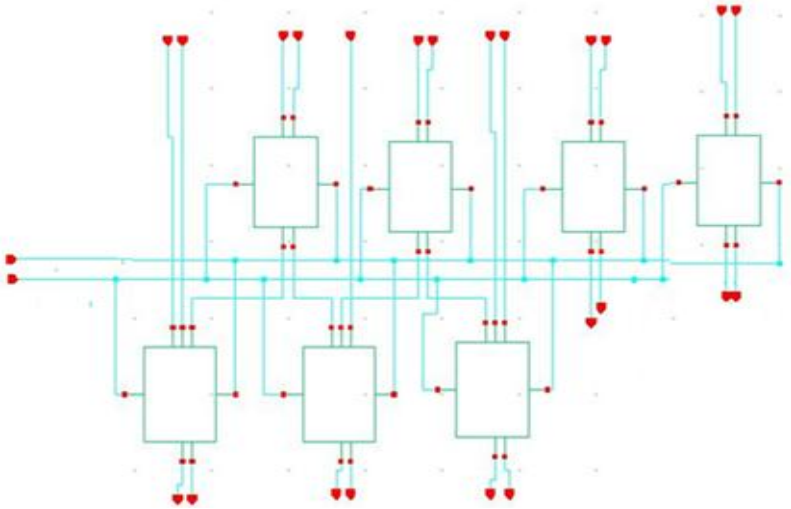

Fig.5 Grouping of partial product module

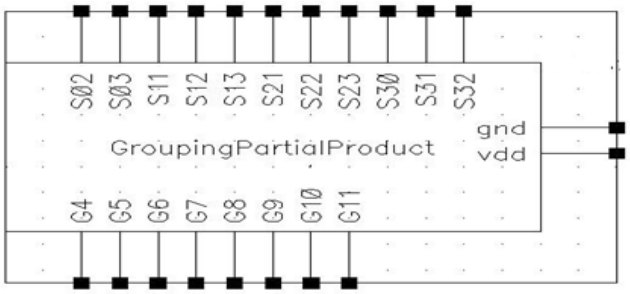

Fig.6 Cellview of grouping of partial product module

2.3 Final Addition Module

Fig.7 shows the final addition module of a 4-bit Wallace multiplier. After the grouping and staging of partial product, final addition module is designed. The cellview of the final addition module is shown in Fig. 8. In this figure, P1, P2, P3, P4, P5, P6 and P7 are final product terms.

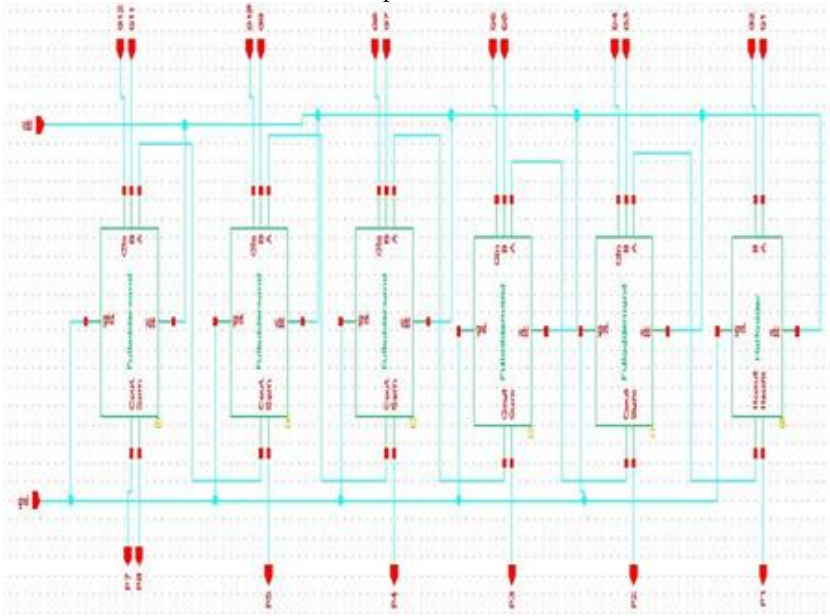

Fig.7 Final addition module

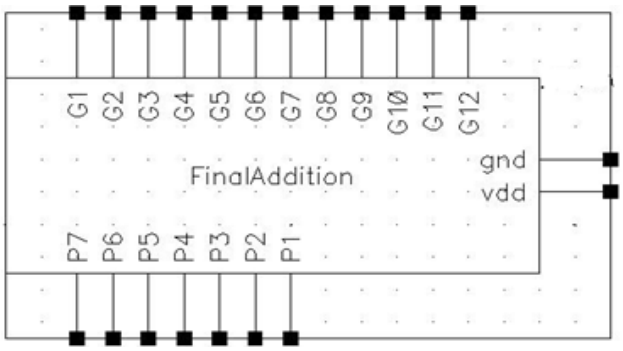

Fig.8 Cellview of final addition module

2.4 Designing A 4-Bit Wallace Multiplier

A 4-bit Wallace multiplier is shown in Fig. 9, which is designed after combining all the three modules. The inputs are connected to the partial product generator module and the outputs of the partial product module are connected as per the architecture of Wallace multiplier.

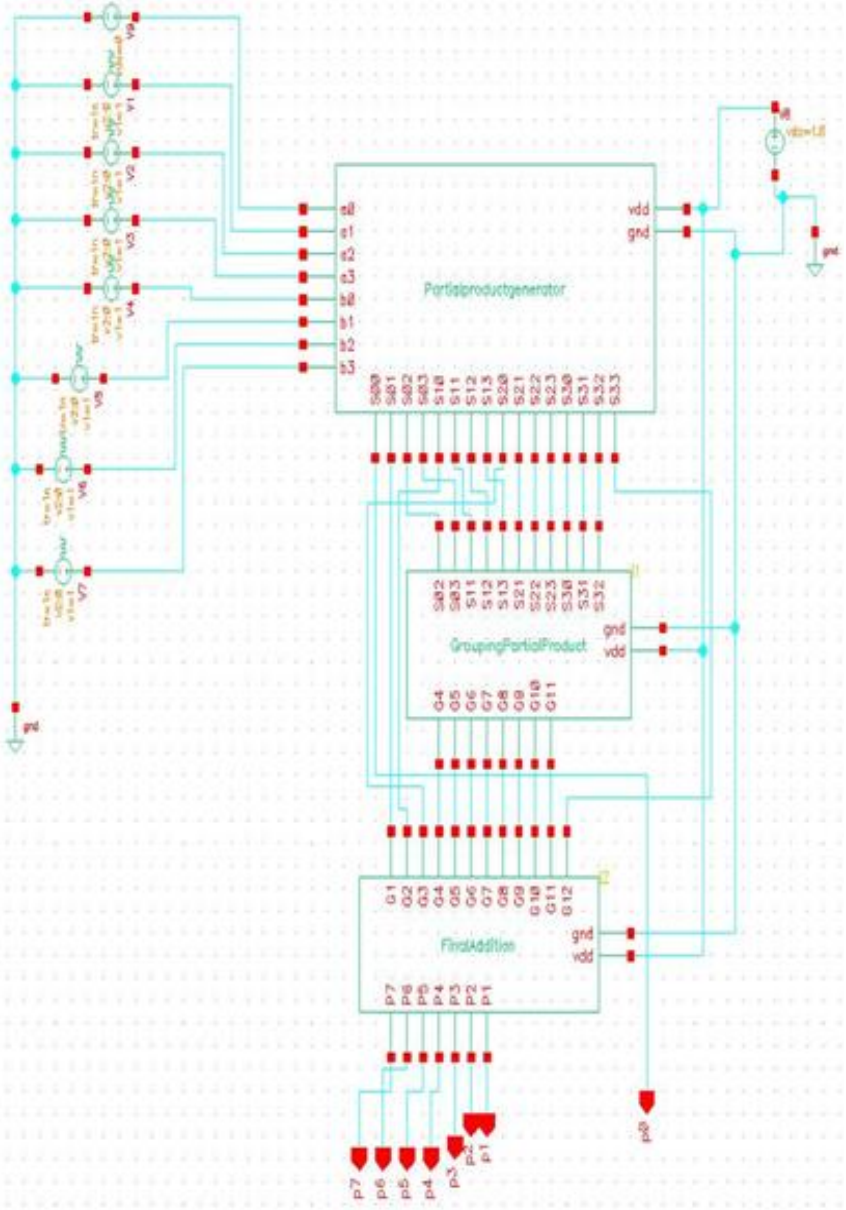

Fig. 8 A 4-bit Wallace multiplier

III. Results And Analysis

Cadence Virtuoso is used for designing a 4-bit Wallace multiplier in 180nm CMOS technology. Transient analysis is performed for this multiplier. Performance analysis in terms of power dissipation, delay, and power delay product are observed by using Cadence virtuoso in 180nm CMOS technology. The conventional 4-bit Wallace multiplier is designed by using AND gate, half adder and full adder. Table 1 shows the total numbers of components used for designing this multiplier.

Table 1: Total number of components used in designing a 4-bit conventional Wallace multiplier

Total number of PMOS used	249
Total number of NMOS used	249
Total number of half adder used	3
Total number of full adder used	9

3.1 Transient Analysis

The transient analysis of a 4-bit Wallace multiplier is done by applying two inputs each of 4-bit. Input and output transient waveforms for the multiplier are shown in the Fig.9 and Fig.10 respectively.

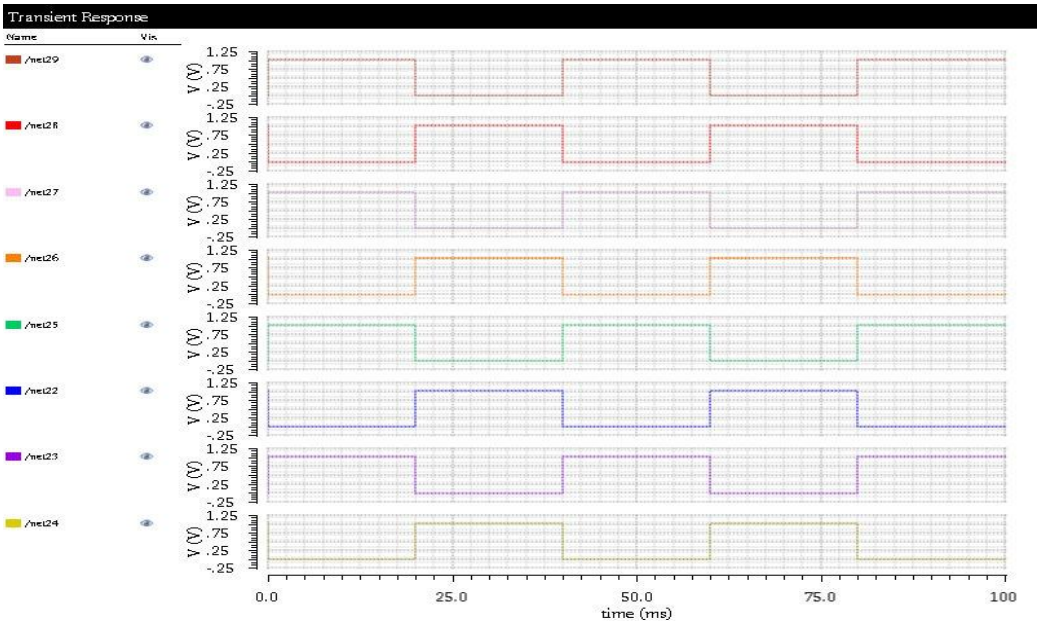

Fig.9 Input transient waveform

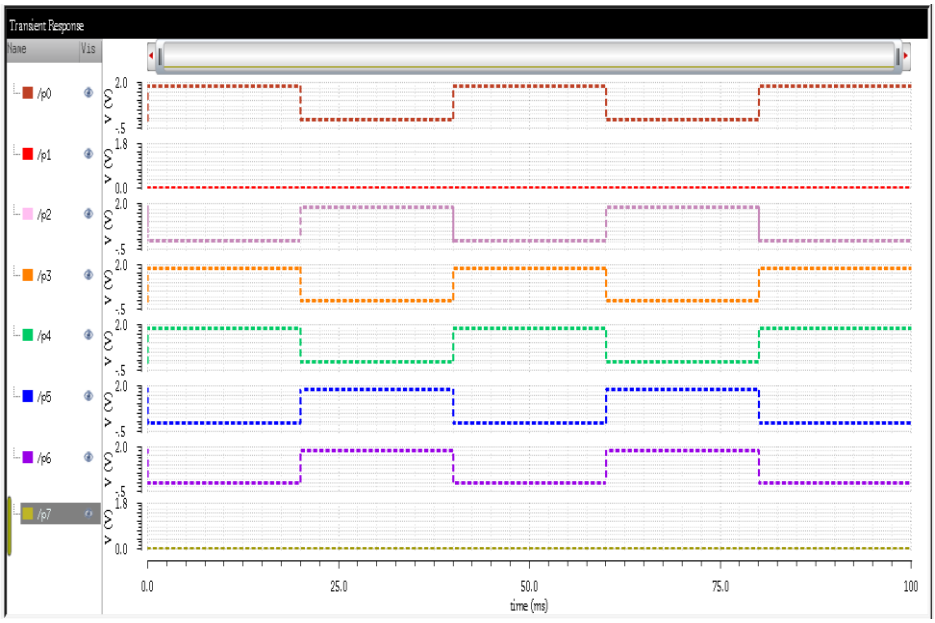

Fig.10 Output transient waveform

3.2 Performance Analysis

Table 2 shows the performance of a 4-bit Wallace multiplier in terms of power dissipation, delay, and power delay product.

Table 2: Performance of a 4-bit Wallace multiplier

Power dissipation	689.3µW
Delay	50µs
Power delay product	34.465nWs

IV. Conclusion

In this paper, design and analysis of a conventional 4-bit Wallace multiplier is performed in 180nm CMOS technology. The power and delay of the designed multiplier are found to be 689.3µW and 50µs.

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