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# Performance Analysis of a 6T SRAM Cell in 180nm CMOS Technology

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***Abstract :*** *SRAM is a memory component and is used in various VLSI chips due to its unique capability to retain data. This memory cell has become a subject of research to meet the demands for future communication systems. In this paper a 6T SRAM cell is designed by using cadence virtuoso EDA tool in 180nm CMOS technology. Its performance characteristics such as power dissipation, delay, and power delay product are analysed. Power dissipation, delay, and power delay product of the designed 6T SRAM cell are 54.63 x10$^{-9}$ W, 19.96 x10$^{-9}$s, and 1070.45 x 10$^{-18}$ Ws respectively.*

***Keywords:*** *Power, Delay, Power delay product, 6T SRAM cell.*

## I. Introduction

Static random access memory (SRAM) is a static memory cell which is widely used in various electronic systems. It is faster and consumes less power as compared to other memory cells [1-2]. It does not require refreshing periodically. Because of this, SRAM is the most popular memory cell among VLSI designers. Hence continuous evolution is going on for better performance of SRAM cells. Due to this, different types of SRAM cells are available in the literature like 6T SRAM cell, 7T SRAM cell, 8T SRAM cell, 9T SRAM cell etc. Most common SRAM cells used in digital system is the 6T SRAM cell. This cell can store 1-bit of data. The bit remains in the cell as long as power is supplied. In this paper, design and performance analysis of a 6T SRAM cell is discussed. Performance analysis is carried out by using Cadence Virtuoso in 180nm CMOS technology.

A conventional 6T SRAM cell consists of two inverters which are connected back to back. Fig. 1 shows the basic structure of a 6T SRAM memory cell [3]. The data which has to be stored is latched in these two inverters. The process of storing a data is known as Write operation and the process of recovering the data is known as Read operation. Write operation is used for uploading the contents in a SRAM cell while Read operation is used for fetching the contents. The read operation is done with the help of sense circuits which sense BL and BLB data line before discharging it completely [4-5].

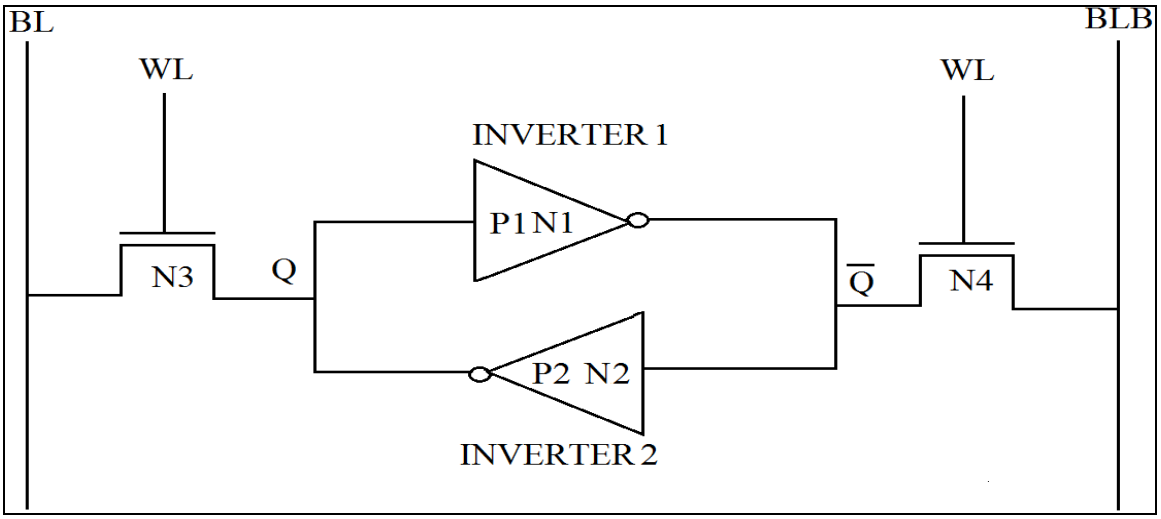


**Fig. 1** A 6T SRAM cell

## II. Design Of A 6T SRAM CELL

The schematic diagram of the designed 6T SRAM cell is shown in Fig. 2. The 6T SRAM cell is designed by using Cadence Virtuoso EDA tool in 180nm CMOS technology.

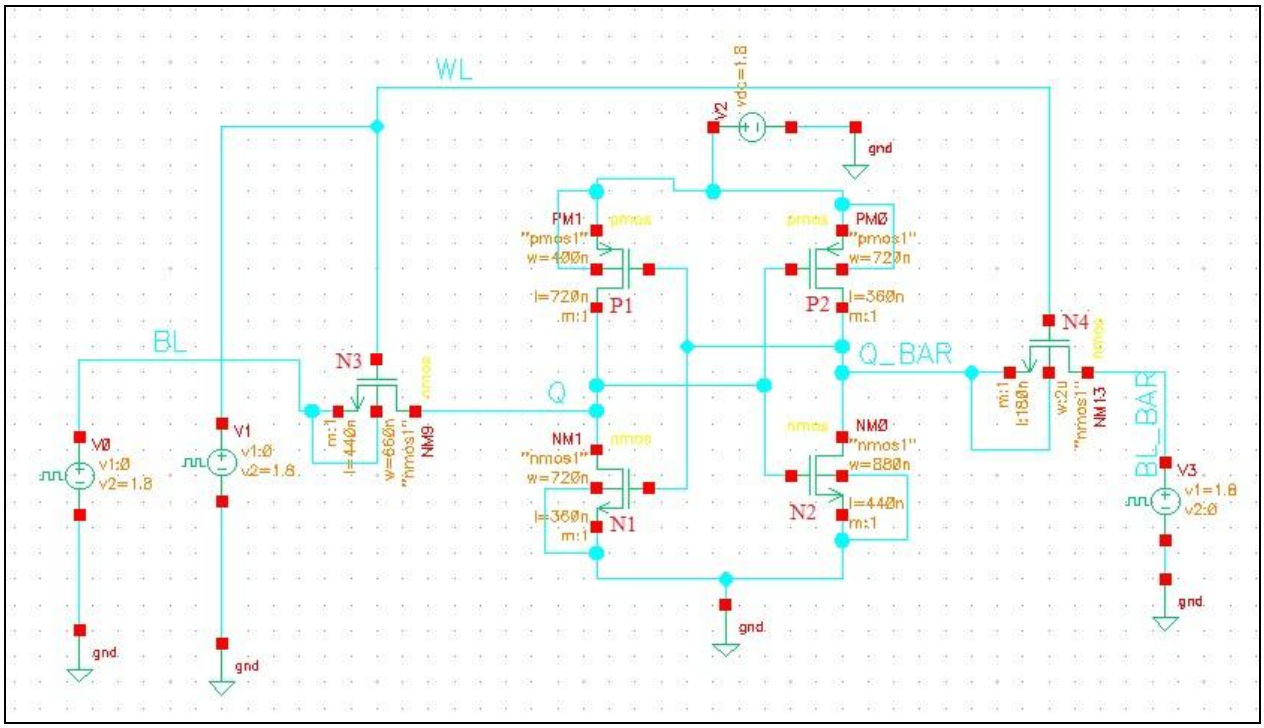


**Fig. 2** Schematic of a 6T SRAM cell

## III. Results And Performance Analysis

Fig. 3 shows the transient waveform of the designed 6T SRAM cell for wordline, Bitline, Q and Q_bar. Table 1 shows the performance characteristics such as power dissipation, delay, and power delay product of the designed 6T SRAM cell in 180nm CMOS technology at power supply voltage ($V_{DD}$) of 1.8V.

**Table 1:** Power dissipation, delay and power delay product of the designed 6T SRAM cell

| Power dissipation | Delay | Power delay product |
|---|---|---|
| 53.63 x $10^{-9}$ W | 19.96 x $10^{-9}$s | 1070.45 x $10^{-18}$ Ws |

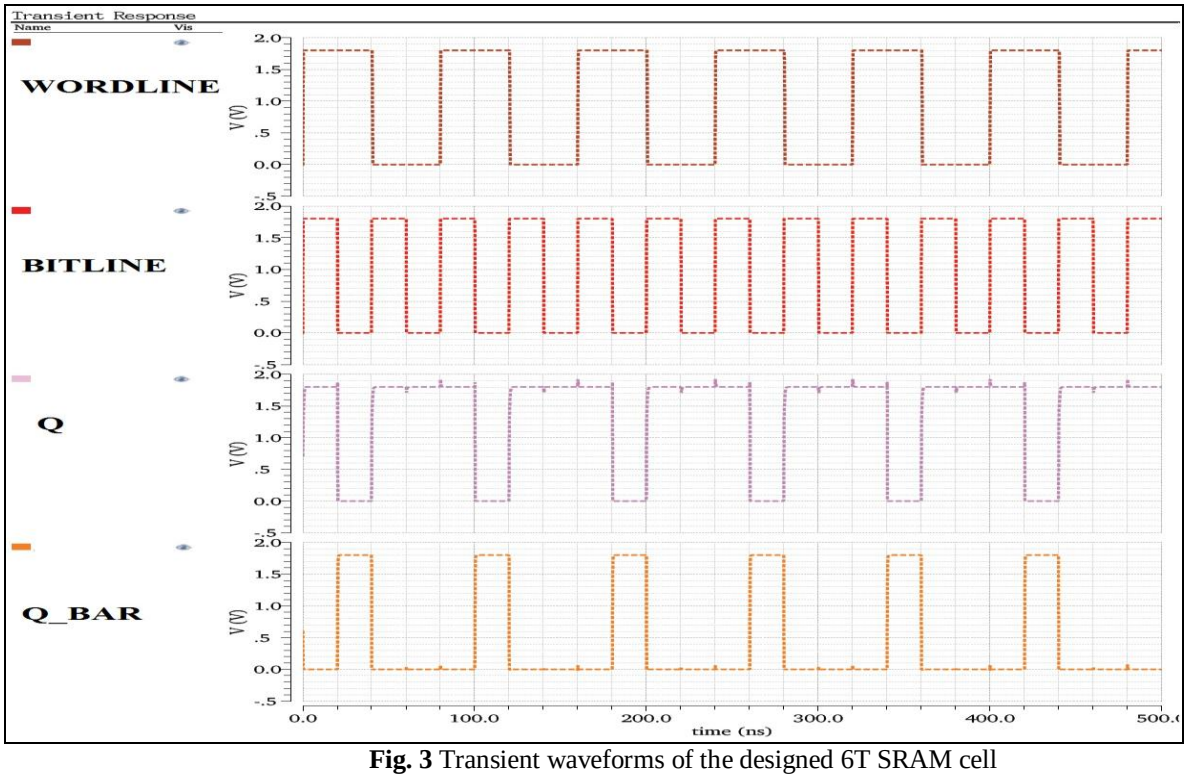


**Fig. 3** Transient waveforms of the designed 6T SRAM cell

## IV. Conclusion

A 6T SRAM cell is designed and its performance characteristics such as power, delay, and power delay product are analysed in 180nm CMOS technology. Power dissipation, delay, and power delay product of the designed 6T SRAM cell are 54.63 $x10^{-9}$ W, 19.96 $x10^{-9}$ s, and 1070.45 x $10^{-18}$ Ws respectively.

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