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Implementation of 2-D Dct Architecture for Optimized Area And Power Utilization

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Abstract: *In this paper, a new approach for 2-D DCT architecture is introduced where both area and power are improved simultaneously. To reduce the area the proposed architecture is designed with tristate buffers. It can calculate first-dimensional and second-dimensional transformations simultaneously by using 1-D discrete cosine transform (DCT) core to reach less hardware utilization. Modules in the 1-D DCT core, including the modified two-input butterfly (MBF2), the pre-reorder, the process element even (PEE), the process element odd (PEO), and the post reorder are designed using the VERILOG HDL. The adders in the design are replaced by a low power reversible Vedic adder to improve the overall performance of the system. The functionality is verified successfully using the XILINX ISE 12.3i EDA tool.*

Keywords: *Discrete cosines transform (DCT), Reversible logic and Vedic mathematics.*

I. Introduction

Transform coding constitutes an integral component of contemporary image/video processing applications. Transform coding relies on the premise that pixels in an image exhibit a certain level of correlation with their neighboring pixels. Similarly in a video transmission system, adjacent pixels in consecutive frames2 show very high correlation. Consequently, these

Correlations can be exploited to predict the value of a pixel from its respective neighbors. A transformation is, therefore, defined to map this spatial (correlated) data into transformed (uncorrelated) coefficients. Clearly, the transformation should utilize the fact that the information content of an individual pixel is relatively small i.e., to a large extent visual contribution of a pixel can be predicted using its neighbors.

A typical image/video transmission system is outlined in Figure 1. The objective of the source encoder is to exploit the redundancies in image data to provide compression. In other words, the source encoder reduces the entropy, which in our case means decrease in the average number of bits required to represent the image. On the contrary, the channel encoder adds redundancy to the output of the source encoder in order to enhance the reliability of the transmission. Clearly, both these high-level blocks have contradictory objectives and their interplay is an active research area. However, discussion on joint source channel coding is out of the scope of this document and this document mainly focuses on the transformation block in the source encoder. Nevertheless, pertinent details about other blocks will be provided as required.

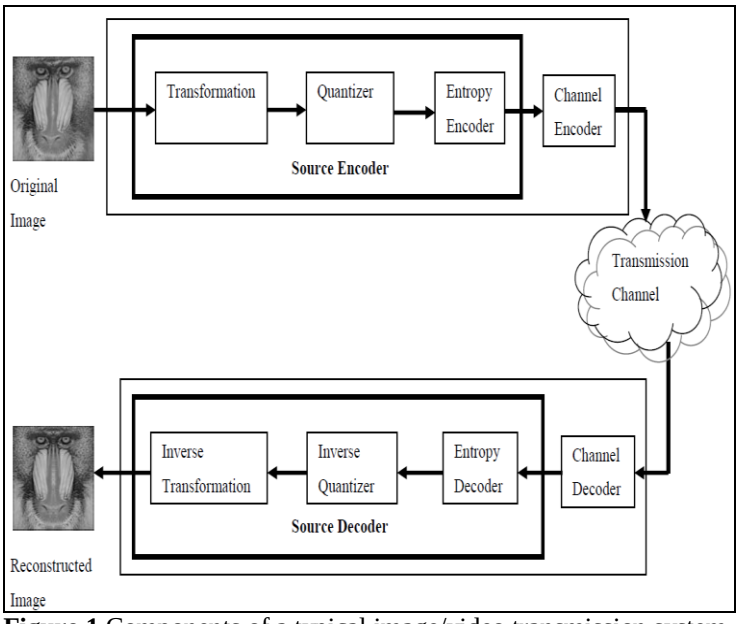


Figure 1. Components of a typical image/video transmission system.

II. The Discrete Cosine Transform

Like other transforms, the Discrete Cosine Transform (DCT) attempts to decorrelate the image data. After decorrelation each transform coefficient can be encoded independently without losing compression efficiency. This section describes the DCT and some of its important properties.

A discrete cosine transform (DCT) expresses a finite sequence of data points in terms of a sum of cosine functions oscillating at different frequencies. DCTs are important to numerous applications in science and engineering, from lossy compression of audio (e.g. MP3)and images(e.g. JPEG) (where small high-frequency components can be discarded), to spectral methods for the numerical solution of partial differential equations. The use of cosine rather than sine functions is critical for compression, since it turns out (as described below) that fewer cosine functions are needed to approximate a typical signal, whereas for differential equations the cosines express a particular choice of boundary conditions.

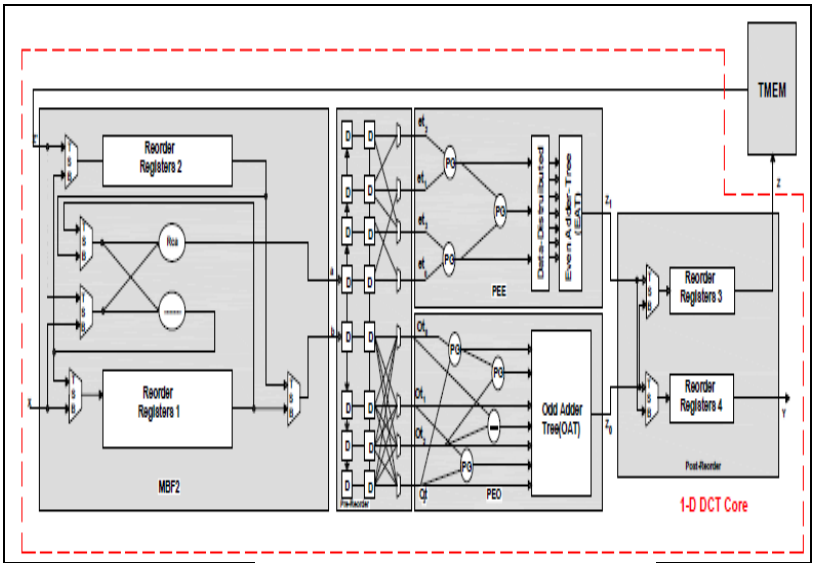


Figure 2. Proposed DCT architecture

In the proposed DCT architecture the multiplexor is replaced by a tristate buffer to reduce the area. A tri-state buffer is a device that ALLOWS you to control when an output signal makes it to the bus. When the tri-state buffer's control bit is active, the input of the device makes it to the output. This is when the "valve" is open.

When it's not active, the output of the device is Z, which is high-impedance or, equivalently, nothing. This is when the "valve" is CLOSED, and no electrical signal is allowed to pass to the output. The output of the MBF2 module is applied to pre reorder module whose output is given to the post reorder module. In the PEE and PEO block the element is implemented using reversible gate PG (Peres gate).This gate is responsible for power consumption optimization.

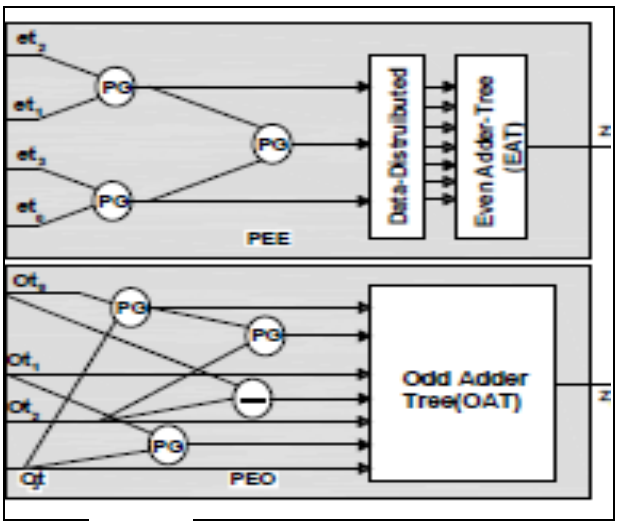


Figure 3. Architecture for Proposed PEE and PEO

The above architecture gives the flow diagram of the PEE and PEO. The adder is implemented using reversible gate by maintaining the same functionality.

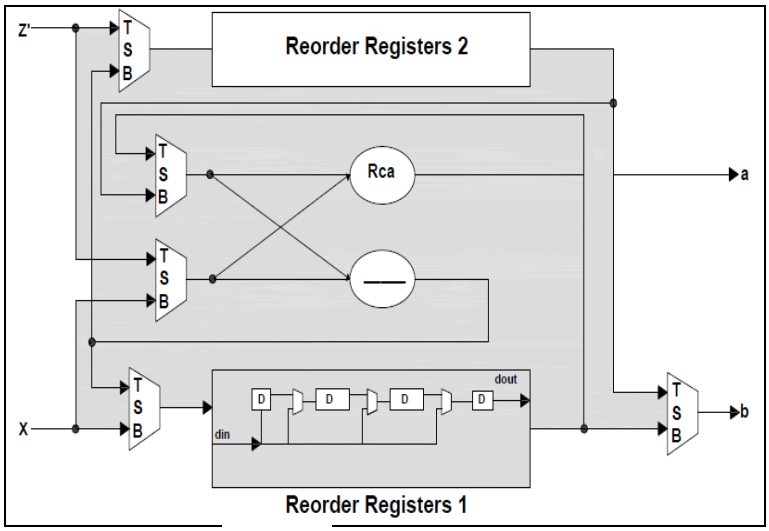


Figure 4. MBF2 Architecture.

The above architecture gives the flow diagram of the MBF2 module where multiplexor is replaced by tristate buffer. Vedic Mathematics is one of the most ancient methodologies used by the Aryans in order to perform mathematical calculations. This consists of algorithms that can boil down large arithmetic operations to simple mind calculations. The above said advantage stems from the fact that Vedic mathematics approach is totally different and considered very close to the way a human mind works. The efforts put by Jagadguru Swami Sri Bharati Krishna Tirtha Maharaja to introduce Vedic Mathematics to the commoners as well as streamline Vedic Algorithms into 16 categories or Sutras needs to be acknowledged and appreciated. The Urdhva Tiryakbhayam is one such multiplication algorithm which is well known for its efficiency in reducing the calculations involved.

With the advancement in the VLSI technology, there is an ever increasing quench for portable and embedded Digital Signal Processing (DSP) systems. DSP is omnipresent in almost every engineering discipline. Faster additions and multiplications are the order of the day. Multiplication is the most basic and frequently used operations in a CPU. Multiplication is an operation of scaling one number by another. Multiplication operations also form the basis for other complex operations such as convolution, Discrete Fourier Transform, Fast Fourier Transforms, etc. With ever increasing need for faster clock frequency it becomes imperative to have faster arithmetic unit. Therefore, DSP engineers are constantly looking for new algorithms and hardware to implement them.

Vedic mathematics can be aptly employed here to perform multiplication. Another important area which any DSP engineer has to concentrate is the power dissipation, the first one being speed. There is always a trade-off between the power dissipated and speed of operation. The reversible computation is one such field that assures zero power dissipation. Thus during the design of any reversible circuit the delay is the only criteria that has to be taken care of. In a reversible Urdhva Tiryakbhayam Multiplier had been proposed.

III. Bit Ripple Carry Adder Using Vedic Mhematics

Vedic mathematics is the ancient Indian system of mathematics which mainly deals with Vedic mathematical formulae and their application to various branches of mathematics. Vedic mathematics was reconstructed from the ancient Indian scriptures (Vedas) by Sri Bharati Krsna Tirtha after his research on Vedas. He constructed 16 sutras and 16 upa sutras after extensive research in Atharva Veda. The most famous among these 16 are Nikhilam Sutram, Urdhva Tiryakbhayam, and Anurupye. It has been found that Urdhva Tiryakbhayam is the most efficient among these. The beauty of Vedic mathematics lies in the fact that it reduces otherwise cumbersome looking calculations in conventional mathematics to very simple ones. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Hence multiplications in DSP blocks can be performed at faster rate. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering.

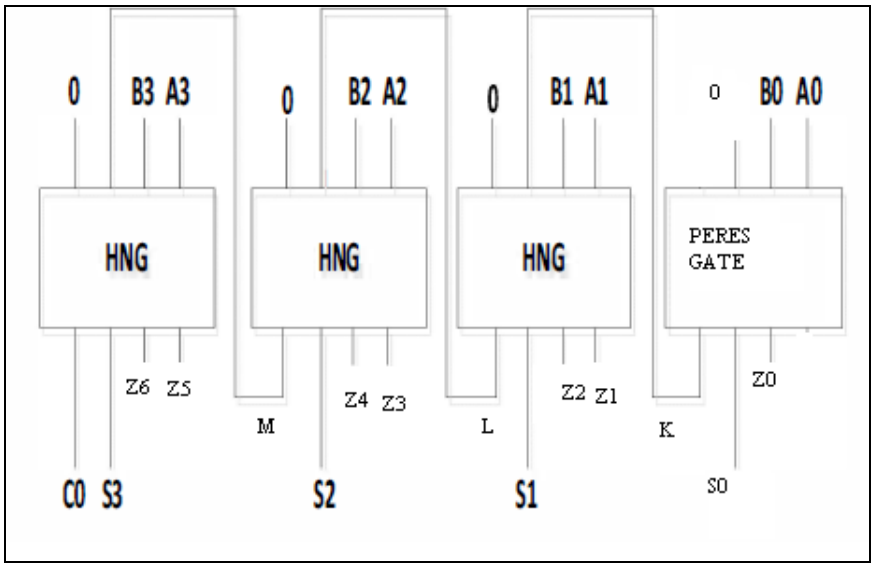


Figure 5. four bit ripple carry adder.

Inputs a[0] and b[0] including with 0 are given as inputs to PERES gate and z0,s0 and k are taken as outputs. The carry generated from the peres gate(k) is given as one of the inputs to HNG 1gate.S1 is taken as sum bit and L as carry bit. The carry bit generated from HNG 1 gate is given as one to the inputs to HNG 2 gate. Like that the Ripple carry adder has to proceed. In general the Ripple carry adder is designed with full adders which will propagate the carry to the next gate and continues so on. In the proposed RCA the main advantage is always one input tied to logic '0' by satisfying the functionality. So obviously the power consumption will be reduced due to this modification and at the same time these gates are reversible.

IV. Reversible Logic Gates

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs.

Peres Gate:

Peres gate which is a 3*3 gate having inputs (A, B, C) and outputs P = A; Q = A XOR B; R = AB XOR C. It has Quantum cost four.

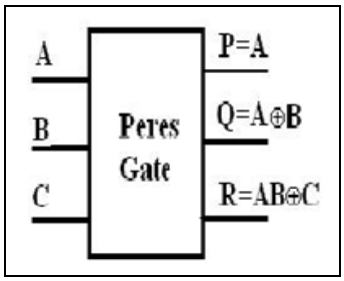


Figure 6. PERES gate and its symbolic representation

HNG Gate:

The reversible HNG gate can work singly as a reversible full adder. If the input vector IV = (A, B, Cin, 0), then the output vector becomes OV = (P=A, Q=Cin, R=Sum, S=Cout).

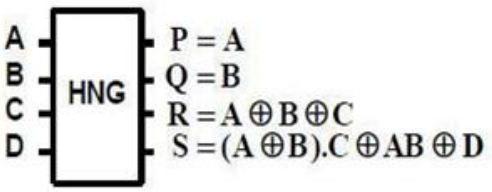


Figure 7. HNG Gate and its symbolic representation

Proof For A Gate To Be Reversible.

Let us consider PERES gate which is shown in Figure 6. A, B and C are taken as inputs and P,Q,R are taken as outputs.

For example consider P = 0, Q = 1, R = 1.Now our task is to obtain inputs from the known output.

As P = A, A = 0;

$Q = 0 \oplus B$

$1 = B$. Hence B = 1.

$R = AB \oplus C$

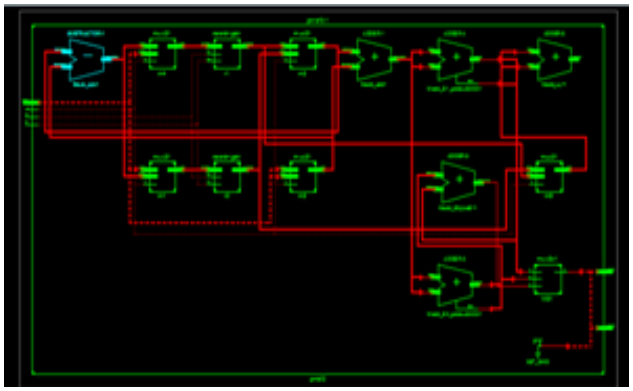
$1 = (0.1) \oplus C$.

C = 1.

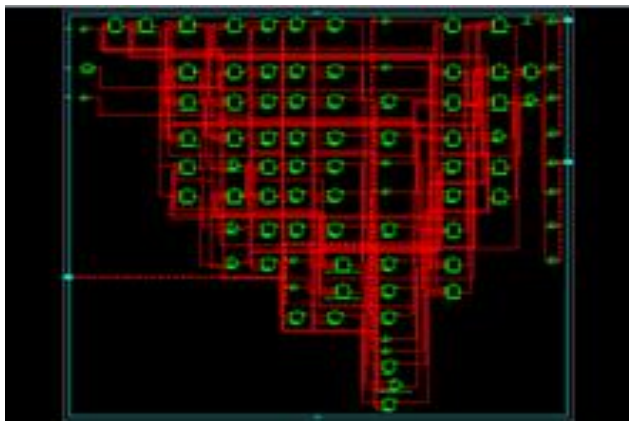
A = 0,B = 1,C = 1 are obtained from the known outputs.

V. Results

RTL Schematic:



Technology Schematic:

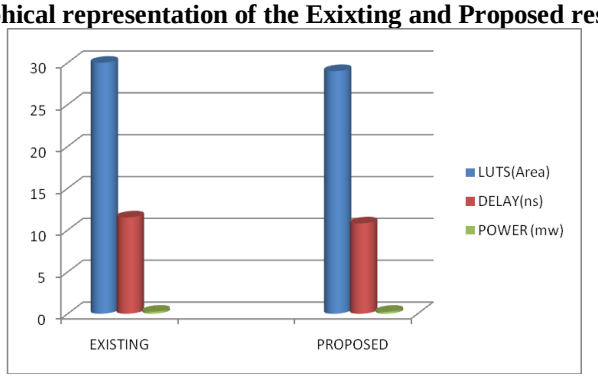


Waveform:

Comparison Table

	LUTS(Area)	TOTAL DELAY	POWER CONSUMED
Proposed	29	10.796ns.	0.23643mw.
Existing	30	11.512ns	0.24458mw

Graphical representation of the Exixting and Proposed results



VI. Conclusion

In this paper the 2-D DCT Architecture is implemented by using Reversible Vedic adder approach. the proposed architecture is designed in such a way that the same architecture is used for both 1D and 2D applications using cascading approaches. The functionality and synthesis is carried out using XILINX ISE 12.3i EDA tool. VERILOG HDL is used to describe the functionality. From the Synthesis results which is mentioned in the comparison table it is concluded that the Delay of 10.796ns along with power consumption of 0.23643mw is reduced when compare with the existing architecture due to replacement of adders with reversible Vedic adder approach along with usage to tristate buffers.

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