IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 5, Issue 5, Ver. I (Sep - Oct. 2015), PP 60-65
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Implementation of FFT Butterfly Algorithm Using SMB Recoding Techniques

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***Abstract**: Arithmetic operations of high complexity are widely used in Digital Signal Processing (DSP) applications. The FFT algorithms use butterfly method in order to find the output. The Butterfly method includes an addition followed by a multiplication. In this work, we focus on optimizing the design of the fused Add-Multiply (FAM) operator for increasing performance and hence the FFT. Optimization of fused add multiply operation is done using three techniques. A direct recoding of the sum of two numbers in its Modified booth form is utilized. The delay and area comparison of the three techniques is done and best algorithm will be used in the Butterfly algorithm of FFT to obtain higher efficiency and Lower Delay. Here SMB2 was found to be lowest in terms of area and delay and it was used in the implementation of butterfly algorithm*
***Keywords:** Booth Recoding; Fused Add Multiply; FPGA; VLSI Design ; Butterfly Algorithm ;FFT*

I. Introduction

The most important need of any VLSI circuit is to have a very high speed and efficient addition. Adders are the essential building blocks of mathematical algorithms in VLSI Circuits. Different techniques were used inorder to increase the speed and to reduce the delay of addition and multiplication. Modified Booth Techniques give a higher speed of addition and Lower Delay than the conventional modes of Multiplication. Modified Booth Algorithm will reduce the number of partial products in a multiplication by half than the conventional multipliers. The modified Booth Algorithm can be used to code the sum of two numbers and can thus be used in the Fused Add Mulitply operation.

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II. Fused Add Multiplication (Fam)

The Addition and Multiplication is combined together to form a single algorithm. This will help reduce the number of partial products in multiplication and hence improve the speed and efficiency of the operation significantly

In the FAM design presented in Fig. 1(b), the multiplier is a parallel one based on the MB algorithm. Let us consider the product X.Y. The term Y is encoded based on the MB algorithm and multiplied with X . Both X and Y consist of n=2k bits and are in 2s complement form.

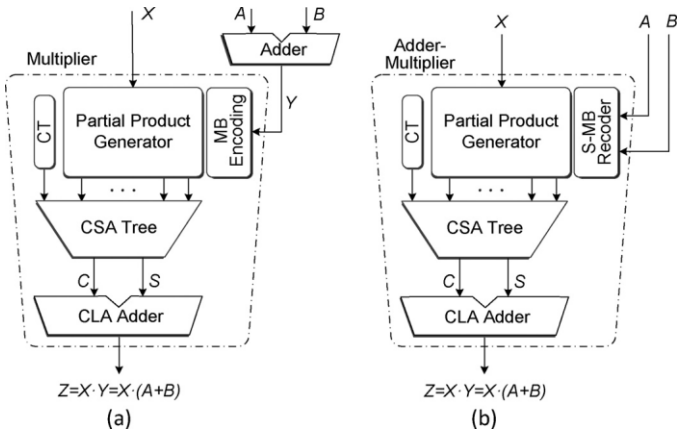

Fig1. Conventional and Fused Add Multiply Operation

III. Sum To Modified Booth Algorithm (Smb)

In S-MB recoding technique, we recode the sum of two consecutive bits of the input A(a2j ,a2j+1) with two consecutive bits of the input B(b2j ,b2j+1) into one MB digit yjMB . As we observe three bits are included in forming a MB digit. The most significant of them is negatively weighted while the two least significant of them have positive weight. This signifies the need of a signed bit arithmetic in order for the signed bit multiplication.

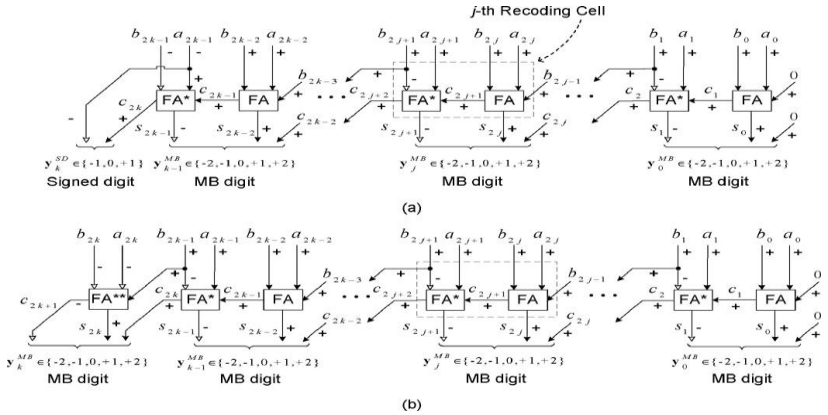

Fig 2. SMB1 Recoding Scheme

There are many advantages for a Sum to Modified Booth recoding technique. There is no carry Ripple. This will significantly reduce the delay and power. The Delay is constant irrespective of the number of bits. There are three different schemes used in SMB recoding Techniques.

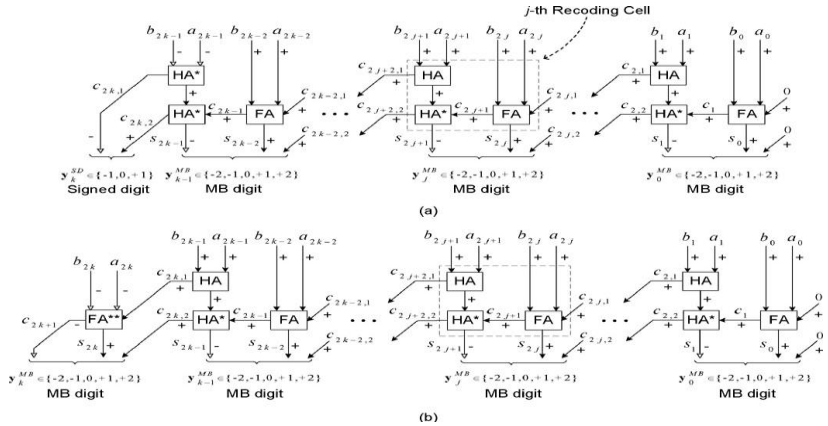

Fig 3 . SMB2 Recoding Scheme

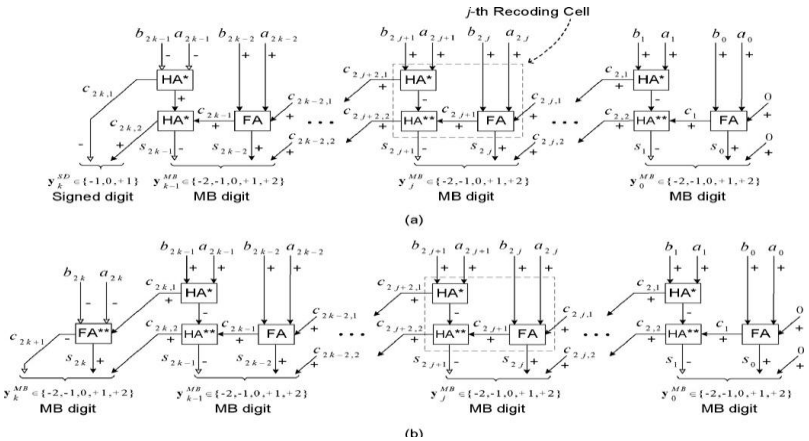

Fig 4 SMB3 Recoding Scheme

IV. Verilog Implementation

The different SMB recoding Techniques were simulated in Verilog ISE.

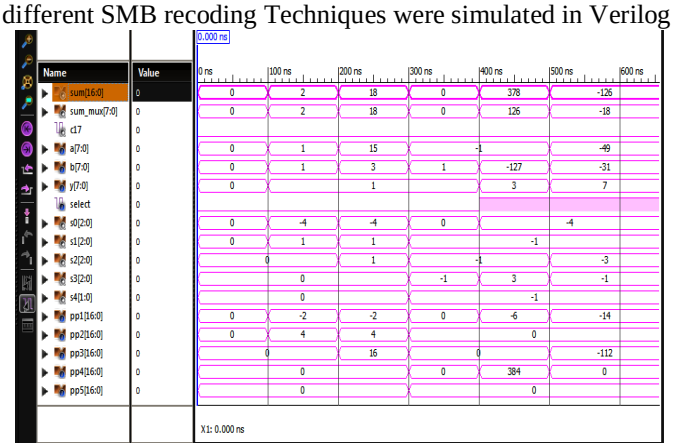

Fig 5: Verilog Implementation

V. Delay Comparison

The delay Comparison is as shown in the figure below

TYPE	DELAY
MODIFIED BOOTH	6
SMB1 EVEN	5
SMB2 EVEN	3
SMB3 EVEN	5
SMB1 ODD	6
SMB2 ODD	5
SMB3 ODD	8

Table 1. Delay Comparison

VI. Fft Butterfly Algorithm

We uses the SMB2 Recoding Technique because it has the lowest delay of all the proposed recoding techniques. It has a constant delay. The technique can be used in the implementation of FFT using the butterfly diagram as shown in the figure.

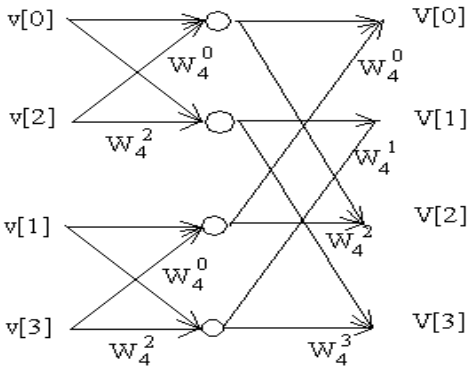

Fig.6 Butterfly Algorithm

Here the values of the input is directly booth encoded by the SMB2 technique and then the twiddle factor in the FFT is chosen as the third element. The Fig.7. as per the algorithm produces real and imaginary part. The implementation of the same is done with the design shown in Fig.8. The real is produced by a full adder with a mux so that it enables the operation with negative numbers also. The second adder used is of SMB2 which produces the recoded output to the booth multiplier thus giving low delay.

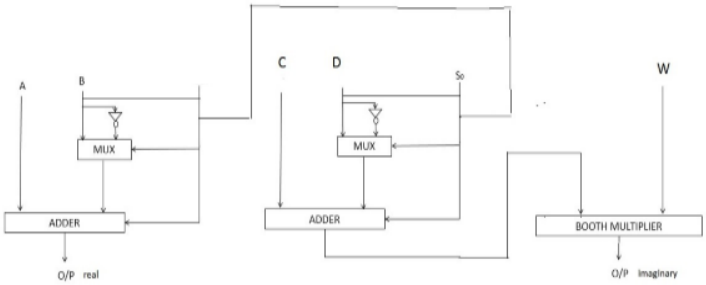

Fig. 7. Implementation Of Butterfly Algorithm

The Delay comparison of the conventional method using multipliers and adders and the proposed method using the Sum to Modified Booth Recoding Technique is as shown in the table below

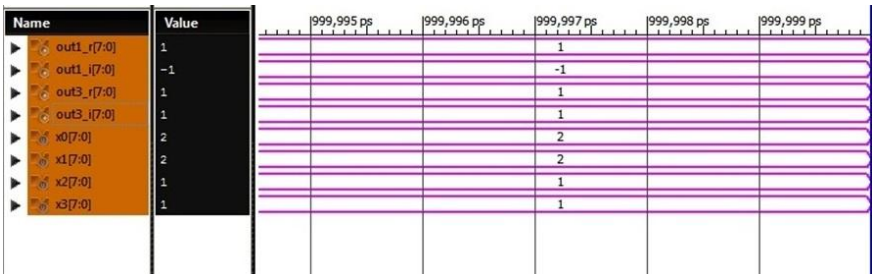

Fig. 8. Implementation Of Butterfly Algorithm in Xilinx ISE 14.6

	DELAY(ns)
Using multipliers and Adders	9.02
Proposed Design	5.04

Table 2. Delay Comparison btw Conventional And Proposed Designs of FFT

VII. Cadence Virtuoso Implementation

The Proposed Design was then implemented in Cadence virtuoso Software.

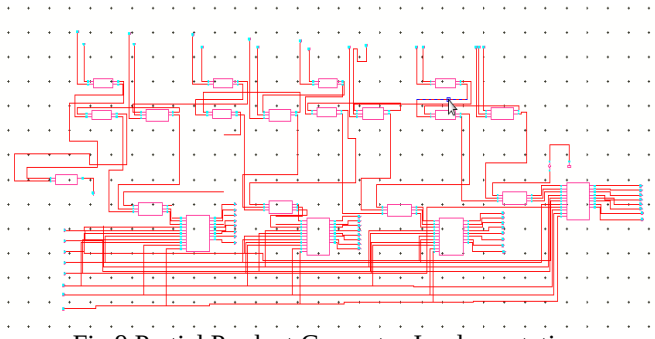

Fig.9 Partial Product Generator Implementation

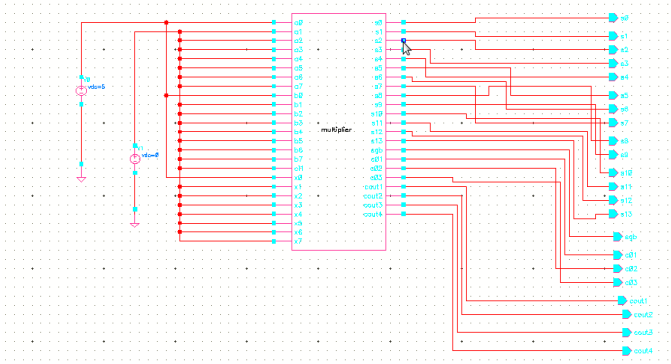

Fig. 10. Implementation of Multiplier

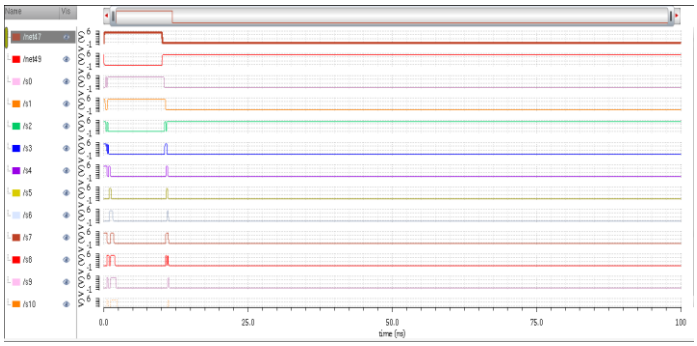

Fig 11. Cadence Virtuoso Output

VIII. Conclusion

The proposed design is an efficient technique for the implementation of FFT and similar techniques where an adder is followed by a multiplier. From the implementation we have proved that delay for the proposed design is much less than the direct implementation. The implementation has been done with the SMB2 type which has lowest and constant delay.The design has been implemented in Xilinx ISE 14.6 and Cadence virtuoso.

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