

## **Comparative Study Of Finfet Based 1-Bit Full Adder Cell Implemented Using TG And CMOS Logic Styles At 10, 22 And 32nm**

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**Abstract:** Paper discussed the comparative analysis of different full adder cells with two logic styles. The logic styles used for implementation of FinFET based 1-bit full adder are Complementary MOS (CMOS) and Transmission Gate (TG). The simulations of full adders have been done at 10nm, 20nm and 32nm technology node. PTM models for multi-gate transistors (PTM-MG) low power are used for simulations. This model is based on BSIM-CMG, a dedicated model for multi-gate devices. Investigation of performance and energy efficiency of all types of full adder cell designs has been done. The performance metrics that were measured, analyzed and compared are average power, leakage power, delay, and energy. It is observed that less power is consumed in Transmission Gate (TG) based full adder than the Conventional full adder in 10nm technology node.

**Keywords:** FinFET, Full Adder, Logic Styles, HSPICE

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### **I. Introduction**

Now a day, the demand of compact, high performance, low power and robust microprocessor is increasing day by day. The central processing unit (CPU) is the core of each microprocessor. The arithmetic logic unit (ALU) is key element of microprocessor located in CPU. ALU can perform logical operation and basic arithmetic operation, namely, addition, subtraction, multiplication, and division. The arithmetic operation can be performed as follows: addition, negative addition, repeated addition, and repeated negative addition. In digital system for nanotechnology node, it is required to design a full adder like that which have low power consumption, high speed, energy efficient, and reliable.

So, high speed, low power, energy efficient, and reliable microprocessors are in demand in the latest and innovative silicon technology processes have led to the rapid growth of modern integrated chip (IC). The VLSI microprocessors can be addressed at various design levels such as architectural, circuit, layout and fabrication. Designing an Arithmetic Unit at a particular circuit level effects its performance as various performance determining factors such as switching capacitance, transition activity and short circuit current are strongly influenced by chosen logic style. So, the objective of the paper is to find out the best efficient logic style between CMOS and TG for 1-bit Full Adder circuit.

There are two types of cell designs used for FinFET based full adder in this study, which are the Complementary MOS (CMOS) and Transmission Gate (TG). The circuit development and simulation were performed using HSPICE and CosmosScope. The design libraries were adapted from the Predictive Technology Model (PTM) for FinFET technology. The five metric performances of 1-bit full adder were analyzed: the propagation delay, average power dissipation, leakage power, power-delay-product (PDP), and energy-delay product (EDP) based on all four cell designs.

In Section II, overview of FinFET technology has been given. In Section III the logic styles used in experimentation is discussed. Section IV shows the Full Adder circuit design with different logic style. Section V presents FinFET parameters used. Performance analysis is done in section VI and presented obtained results. In section VI comparative results of cell designs are presented. The paper concludes in Section VIII.

### **II. Overview Of Finfet Technology**

FinFET is a non-planar device having 'fin' like shaped where the gate is wrapped around and over the fin which acts as a transistor channel. It is also termed as quasi-planar device as the current flows parallel to wafer plane and the channel is perpendicular to wafer plane.

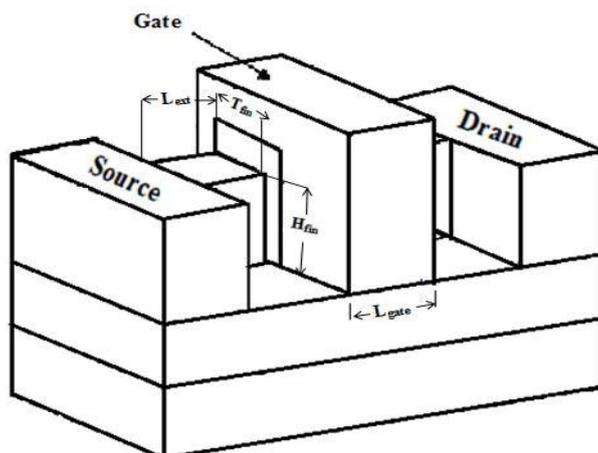


Fig.1: Structure of FinFET

Basically, FinFET was designed to be constructed on silicon-on-insulator (SOI) wafers. But the recent research has made it possible for FinFETs to work on bulk silicon wafers and improve the performance of certain parameters.

Effective channel length  $L_{eff} = L_{gate} + 2 \times L_{ext}$  (1)

Effective channel width  $W = T_{fin} + 2 \times H_{fin}$  (2)

Where  $H_{fin}$  and  $T_{fin}$  the fin height and thickness respectively,  $L_{gate}$  is length of the gate,  $L_{ext}$  is extended source or drain region as explained in Fig.1. Fin width ( $T_{fin}$ ) plays a major role for controlling the short channel effect effectively. Therefore  $T_{fin} \sim L_{gate}/2$  is followed.

In a FinFET structure, an ultra-thin Si fin forms a conducting channel wherein the electrons flow from source to drain. This conducting channel is wrapped by gate where the input voltages are supplied. Hence controlling the flow of electrons even in off state preventing the leakage of current. Sometimes there is an increase in the amount of charge carriers and the rate at which it flows, resulting in the breakdown of the conducting channel formed by single fin. This blocks the flow of electrons from source to drain which ceases the current flow. The number of fins is increased in multi-gate field-effect transistors (MuGFET) which are constructed parallel to each other improving short channel effect. As the number of fins increases, the amount of charge carriers flowing from higher potential to lower potential also increases. Therefore, the rate at which the carriers flow is faster increasing the switching speed. The main advantage of multiple fins is better gate control over the conducting channel. Due to this, there is a reduction in current leakage. This attains high onstate drive current. FinFETs have various logic design styles designing of different FinFETs; one circuit can be configured in one of the subsequent modes:

- **Shorted-gate (SG) mode**, in this mode both gate are shorted and we get improved drive strength and have better control over the channel length
- **Independent-gate (IG) mode**, in which independent signals drive the two device gates, this may reduce the number of transistors in the circuit.
- **Low-power (LP) mode**, in which we are applying a low voltage to n-type FinFET and high voltage to p-type FinFET. This varies the threshold voltage of the devices which reduces the leakage power dissipation at the cost of increased delay.
- **Hybrid IG/LP-mode** is a combination of LP and IG modes.

### III. Logic Style

Logic style of a circuit influences its speed, power dissipation, size and wiring complexity. The circuit delay depends upon the number of transistors in series, transistor sizes and wiring capacitances. Robustness with respect to voltage and transistor scaling as well as varying process, working conditions and compatibility with surrounding circuitries are important aspects influenced by implemented logic style.

#### 1.) Complementary MOS Logic Style (CMOS)

Complementary MOS logic style is a combination of two networks; the Pull up Network (PUN) and the Pull down Network (PDN). The Pull up Network consists of PMOS transistors and Pull down Network consists of NMOS devices. The function of Pull up Network is to provide connection between gate output and  $V_{dd}$ , anytime the output of the gate is meant to be high. Similarly, function of Pull down Network is to provide connection between gate output and GND anytime the output of the gate is meant to be low. The Pull up

Network and Pull down Network are mutually exclusive to each other. The noise margin and propagation delay depends on the input patterns.

**2.) Transmission Gate(TG)**

It consists of n-channel transistor as well as p-channel transistor with separate gate connections and common source and drain connections. The control signal is applied to gate of n-channel transistor and its complement is applied to the gate of p-channel transistor. By combining the characteristics of p-channel transistor as well as n-channel transistor, it is able to pass logic ‘1’ and logic ‘0’ efficiently without any distortion.

**IV. Full Adder Circuit Design**

Addition is the most basic arithmetic operation and usually used in any digital electronic devices and arithmetic logic unit (ALU) to add any value of numbers. The commonly used adder cell is full adder where three inputs i.e. A, B and C<sub>IN</sub> will be added together to calculate the output of Sum and C<sub>OUT</sub>. The expression for Sum and C<sub>OUT</sub> is given by:

$$Sum = A \oplus B \oplus Cin$$

$$C_{out} = A \cdot B + Cin \cdot (A \oplus B)$$

Where above Equations are generated from the truth table of 1-bit full adder as shown in Table 1

**Table 1: Truth Table of 1-bit full adder**

INPUTS			OUTPUTS	
A	B	C	SUM	COUT
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

**1.) 1-Bit Complementary MOS (CMOS) Full Adder**

The CMOS full adder has 28 transistors in the design and it is the simplest implementation based on above equations. The circuit of CMOS 1-bit full adder is as shown in Fig2. This design has its advantages and disadvantages. The advantages include high noise margin is very reliable to low voltage. However, high number of transistors may results in large power consumption, high input loads and requires larger Silicon area in a wafer. It also stated that this design may introduces more delay because Sum is generated from Cout as input as can be observed from Fig.2.

**2.) 1-Bit Transmission Gate (TG) Full Adder:**

Transmission gates full adder consists of 20 transistors which made up of transmission gates, PMOS and NMOS transistors as illustrated in Fig.3. Transmission gates are used in the design because it has high speed operation and low power dissipation. The TG full adder circuit is simpler than CMOS with balanced generation of Sum and Cout output signals besides less transistor count, less intermediate nodes and lower input loading. In contrast, compared to CMOS full adder, TG full adder has higher power dissipation. It is also said that if TG full adder is cascaded in series, the propagation delay also may increases excessively.

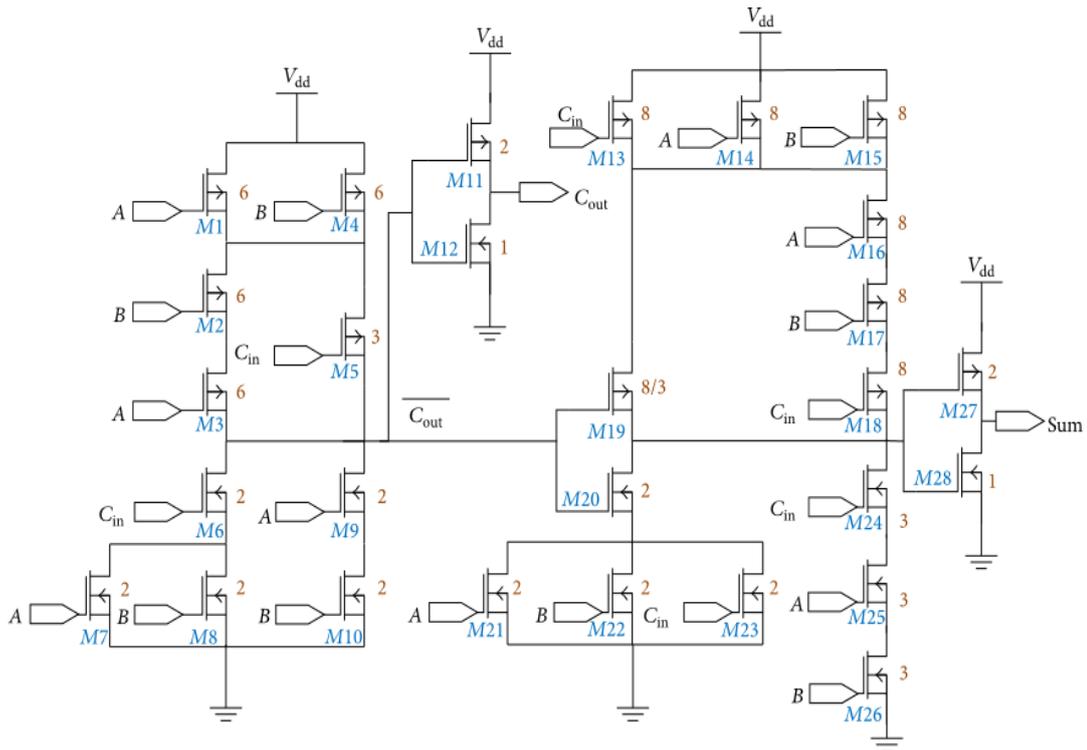


Fig.2: 1-Bit CMOS Full Adder [3]

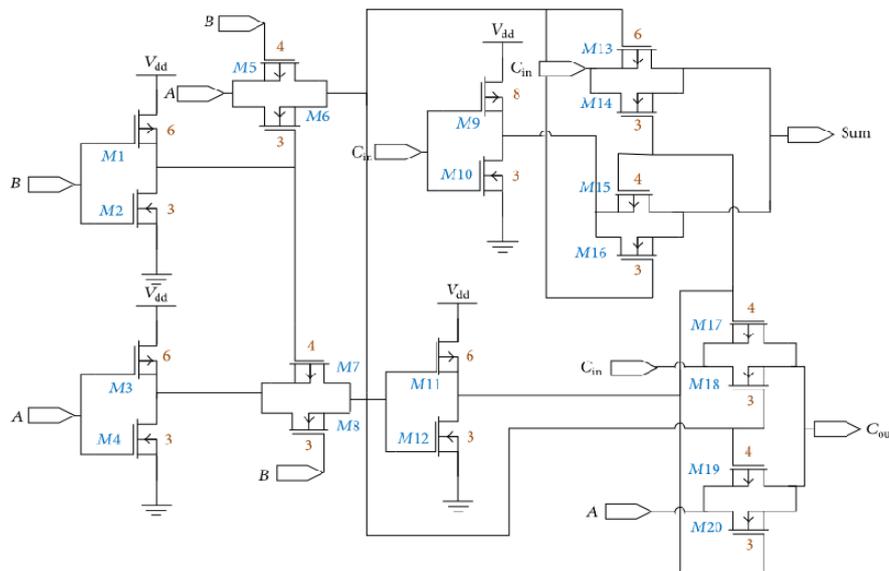


Fig.3: 1-Bit TG Full Adder [3]

**V. Parameters Used In Experimentation**

In this section, parameters used in experimentation are presented. The FinFET based 1-bit Full Adder circuits in different logic styles have been simulated using HSPICE tool. The technology generation that is used to realize the circuits' are 10nm, 20nm and 32nm. The models used for simulation are derived from the PTM website. The parameters of the devices that are used in FinFET based full Adder for simulation in 10nm; 20nm and 32nm are shown in Table-2 and Table-3. These parameters were extracted from ITRS and IEEE Papers.

**Table 2: Parameters used in experimentation of Full Adder Circuit in 32nm**

Parameters	Value
Technology node	32nm
Supply Voltage(Vdd)	.7v
Capacitance	14.5332f
Threshold Voltage of front and back gate NMOS	0.29v

Threshold Voltage of front and back gate PMOS	-0.25v
Width and length of NMOS	wdg=80n ldg=32n
Width and length of PMOS	wdg=1u ldg=32n

**Table 3: Parameters used in experimentation of Full Adder Circuit in 20nm and 10nm**

Parameters	Value	
	20nm	10nm
Technology node	20nm	10nm
Supply Voltage(Vdd)	.7v	.7v
Capacitance	14.5332f	14.5332f
Fin Width(T <sub>FIN</sub> )	15n	9n
Fin Length(L <sub>g</sub> )	24n	14n
Fin Height(H <sub>FIN</sub> )	28n	21n
Number of Fin(N <sub>FIN</sub> )	1	1

## VI. Experimentation And Results

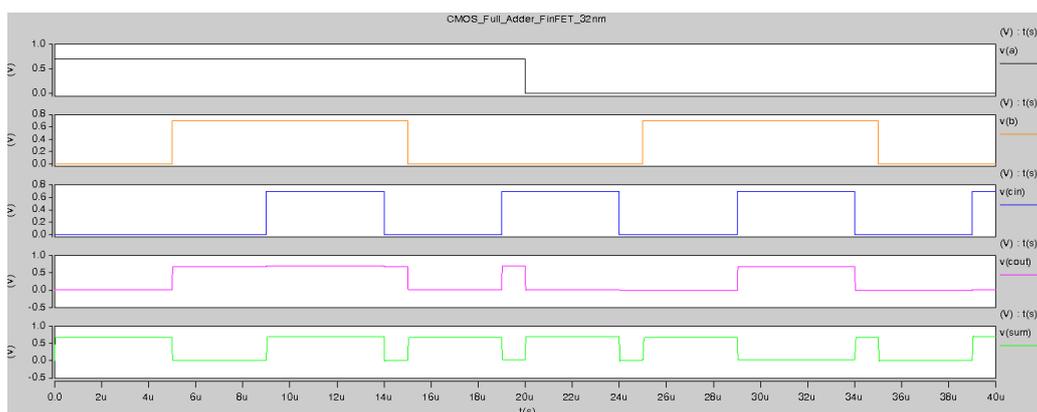
The performance metrics of the full Adder measured are power, delay and energy. The simulation analysis is done over HSPICE and waveforms are observed on CosmosScope. The simulation analysis is carried out with three inputs (A, B, C) and two outputs (Sum and Carry) of full Adder. The simulation waveform of power, delay and energy of FinFET based circuits is discussed.

### 1. Performance Analysis of 1-bit Full Adder at 32nm technology node using CMOS and TG logic styles:

The experimentation done under the parameter of VDD = .7v. The threshold voltage of front and back gate for nmos is 0.29v and 0.29v respectively and threshold voltage of front and back gate for pmos is -0.25v and -0.25v respectively for 32nm. The width and length of nmos is wdg=80n ldg=32n and for pmos are wdg=1u ldg=32n respectively. Table 4 shows performance parameter of FinFET based 1-bit CMOS and TG Full adder at 32nm. Fig.4 and Fig.5 shows Input and Output signal of FINEFET based 1-bit CMOS and TG Full-Adder Circuit at 32nm respectively. Similar waveforms were obtained for 20nm and 10nm technology nodes.

**Table 4: Performance parameter of FinFET based 1-bit CMOS and TG Full adder at 32nm**

Parameter	CMOS	TG
Average Power(watts)	$3.2759 \times 10^{-7}$	$3.8245 \times 10^{-7}$
Delay(sec)	$4.0000 \times 10^{-6}$	$3.2000 \times 10^{-6}$
Energy(joule)	$6.5525 \times 10^{-12}$	$5.8212 \times 10^{-12}$
Leakage Power(watts)	$6.5525 \times 10^{-4}$	$5.8212 \times 10^{-4}$
Leakage Current(amp)	$9.3608 \times 10^{-4}$	$8.3160 \times 10^{-4}$
EDP(joule)	$2.6535 \times 10^{-17}$	$3.4420 \times 10^{-12}$
PDP(joule)	$2.9483 \times 10^{-12}$	$3.9780 \times 10^{-17}$



**Fig.4: Input and Output signal of FinFET based 1-bit CMOS Full-Adder Circuit at 32nm**

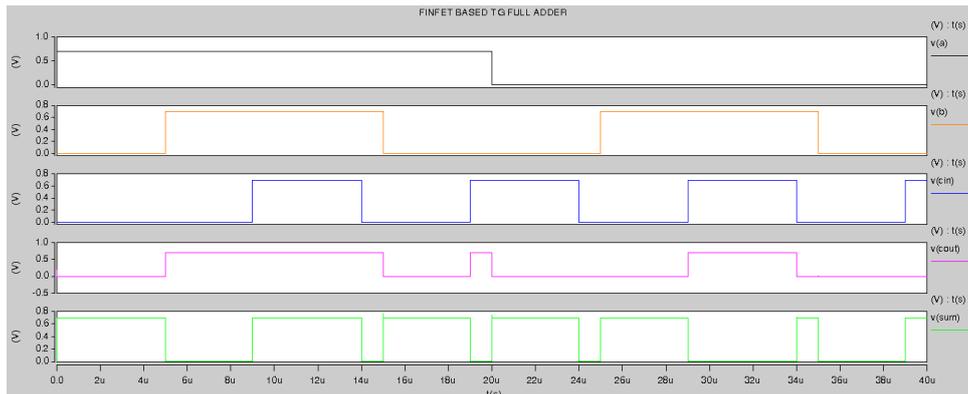


Fig.5: Input and Output signal of FINFET based 1-bit TG Full-Adder Circuit at 32nm

### 2. Performance of 1-bit Full Adder at 20nm technology node using CMOS and TG logic styles

The experimentation done under the parameter of VDD = .7v. Nodes in the model target Ioff=0.1 nA/um where effective width (Weff) =2\*fin\_height+fin\_width. \* vdd. Height of the Fin (HFIN) is 28nm, thickness of the Fin (TFIN) is 15nm and Gate Length (lg) is 24n. Table5 shows performance parameter of FinFET based 1-bit CMOS and TG Full adder at 20nm.

Table 5: Performance parameter of FinFET based 1-bit CMOS and TG Full adder at 20nm

Parameter	CMOS	TG
Average Power(watts)	$6.7950 \times 10^{-8}$	$1.2566 \times 10^{-7}$
Delay(sec)	$1.4983 \times 10^{-7}$	$1.4112 \times 10^{-7}$
Energy(joule)	$1.3591 \times 10^{-12}$	$1.6920 \times 10^{-12}$
Leakage Power(watts)	$1.3591 \times 10^{-4}$	$1.6920 \times 10^{-4}$
Leakage Current(amp)	$1.9416 \times 10^{-4}$	$2.4172 \times 10^{-4}$
EDP(joule)	$1.5253 \times 10^{-17}$	$1.8838 \times 10^{-12}$
PDP(joule)	$2.824 \times 10^{-12}$	$2.824 \times 10^{-17}$

### 3. Performance of 1-bit Full Adder at 10nm technology node using CMOS and TG logic styles:

The experimentation done under the parameter of VDD = .7v. Nodes in the model target Ioff=0.1 nA/um where effective width (Weff) =2\*fin\_height+fin\_width. \* vdd. Height of the Fin (HFIN) is 21nm, thickness of the Fin (TFIN) is 9nm and Gate Length (lg) is 14n. Table6 shows performance parameter of FinFET based 1-bit CMOS and TG Full adder at 10nm.

Table 6: Performance parameter of FinFET based 1-bit CMOS and TG Full adder at 10nm

Parameter	CMOS	TG
Average Power(watts)	$1.1085 \times 10^{-9}$	$1.5395 \times 10^{-9}$
Delay(sec)	$1.4972 \times 10^{-8}$	$1.4983 \times 10^{-8}$
Energy(joule)	$7.2275 \times 10^{-15}$	$1.2772 \times 10^{-14}$
Leakage Power(watts)	$7.2275 \times 10^{-7}$	$1.2772 \times 10^{-6}$
Leakage Current(amp)	$1.0325 \times 10^{-6}$	$1.8246 \times 10^{-6}$
EDP(joule)	$2.4580 \times 10^{-19}$	$2.3067 \times 10^{-14}$
PDP(joule)	$1.6597 \times 10^{-14}$	$3.4561 \times 10^{-19}$

## VII. Comparison Analysis Of Performance Metric

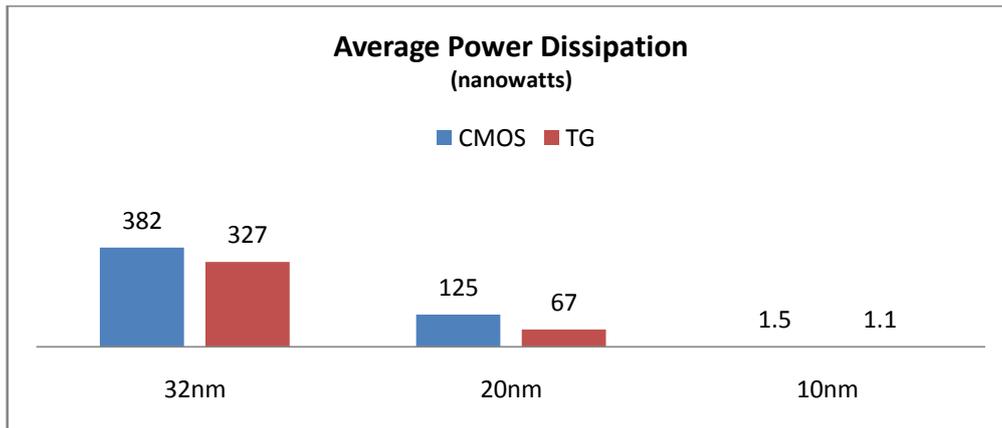
In this section, performance of average power dissipation, delay, leakage power, power delay product and energy delay product metric is analyzed. This metric is measured in CMOS and TG based 1-bit full adder for 10nm, 20nm and 32nm technology node. Each of the cell designs is implemented to determine the optimal tradeoff between delay-energy-power in 10nm, 20nm and 32nm in modern digital systems.

### 1. Comparative Analysis of Average Power Dissipation

The average Power in CMOS and TG Full Adder at 10nm, 20nm and 32nm is tabulated in Table8 and the graph is plotted in Fig.6.

Table 8: Comparative Analysis of Average Power of CMOS and TG Full Adder at 10nm, 20nm and 32nm

Full Adder Circuit	Technology Node		
	32nm	20nm	10nm
CMOS	$3.2759 \times 10^{-7}$	$6.7950 \times 10^{-8}$	$1.1085 \times 10^{-9}$
TG	$3.8245 \times 10^{-7}$	$1.2566 \times 10^{-7}$	$1.5395 \times 10^{-9}$



**Fig.6: Comparative Analysis of Average Power of CMOS and TG Full Adder at 10nm, 20nm and 32nm**

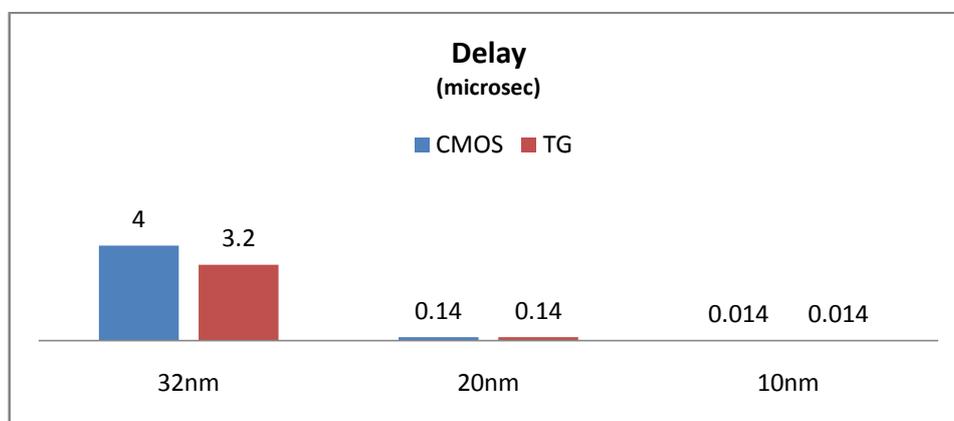
The TG Full Adder provides 14.3% reduced power dissipation in comparison with CMOS full adder for 32nm. The TG Full Adder provides 46.4% reduced power dissipation in comparison with CMOS full adder for 20nm. The TG Full Adder provides 26.6% reduced power dissipation in comparison with CMOS full adder for 10nm. Hence, The TG Full Adder gives reduced power dissipation in among all cell designs of full-adder. The average power dissipation for 10nm reduced greatly compared to 20nm and 32nm, which can be seen in Fig.6.

**2. Comparative Analysis of Delay**

The delay in CMOS and TG Full Adder at 10nm, 20nm and 32nm is tabulated in Table9 and the graph is plotted in Fig.7.

**Table 9: Comparative Analysis of Delay of CMOS and TG Full Adder at 10nm, 20nm and 32nm**

Full Adder Circuit	Technology Node		
	32nm	20nm	10nm
CMOS	$4.0000 \times 10^{-6}$	$1.4983 \times 10^{-7}$	$1.4972 \times 10^{-8}$
TG	$3.2000 \times 10^{-6}$	$1.4112 \times 10^{-7}$	$1.4983 \times 10^{-8}$



**Fig.7: Comparative Analysis of Delay of CMOS and TG Full Adder at 10nm, 20nm and 32nm**

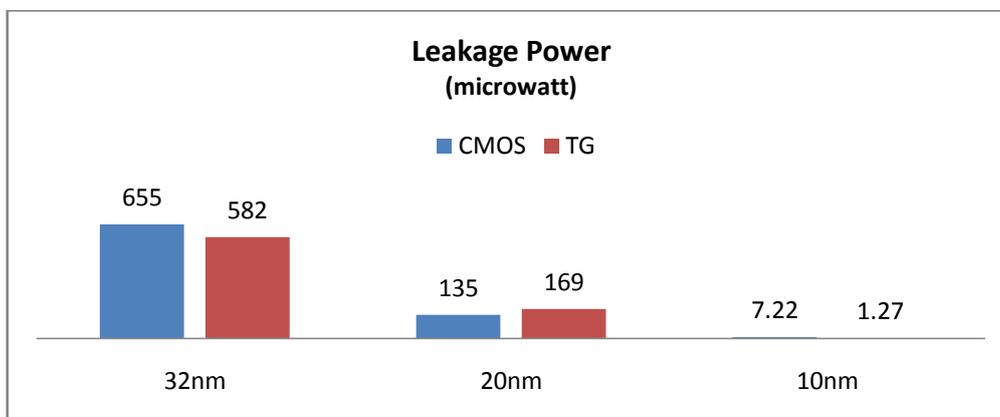
The TG Full Adder provides 25% delay in comparison with CMOS full adder for 32nm. The TG Full Adder provides 33.3% approximately equal delay with CMOS full adder for 20nm. The TG Full Adder provides 41.6% approximately equal delay with CMOS full adder for 10nm. Hence, The TG Full Adder gives reduced delay in among all cell designs of full-adder. The delay for 10nm reduced greatly compared to 20nm and 32nm, which can be seen in Fig.7.

**3. Comparative Analysis of Leakage Power**

The leakage power in CMOS and TG Full Adder at 10nm, 20nm and 32nm is tabulated in Table10 and the graph is plotted in Fig.8.

**Table 8: Comparative Analysis of Leakage Power of CMOS and TG Full Adder at 10nm, 20nm and 32nm**

Full Adder Circuit	Technology Node		
	32nm	20nm	10nm
CMOS	$6.5525 \times 10^{-4}$	$1.3591 \times 10^{-4}$	$7.2275 \times 10^{-6}$
TG	$5.8212 \times 10^{-4}$	$1.6920 \times 10^{-4}$	$1.2772 \times 10^{-6}$



**Fig.8: Comparative Analysis of Delay of CMOS and TG Full Adder at 10nm, 20nm and 32nm**

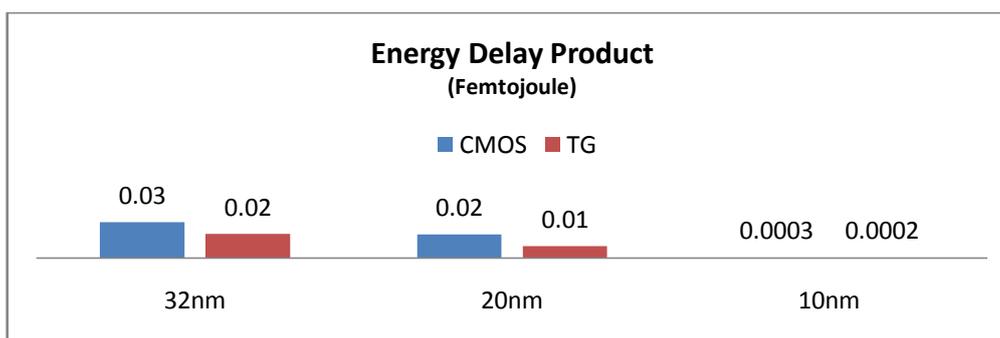
The TG Full Adder provides 11.1% reduced leakage power in comparison with CMOS full for 32nm. The CMOS Full Adder provides 47.4% reduced leakage power TG full adder respectively for 20nm. The TG Full Adder provides 82.4% reduced leakage power in comparison with CMOS full 10nm. Hence, The TG Full Adder gives reduced leakage power from CMOS cell design of full-adder at 10nm and 32nm technology mode but CMOS full adder gives lesser leakage power in 20nm technology node. The leakage power for 10nm reduced greatly compared to 20nm and 32nm, which can be seen in Fig.8.

**4. Comparative Analysis of Energy Delay Product**

The EDP in CMOS and TG Full Adder at 10nm, 20nm and 32nm is tabulated in Table11 and the graph is plotted in Fig.9.

**Table 11: Comparative Analysis of Energy Delay Product of CMO and TG Full Adder at 10nm, 20nm and 32nm**

Full Adder Circuit	Technology Node		
	32nm	20nm	10nm
CMOS	$3.0978 \times 10^{-17}$	$2.824 \times 10^{-17}$	$3.4561 \times 10^{-19}$
TG	$2.6535 \times 10^{-17}$	$1.5253 \times 10^{-17}$	$2.4580 \times 10^{-19}$



**Fig.9: Comparative Analysis of Energy Delay Product of CMOS and TG Full Adder at 10nm, 20nm and 32nm**

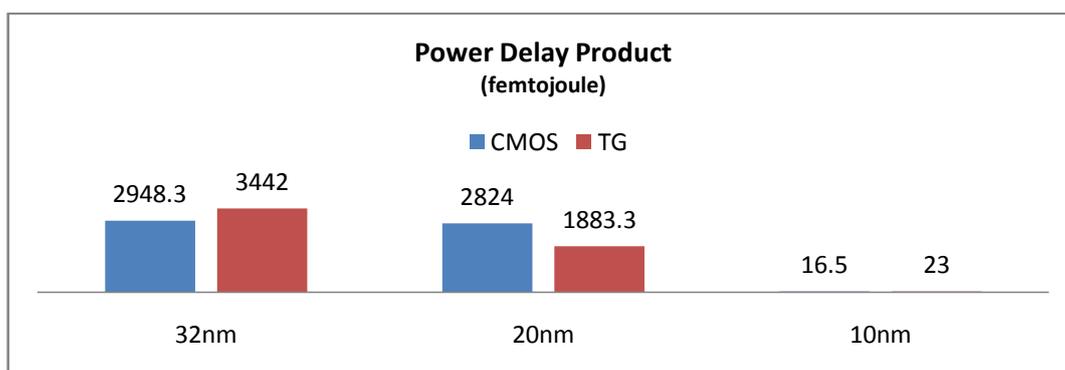
The TG Full Adder provides 33.3% reduced EDP in comparison with CMOS full for 32nm. The TG Full Adder provides 50% reduced EDP from CMOS full adder for 20nm. The TG Full Adder provides 33.3% in comparison with CMOS full adder for 10nm. Hence, The TG Full Adder gives reduced EDP in among all cell designs of full-adder at 10nm, 20nm and 32nm. The EDP for 10nm reduced greatly compared to 20nm and 32nm, which can be seen in Fig.9.

### 5. Comparative Analysis of Power Delay Product

The PDP in CMOS and TG Full Adder at 10nm, 20nm and 32nm is tabulated in Table12 and the graph is plotted in Fig.10.

**Table 12: Comparative Analysis of Power Delay Product of Full CMOS and TG Full Adder at 10nm, 20nm and 32nm**

Full Adder Circuit	Technology Node		
	32nm	20nm	10nm
CMOS	$2.9483 \times 10^{-12}$	$2.824 \times 10^{-12}$	$1.6597 \times 10^{-14}$
TG	$3.4420 \times 10^{-12}$	$1.8838 \times 10^{-12}$	$2.3067 \times 10^{-14}$



**Fig.10: Comparative Analysis of Power Delay Product of CMOS and TG Full Adder at 10nm, 20nm and 32nm**

The CMOS Full Adder provides 14.3% reduce PDP in comparison TG full adder respectively for 32nm. The TG Full Adder provides 33.2% reduced PDP from CMOS full adder for 20nm. The CMOS Full Adder provides 58.8% reduced leakage power in comparison with TG full adder for 10nm. Hence, The TG Full Adder gives reduced EDP in among all cell designs of full-adder at 10nm, 20nm and 32nm. The EDP for 10nm reduced greatly compared to 20nm and 32nm, which can be seen in Fig.10.

### VIII. Conclusion And Future Work

This paper investigated the cell design is also major factor which contributes in good performance of digital circuits. So, it was verified that the 1-bit Transmission gate (TG) FinFET based full adder performed very well with a reduced amount of PDP and EDP compared to other cell design because of its high-speed performance and full swing operation in 10nm technology node. Based on the findings, the 1-bit FinFET-based full adder at 10nm technology node was shown to be the lowest and optimal tradeoff in all metric performances. It is recommended that the future work of this research should include the complete arithmetic logic unit (ALU) design. Besides that, the performance and potential of other logic style such as Static Energy-Recovery full adder (SERF) and Hybrid CMOS (HC) Full Adder should be explored in future work.

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