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Optimization of Floor-Planning Using Genetic Algorithm and Hybrid Partitioning Algorithm

B.Mahalakshmi[1], CH.Sumalatha[2], G.Divya[3,]G.Emilygrace[4]
[1,2,3] *Bapatla Women's Engineering College,Bapatla,A.P,India*
[4] *Vrs&Yrn College Of Engineering And Technology,Chirala,A.P,India*

Abstract: *Floor-planning is one of the key design flow of VLSI chip designing process.Area miniaturization is the essence of compaction of any application circuit in chip designing. The physical design stages involve virtual design realizations iterated for their efficiency.For this purpose, the CAD algorithms offer avariety of solutions depending on the needs and specifications of the designer. The use of EDA tools help invisualization of the effects of design algorithms on the circuit performance and the dimensions of the floor areaoccupied by the design. It also uses a genetic algorithm (GA) .GA has been implemented and tested on popular benchmark problems. Experimental results show that GA can quickly produce optimal solutions for all tested benchmark problems.The hybrid algorithm on the circuit design is, effect of applying the move based partitioning algorithms KL,FM to circuits and optimizing the cells of the circuit using Hybrid Genetic Algorithm (HGA) is discussed. The results suggest that, this approach on circuits provides scope to unify the stages of physical design stages of partitioning and placement and also optimize the area parameter of a physical design process.*

Keywords:*Floor-planning, CAD algorithms, EDA tools, genetic algorithm(GA), Hybrid Genetic Algorithm(HGA)*

I. Introduction

Floor planning decides how to arrange the modules on a chip under the constraint that no two modulesare overlap while controlling the area, wire length, and other performance indices to be optimal.Partitioning is the first design step towards the production of chip from a design.Floor-plans can be divided into two categories, the slicing structure and the non-slicingstructure. A slicing structure can be represented by a binary tree whose leaves denote modules andinternal nodes specify horizontal or vertical cut lines. For non slicing floor plans, there are differenttechniques such as sequence pair, bounded slicing grid (BSG), O-tree and B* tree.Sequence pairs can be used to floor plan hard rectangular blocks by simulated annealing.Tohandle non-slicing floor-plans, this paper propose an iterative optimized framework which uses GA forlocal search on each iteration and adopts an ordered binary-tree based representation, called B*-trees for the placement of rectangle modules. Inheriting from the particular characteristics of the ordered binarytree, the B*-tree has many advantages compared with other representations. The B*tree is very flexible very fast and easy for implementation. It does not need to construct constraint graphs for area costevaluation.The choice of the design style asfull custom or semicustom ASICs depend on the intended functionality of the chip, time tomarket and the total number of chips to be manufactured.

Table [1]: Chip Area, Performance and Fabrication for different designs

Parameter	Style			
	Full custom	Standard cell	Gate array	FPGA
Area	Compact	Compact to Moderate	moderate	Large
Performance	High	High to moderate	Moderate	Low
Fabricate	All layers	All layers	Routing layers only	No layers

The table[1] above describes the essence of various design style to parameter underconsideration. The Design styles can be seen as to cater to the differing needs of the applicationdevelopment purpose. From the Comparison in table[1], it can also be observed that the fullcustom providescompact layouts for high performancedesigns and FPGA is completelyprefabricated and requires no user specific fabrication steps.The stage of partitioning,though entitles as a separate step; it is validated only through the placement stage. Thisnecessitates the need for unification of these consecutive and distinctly irreversible stages of the physical design.

II. Problem Formulation

In hybrid partioning algorithm, The circuit is visualized as graph. A hypergraph G = (V, E) of the circuit is considered.V = {v1,v2,….,vn} are a set of vertices of the hypergraph and E = {e1, e2,…, em} are a set ofhyperedges. Each vertex represents a component and a hyperedge joining the vertices; wheneverthe component corresponding to these vertices are to be connected. Thus each hyperedge is thesubset of vertex set.In other words, each net is represented by a hyperedge.

The partitioning problem is to partition V into V1, V2, …,Vk where Vi and Vj = e i j. Partitionis also referred to as‘cut’ in the graph. The cost of partitioning is called the cut size, which is the number of hyperedges crossing the cut.Minimization of a cost function, is as shown in eq (1)below C=$\sum_{i=1}^{k}, \sum_{j=1}^{k} I[i,j] i \neq j$……….(1)

Where i, j are the vertices of an edge ,C = cost of cut , I [i,j] = cost of an edge.
As the problem involves bi-partitioning of a circuit, equality condition must be satisfied aseq (2):
$\sum_{i=0}^{k}[mi] \neq \sum_{j=0}^{k}[nj]$…………(2)

Where mi and nj are nodes in the two partitions.This forms the initial input netlist from thecircuit and determines the gain calculation and stopping criterion of the algorithms.The detailedprocedures on various algorithms is studied before choosing move based KL and FMalgorithm.The algorithm pseudocodes for KL and FM are implemented for move basedpartitioning and the hybrid genetic algorithm with mincut procedure is implementedfor optimization .All the codes are implemented in C Language.

Poems Algorithm:POEMS algorithm works in iteration.The aim of the following iterations of the POEMS algorithm is to find the best modification of the prototype with use of the genetic GA, which serves as a modification optimizer. The evolution is started, and a selection, crossover and mutation operators are used ,in order to breed the action sequences. The fitness function of each action sequence is defined as a fitness of the prototype solution after being modified by the particular sequence evaluated. The overall program. A prototype is the initial solution created and improved by the POEMS algorithm. Its creation is a very important step, because the initial position highly influences the space searched
The best-fit heuristic is a general name for a greedy rectangle packing algorithm. The principle is toselect the best fitted module for each hole in the final placement. Both holes and modules are stored in aqueue and the algorithm iterates until the module queue is empty. After each placement of the module,the whole list is updated.

Each action in the POEMS algorithm represents a certain parameterized modification of theprototype. Every action has a Boolean flag that enables or disables the action. If the action is disabled, itdoes nothing to the input tree. Individual actions are joined together to sequences that are optimized bythe GA. This algorithm used six actions- rotate action, flip action, mirror action, exchange value action,exchange node action and hang node action. schema is shown in figure 1.

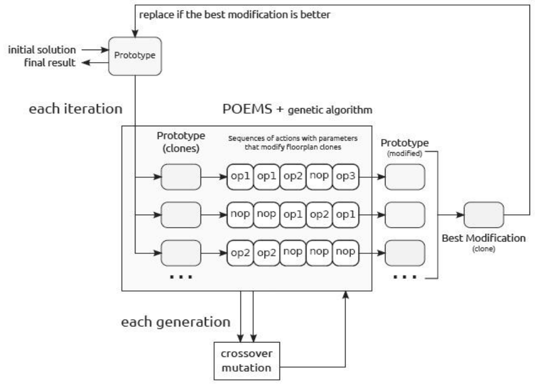


Fig. 1: Overall program schema

Genetic Algorithms (GA): The genetic algorithm is a method for solving both constrained and unconstrained optimizationproblems that is based on natural selection, the process that drives biological evolution. At each step, thegenetic algorithm selects individuals at random from the current population to be parents and uses themto produce the children for the next generation. Over successive generations, the population "evolves"toward an optimal solution. Here each individual in the population of GA represents a sequence ofactions, which, if applied to the prototype floor-plan, creates another floor-plan. The fitness value used is the negative amount of the unused area (TUA) (total area of the enclosingrectangle without the area of placed modules) i.e. q(f) = TUA(f).

Here roulette selection procedure is used to select parent. Roulette selection chooses parents bysimulating a roulette wheel, in which the area of the section of the wheel corresponding to an individual isproportional to the individual's expectation. The algorithm uses a random number to select one of thesections with a probability equal to its area. This paper used three point crossover methods to shuffle the different characteristics of an individual and create children out of parents inheriting the characteristics directly. As in two point crossover method it chooses three points A, B and C at random and based on these three the offspring's are generated. So the characteristics of parents are uniformly distributed among the children

The circuit is converted as a net list and then the algorithms are applied. Initially the nodes arepartitioned using KL algorithm and then mincut algorithm merged with genetic algorithm is used as hybrid genetic algorithm approach to minimize the area parameter of thecircuit at gate level.

The optimization is achevied using the Genetic algorithm approach. Further the GA is infusedwith the mincut algorithm and the Hybrid genetic algorithm performance on the test circuit usingKL and FM algorithms .The mincut algorithm defines thefitness function of the genetic algorithm, thus making it Hybrid Genetic Algorithm[HGA].

III. Experimental Results

The experiment employed MCNC/GSRC benchmarks for the VLSI floor-planning problem. Itcompared with Simulated Annealing (SA) and Differential evolution (DE) algorithms. The resultsobtained in this project are better compared to other techniques. The experimental results are shown inTable 4.1 for Area estimation.

3.1. GSRC benchmark

Two benchmarks (n10, n100) were selected from GSRC and tested. The results are shown in Table4.2. In the table, setup parameters with the resulting used area, unused area statistics and the computationtime are displayed. The test indicates that the longer (in the terms of iterations) is the algorithm executed,the higher quality of the result can be achieved.

Table 4.1: area comparisons

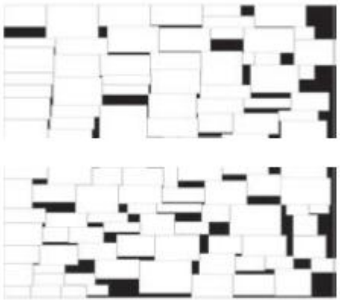
Circuits	No. of Modules	SA Area (mm2)	DE Area (mm2)	GA Area (mm2)
ami33	33	1.36	1.22	1.17
ami49	49	43.34	36.22	35.45
Xerox	10	20.47	19.19	19.35
Hp	9	9.57	9.293	8.83

Table 4.2: The GSRC benchmark results

Test	I	G	N	S	Used area	Unused area
n10	10	10	3	50	0.223	0.017
n10	100	10	3	50	0.223	0.009
n100	10	10	3	50	0.179	0.036
n100	100	10	3	50	0.179	0.025

Table 4.3: MCNC benchmark results

Test	I	G	N	S	Used area (mm^2)	Unused area (mm^2)
Ami33	10	10	3	50	1.16	0.162
Ami33	100	10	3	50	1.16	0.082
Ami49	10	10	3	50	35.44	7.4
Ami49	100	10	3	50	35.44	5.65
Xerox	10	10	3	50	19.35	1.78
Xerox	100	10	3	50	19.35	1.57
Hp	10	10	3	50	8.83	0.883
Hp	100	10	3	50	8.83	0.553



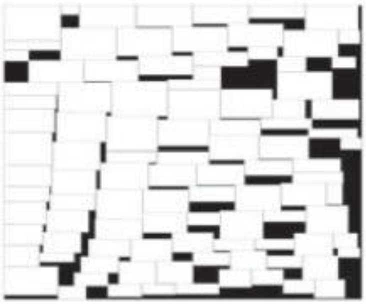
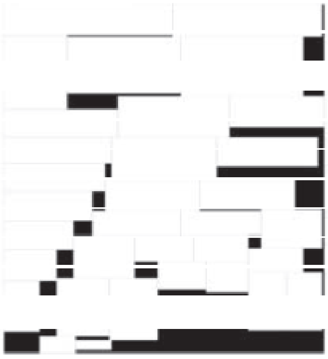


Fig..(a) n100 (17% Dead when I=10)   Fig .(b) n100 (12.4% Dead when I=100)



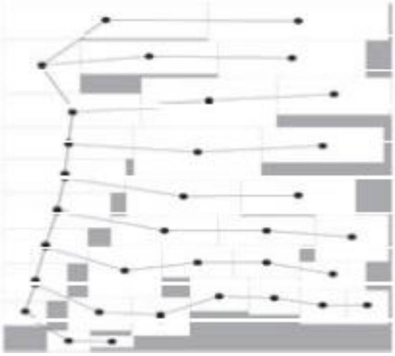
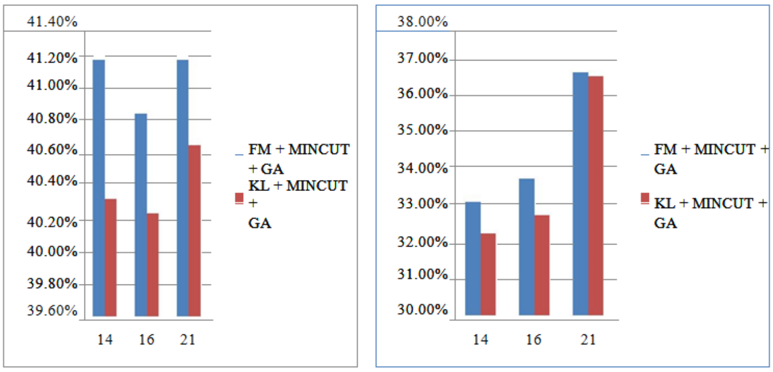


Fig .(c) Ami33(12.3% deadFig .(d) B* tree of the placement

MCNC benchmark: Five benchmarks (ami33, ami49, apte, hp, Xerox) were selected from MCNC and tested. Theresults are shown in Table 4.3. The algorithm performance trend is the same as for GSRC benchmarks.The result of this benchmark also shows that as the number of iteration increases the better optimizationis achieved by decreasing the unused area. In Ami33, 12.3% area is unused when I is 10 and 6.6% area is unused when I is 100. So as iteration increase better optimization is achieved.

The result of mincut algorithm merged with genetic algorithm ie Hybrid genetic algorithm [HGA] is used to extract the optimized area for the given circuitThe graph below showcases the different optimizations obtained for different circuits (C3540,C1908).To evaluate the performance of the algorithm 16 runs were performed on each C3540,C1908 circuits and the result is shown as graph in Fig.



C3540 circuit.C1908 circuit.

Fig :Comparison graph showing percentage area reduction on C3540 ,C1908 circuit.

IV. Conclusion

This paper deals with the combinatorial benchmark circuit implementations at gatelevel, area optimization using evolution based GA approach. The hybrid genetic algorithm[HGA] applied to the partitioning and placed nodes and unifies the two design stages of floorplanning and partitioning. The results suggest thatan overall area optimization to a level of 40%among different sized small and medium circuits of the benchmark. It also emphasizes on theflexibility of choosing the flow of algorithms based on the application and complexity of thecircuits.

The GA algorithm is implemented using the Java programming language and tested on public benchmarkdata available on the website (GSRC , MCNC). The experiments show that the suggested algorithm iscompetitive in quality, and even slightly better than all the other algorithms tested. Therefore a solution for the 2D rectangle packing problem (floor-planning) is designed, implemented and tested. Now furtherdevelopment of the algorithm could include dealing with pre-placed or soft modules, rectilinear modules.Another possibility is to calculate the wire lengthbetween the blocks and optimize it. In that case fitness calculation will be changed.

References

[1]. H. Murata, K. Fujiyoshi, S. Nakatake, and Y.Sajitani,"VLSI module placement based on rectangle-packing by thesequence-pair," IEEE Trans. on Computer Aided Design, vol. 15, pp. 1518-1524, Dec. 1996.

[2]. S.Nakatake, K.Fujiyoshi, H.Murata, and Y.Kajitani," Module Placement on BSG-Sructure and IC layoutApplicaios,"Proc.ICCAD,pp 484- 491,1996.

[3]. P.-N. Guo, C.-K. Cheng, and T. Yoshimura, "An O-Tree Representation of Non- Slicing Floorplan and ItsApplications,"Proc.DAC, pp. 268–273, 1999.

[4]. Y. C. Chang, Y. W. Chang, G. M. Wu, and S. W. Wu,"B*-Trees: A new representation for nonslicingfloorplans," DesignAutomation Conference, pp. 458-463. 2000

[5]. D.E. Goldberg, "Genetic Algorithms in Search, Optimization and Machine learning", Pearson Education, ISBN: 13: 9780201157673, 2004

[6]. M. Tang, and X. Yao, "A Memetic Algorithm for VLSI Floorplanning", IEEE Transactions on Systems, Man, andCybernetics, Part B, vol. 37, pp. 62-69, 2007.

[7]. Christopher J. AugeriHesham H. Ali, "New Graph-Based Algorithms for Partitioning VLSI Circuits", Inproceedings of International symposium on Circuits and systems ,ISCAS, 2004,vol-4, pp:521-524,2004

[8]. B.W. Kerhinghan, S. Lin, "An efficient heuristic procedure for partitioning graphs", Bell System Tech.Journal, Vol. 49, pp. 291 – 307,1970

[9]. David A. Papa and Igor L. Markov,"Hypergraph partitioning and clustering", In Approximation Algorithmsand Metaheuristics,CRC press, ISBN:61-1-61-19,2007.

[10]. NaveedSherwani, "Algorithms for VLSI Physical Design and Automation", third edition, Springer (India)Private Limited, New Delhi, ISBN: 0792383931, 2005

[11]. PinakiMazumder, "Genetic Algorithms for VLSI Design, Layout and Test Automation", Addison-wesley,ISBN 9789814035521, 1999.

[12]. www.cbl.ncsu.edu.benchmarks (for ACM /SIGDA test circuits)

[13]. http://vlsicad.eecs.umich.edu/BK/CompaSS/results/mcnc opt.html

[14]. http://vlsicad.eecs.umich.edu/BK/CompaSS/results/gsrc opt.html