Implementation of LMS Adaptive Filter using Vedic Multiplier

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Abstract: In this paper, we propose LMS (least mean squares) algorithm for the designing an of adaptive traversal filters using two different techniques, a carry save multiplier based architecture and a high speed vedic mathematics based multiplier architecture. Finally comparing the results to evaluate the best design in terms of processing speed. Both of the adaptive filter architectures have been coded in verilog HDL language and synthesized, simulated in Xilinx ISE environment. The main application areas includes unknown system identification for communication processes, Channel Equalization, Noise Cancellation and Echo cancellation like DSP operations.

Keywords: Adaptive Filter, LMS Algorithm, Vedic multiplier, Transversal FIR filter, Carry Slave multiplier.

I. Introduction

Adaptive filters are composed of three basic modules such as filtering structure, performance criterion and adaptive algorithm. The filtering structure determines the output of the filter from given input samples. FIR is preferred over the IIR for filtering due to stability measures. Then, the performance criterion is chosen according to the application and it is used to derive the adaptive algorithm. The three generally used performance criteria are mean squared error, least squares and weighted least squares. Finally, the adaptive algorithm is used to update the filter coefficient based on the performance criterion to improve the performance. An adaptive filter automatically sets its weights with the changing environment by using various adaptive algorithms like LMS and RLS etc. and it is used to evaluate unknown parameters for the system and adaptive estimation of parameters or signals.

II. Adaptive Filter

An adaptive filter takes a signal input of x(n) and gives the output signal as y(n) in the operation of convolution with the weight w(k).



Fig. 2.1 Block diagram of Adaptive filter

At the same time a desired signal/wished signal d(n), is used to calculate the error denoted by e(n). The resulted e(n) error signal is used to automatically adjust the filter weight with the use of an adaptive algorithm. Following are some example algorithms used for adaptive change of weight. These are LMS-Least Mean Square and RLS-Recursive Least Square.

An FIR Transversal filter is chosen as adaptive filter because of its stability. The use of the transversal structure allows relatively straight forward construction of the filter. The output of the filter is compared with the desired response to find the error signal. The error signal is used by the adaptation algorithm to update the adaptive filter coefficient vector according to mean square error performance criterion. In general, the whole adaptation process aims at minimizing some metric of the error signal, forcing the adaptive filter output signal to approximate the reference signal in a statistical sense. There are several adaptation algorithms with different

performance criterion. Due to its low complexity and proven robustness, Least Mean Square (LMS) algorithm is used widely.

III. Transversal Filter

An N-Tap transversal was assumed as the basis for this adaptive filter. The value of N is determined by practical considerations. An FIR filter was chosen because of its stability. The use of the transversal structure allows relatively straight forward construction of the filter.

As the input, filter coefficients and output of the filter are all assumed to be complex valued then the natural choice for the property measurement is the modulus, or instantaneous amplitude. If y(k) is the complex valued filter output, then |y(k)| denotes the amplitude.



Fig. 3.1 Block diagram of Transversal filter

The structure of a transversal FIR filter shown in Fig. 3.1 with N tap weights (adjustable during the adaptation process) with values at time n denoted as:

$$W_0(n), W_1(n), \dots, W_{N-1}(n)$$

The tap weight vector, $\underline{W}(n)$ is represented as:

 $\underline{\mathbf{W}}(n) = [\mathbf{W}_0(n)\mathbf{W}_1(n)\dots\mathbf{W}_{N-1}(n)]\mathbf{T}$

The tap input vector, $\underline{U}(n)$ is represented as:

 $\underline{U}(n) = [U(n) U(n-1)...U(n-N+1)]T$

The FIR Filter output, y(n) can then be expressed as:

$$y(n) = \underline{W}^{T}(n) \ \underline{U}(n) = \sum_{i=0}^{N-1} W_{i}(n) \ U(n-i)$$
(2)

Where T : Transpose n: Time index function N: Order of Filter



(1)

In a transversal filter of length N, as depicted in Fig. 3.2, at each time n the output sample y[n] is computed by a weighted sum of the current and delayed input samples x[n], x[n - 1], ...and the error is being calculated by the adaptive algorithm.

IV. Lms Algorithm

It is a stochastic gradient descent method in that the filter is adapted based on the error at the current time. It was invented in year 1960 by Stanford University professor Bernard Widrow and his first Ph.D. student, Ted Hoff. LMS is linear adaptive filter algorithm and it is consisted of filtering process and adapting process.

FIR filters:

$$\begin{split} y(n) &= w_0(n)x(n) + w_1(n)x(n-1) + \ldots + w_{M-1}(n)x(n-M+1) \quad (3) \\ &= \\ M-1 \\ \sum w_k(n)x(n-k) &= \underline{w}(n)^T \underline{x}(n), n = 0, 1, 2, \ldots, \infty \end{split}$$

k=0

Error between filter output y(t) and a desired signal d(t):

 $e(n) = d(n) - y(n) = d(n) - \underline{w}(n)^{T} \underline{x}(n)$ (5)

Change the filter parameters according to

 $w(n + 1) = w(n) + \mu x(n)e(n)$



(6)

Fig. 4.1 Block diagram of LMS adaptive filter

LMS Algorithm uses a rough gradient approximation, and seeks the wished weight vector This process is used to find the weight vectors for training the ALC (Adaline). The learning rules can be incorporate to the same device that therefore can be auto adapted as there are presented the wished inputs and outputs. The weight vectors values are changed as every combination input-output is processed. This goes on until the ALC gives the correct outputs. This is a truly training process since there is not necessary to clearly calculate the weight vector value.

V. Vedic Multiplier

The Vedic Multiplier is based on a novel technique of digital multiplication which is quite different from the conventional method of multiplication like add and shift Where smaller blocks are used to design the bigger one. The 8 bit number is decomposed into 4 bit and then again the 4 bits are further decomposed into 2 bit numbers. Vedic multiplier is faster among the other conventional multiplier. Speed is improved by parallelizing the generation of partial products with their concurrent summations. Also as the number of bit multiplication increases from 2×2 bits to 8×8 bits the time delay associated with it is greatly reduced as compared to other multipliers. Fig. 5.1 shows the implementation of 8 bit vedic multiplier.

The designing of Vedic Multiplier is based on a novel Urdhava Triyakbhyam technique of digital multiplication which is quite different from the conventional method of multiplication like add and shift. Urdhava Tiryakbhyam literally means Vertical & Crosswise. It main concept of this sutra is that the generation of all partial products can be done with the concurrent addition of these partial products. The algorithm can be implemented for n x n bits.



Fig. 5.1 Flow diagram of implementation of 8 bit vedic multiplier

5.1 Multiplication of two decimal numbers using Vedic multiplier- 325*738

The multiplication of two decimal number is illustrated in Fig.: 5.2 .The digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and all other bits act as carry for the next step. Initially the carry is taken to be zero.



325 x 738 = 239850

Fig. 5.2 Vedic multiplication of two decimal numbers

VI. Simulation Result

The LMS adaptive filter using vedic multiplier is found to be highly efficient in terms of processing speed. For comparison we have verilog coded the carry slave multiplier for the implementation of LMS adaptive filter. Figure 6.1 shows the simulation results of LMS adaptive filter using vedic multiplier and Figure 6.2 shows the simulation results of LMS adaptive filter using carry slave multiplier. The filter structured in Verilog is synthesized on Xilinx ISE.

	4,800 ns	5,000 ns	5,200 ns	5,400 ns	5,600 ns	5,800 ns
📸 yn[15:0]	10	X		50		
📸 xn[7:0]	10	X		50		
Man (15:0)	20	×		70		
mantissa[7:0]				9		
acconent[16:0			10	000		
ll ck	INNANA AAAA	mmmmmm		hhhhhhhhhhh	hannanan	
Note: 12:03 Prod0[15:0]				¢.		
North (15:0]				¢		
aprod2[15:0]				¢.		
prod3[15:0]				0		
aprod4[15:0]	10	x		50		
prod5[15:0]	10	X		50		
prod6[15:0]	10	×		50		
aprod7[15:0]	10	×		50		
product[15:0]	200	×		3500		
product1[15:0				1		
product2[15:0	1800	x		1548		
No. 1210				0		
No. 12111				0		
res3[15:0]				0		
No. 15:0]				0		
N res5[15:0]	10	x		50		
ares6[15:0]	10	x		50		
ares7[15:0]	10	x		50		
ares8[15:0]	10	x		50		
an1[7:0]	10	x		50		
an2[7:0]	10	x		50		
📸 xn3[7:0]	10	x		50		
yk2s[15:0]				0		

Fig. 6.1 Simulation result of LMS adaptive filter using vedic multiplier

DEVICE UTILIZATION SUMMARY (ESTIMATED VALUES) Target Device: xc3e50-5pq208					
Logic Utilization	Used	Available	Utilization		
Number of Slices	253	768	32%		
Number of Slice Flip Flops	176	1536	11%		
Number of 4 input LUTs	445	1536	28%		
Number of Bounded IOBs	41	124	33%		
Number of GCLKs	1	8	12%		

 Table 1.1: Device Utility Summary for 8 bit LMS Adaptive Filter using Vedic Multiplier

	800 ns	1,000 ns	1,200 ns	1,400 ns	1,600 ns	1,800 ns
📷 yn[15:0]	x	XX		100		
📷 xn[7:0]	Z	\frown		10		
an[15:0]	z			20		
📷 mew[7:0]			ZZZ	ZZZZZ		
mantissa[7:0]	z	\frown		5		
exponent[16:0	z	\frown		100		
🗓 clk						
Prod0[15:0]				0		
aprod1[15:0]				0		
aprod2[15:0]				0		
aprod3[15:0]				0		
Prod4[15:0]	x	XX		100		
Prod5[15:0]	x	XX		100		
prod6[15:0]	x	XX		100		
Prod7[15:0]	x	XX		100		
product[15:0]	x	×		200		
Product1[15:0	0	x X		10		
product2[15:0	x	X		1000		
Pres1[15:0]				0		
📷 res2[15:0]				0		
ares3[15:0]				0		
ares4[15:0]				0		
Page res5[15:0]	x	XX		100		
Page res6[15:0]	x	XX		100		
ires7[15:0]	x	XX		100		
Pres8[15:0]	x	XX		100		
📷 xn1[7:0]	z	\subset		10		
📷 xn2[7:0]	Z	\subset		10		
an3[7:0]	z	<		10		
M	×			0		

Fig. 6.2 Simulation result of LMS adaptive filter using vedic multiplier

DEVICE UTILIZATION SUMMARY (ESTIMATED VALUES) Target Device: xc3e50-5pq208					
Logic Utilization	Used	Available	Utilization		
Number of Slices	255	768	33%		
Number of Slice Flip Flops	32	1536	2%		
Number of 4 input LUTs	454	1536	29%		
Number of Bounded IOBs	41	124	33%		
Number of GCLKs	1	8	12%		

 Table 1.2: Device Utility Summary for 8 bit LMS Adaptive Filter using Carry Slave Multiplier

VII. Conclusion

The LMS Adaptive filter is being highly adaptive with the changing environment and is capable of providing the best result in the estimation of the time varying parameter. Also the Vedic multiplier which is based on an algorithm Urdhava Tiryakbhyam of ancient Indian Vedic Mathematics provides the best result in terms of speed. Among Adaptive Least Mean Square FIR using Vedic multiplier and Adaptive Least Mean Square FIR using Carry slave multiplier the performance of LMS Adaptive filter using Vedic multiplier was found more satisfactory in terms of processing speed. The Filter is coded using Verilog HDL and further it is Synthesized using the tool Xilinx9.1i. The presented Adaptive Least Mean Square FIR filters, and may be utilized in various communicational techniques and DSP processes such as Signal Channel Equalization, Noise-Cancellation, Echo-cancellation and unknown System identification for adaptive and changing environment.

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