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IC Layout Design of 4-bit Magnitude Comparator using Electric VLSI Design System

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Abstract: *There is need to develop various new design techniques in order to fulfil the demand of increased speed, reduced area for compactness and reduced power consumption. It is considered that improved other performance specifications such as less delay, high noise immunity and suitable ambient temperature conditions are the prime factors. In this paper two different techniques are used for designing a 4-bit Magnitude Comparator(MC) and then a comparison is made about area and average delay. First one is Transmission Gate (TG) technique and second one is GDI Technique. This paper describes the design of an Integrated Circuit (IC) layout for a 4-bit MC. The layout was designed by use of an open source software namely Electric VLSI Design System which is Electronic Design Automation (EDA) tool. LTspiceXVII is used as simulator to carry out the simulation work.*

Keywords: *TG, GDI, Comparator, VLSI, CMOS, DRC, LVS, ERC, MC.*

I. Introduction

(a) TG Technique

Transmission gate logic circuit is a special kind of pass-transistor logic circuit. It is built by connecting a PMOS transistor and an NMOS transistor in parallel, which are controlled by complementary control signals. Both the PMOS and NMOS transistors will provide the path to the input logic "1" or "0", respectively when they are turned on simultaneously. Thus, there is no voltage drop problem whether the "1" or "0" is passed through it [1].

(b) GDI Technique

GDI cell contains three inputs – G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS). Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with CMOS inverter. It must be remarked, that not all the functions are possible in standard P-Well CMOS process, but can be successfully implemented in Twin-Well CMOS or SOI technologies. GDI

Technique allows improvements in design complexity level, transistor counts, static power dissipation and logic level swing. Fig.1 represents the basic building block of GDI cell. In this cell Boolean expression of Z is $\bar{A}.B + A.C$. On the basis of this expression, any logic can be implemented by GDI cells. Implementation Detail of gates has described in table.2.

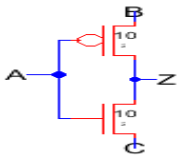


Fig.1 basic building block of GDI cell

(c) Magnitude Comparator (MC)

Magnitude comparator is a combinational logic design which is used to compare the magnitude of two binary data (supposed A & B) and determines if the numbers are equal, or if one number is greater than or less than the other number. It has three outputs G, E and L. when A>B then only G will remains in enable mode. When A=B then only E will remains in enable mode. When A<B then only L will remains in enable mode. The magnitude comparator is one of the fundamental arithmetic components of digital system with many applications such as Digital Signal Processors for data processing, encryption devices and microprocessor for decoding instruction.

(d) Electric VLSI Design System

Electric VLSI Design System is a powerful open source full custom IC Design Electronic Design Automation (EDA) tool. In this EDA tool, verification of IC Design layout involves mainly three processes. These are DRC (Design Rule Check), LVS (Layout Versus Schematic) and ERC (Electrical Rule Check).

Design Rule Check (DRC): DRC is the first most powerful physical verification process to check IC design Layout. DRC will not only check the designs that are created by the designers, but also the design placed within the context in which it is going to be used. Therefore, the possibility of errors in the design will be greatly reduced and a high overall yield and reliability of design will be achieved.

Layout Versus Schematic (LVS): LVS is the second and most powerful physical design verification process in which layout is matched with its equivalent schematic design. In LVS schematic is assumed as a reference and layout is checked against it. In this process, the electrical connectivity of all signals, including the input, output and power signals to their corresponding schematic are checked.

Besides that, the sizes of the device will also be checked including the width and length of transistors, sizes of resistors and capacitors[2].

Electrical Rule Check (ERC): ERC is third and optional physical design verification process to check the layout. This is used to check the error in connectivity of device. ERC is specially used to check for any unconnected, partly connected or redundant devices. Also, it will check for any disabled transistors, floating nodes and short circuits.

(e) LTspiceXVII simulation software

LTspiceXVII is the simulation software which we have used in this project. It is a high performance SPICE simulator that provides a schematic capture and waveform viewer. It is used to simulate the outputs of both schematic circuit and layout during DRC and LVS.

II. Design Methodology

There are different technologies to construct integrated circuits such as bipolar integrated technology, CMOS technology, NMOS pass transistor logic, Transmission Gate(TG) technology and gate diffusion input(GDI) technology. In this paper we have used two technologies to design 4-bit MC and comparison is made against these technologies. The main reason of using GDI technique is due to its low propagation delay, low power consumption and low chip area.

There are basic design rules which are to be used in order to design an IC layout successfully. These rules are called layout design rule. The layout rule which is to be followed in Electric VLSI Design System has a universal parameter λ in which rule described. Table.1 gives the clarification about layout design rule.

Table.1 fundamental of layout design rule [3]

WELL	
minimum well size	12λ
minimum well spacing between same potential	6λ
minimum well spacing between different potential	0λ
minimum well are	$144\lambda^2$
POLYSILICON1	
minimum polysilicon1 width	2λ
minimum polysilicon1 spacing	3λ
minimum spacing between polysilicon1 to metal	N/A
minimum polysilicon1 area	$4\lambda^2$
POLYSILICON2	
minimum polysilicon2 width	2λ
minimum polysilicon2 spacing	3λ
minimum spacing between polysilicon1 to metal	N/A
minimum polysilicon2 area	$4\lambda^2$
METAL 1,2,3,4,5	
minimum metal width	3λ
minimum spacing between same metal	3λ
minimum spacing between different metals	N/A
minimum metal area	$9\lambda^2$
METAL 6	
minimum metal 6 width	5λ
minimum metal 6 spacing	5λ
minimum spacing between metal 6 to other metals	N/A

minimum metal 6 area	$25\lambda^2$
VIA 1,2,3,4	
minimum via width	2λ
minimum via area	$4\lambda^2$
VIA 5	
minimum via 5 width	3λ
minimum via 5 area	$9\lambda^2$

In our design the basic building blocks are inverter, [2,3,4,5-input AND gate], 5-input OR gate and 2-input XOR gate. So implement our design we need to develop basic buildings block used in project. Fig.2, fig.3 and fig.4 are the basic building blocks of our design. They are 5-input AND gate, 5-input OR gate and 2-input XNOR gate respectively.

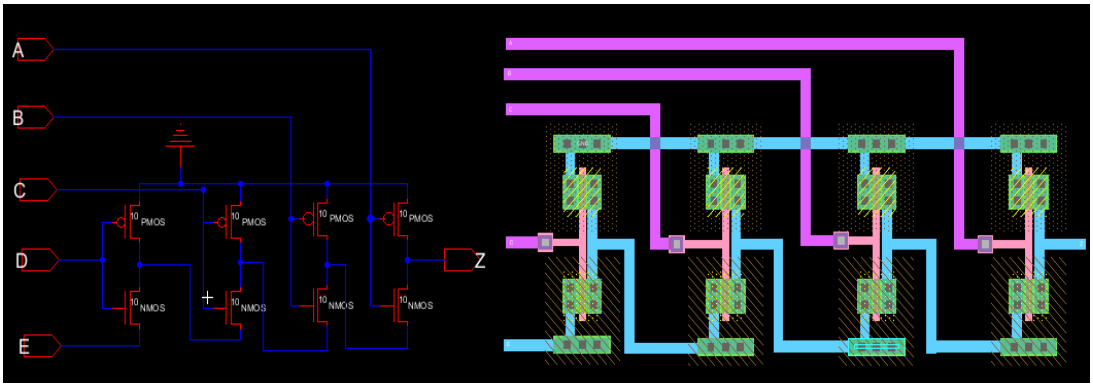


Fig.2 schematic and layout of 5-input AND gate (GDI tech)

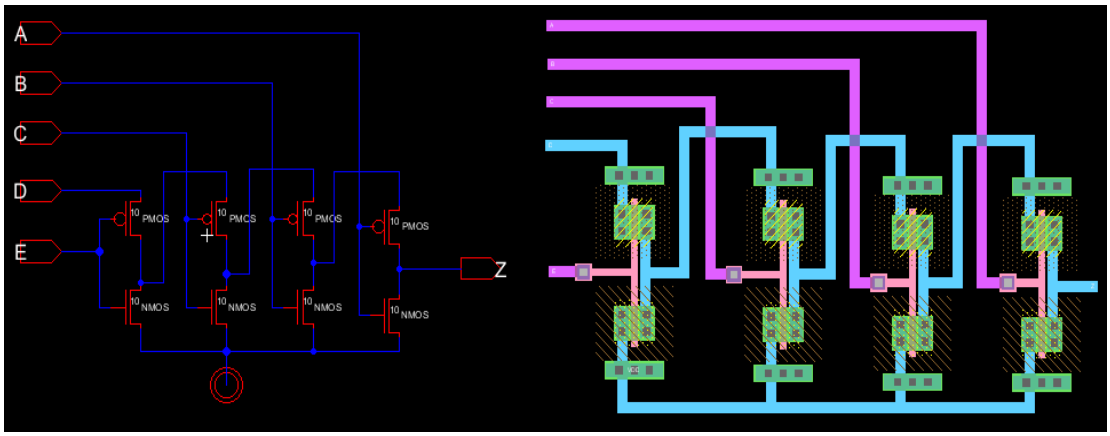


Fig.3 schematic and layout of 5-input OR gate (GDI tech)

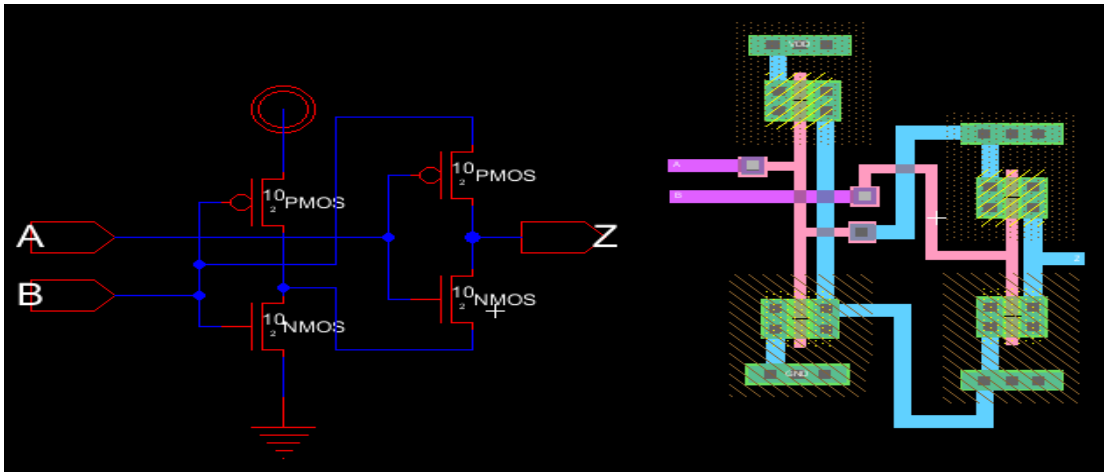


Fig.4 schematic and layout of 2-input XNOR gate (GDI tech)

Boolean equation of our design is

$Go = A3.\overline{B3} + (A3 \copyright B3).A2.\overline{B2} + (A3 \copyright B3).(A2 \copyright B2).A1.\overline{B1} + (A3 \copyright B3).(A2 \copyright B2).(A1 \copyright B1).A0.\overline{B0} + (A3 \copyright B3).(A2 \copyright B2).(A1 \copyright B1).(A0 \copyright B0).\overline{Ei}.\overline{Li}$

$Eo = (A3 \copyright B3).(A2 \copyright B2).(A1 \copyright B1).(A0 \copyright B0).Ei$

$Lo = \overline{A3}.B3 + (A3 \copyright B3).\overline{A2}.B2 + (A3 \copyright B3).(A2 \copyright B2).\overline{A1}.B1 + (A3 \copyright B3).(A2 \copyright B2).(A1 \copyright B1).\overline{A0}.B0 + (A3 \copyright B3).(A2 \copyright B2).(A1 \copyright B1).(A0 \copyright B0).\overline{Ei}.\overline{Gi}$

Where A3 A2 A1 A0 & B3 B2 B1 B0 are comparing inputs and Gi Ei Li cascading inputs whose functionality is described in table.2

Table.2 truth table of proposed MC

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	Gi	Li	Ei	Go	Lo	Eo
A3>B3	X	X	X	X	X	X	1	0	0
A3=B3	A2>B2	X	X	X	X	X	1	0	0
A3=B3	A2=B2	A1>B1	X	X	X	X	1	0	0
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	1	0	0
A3<B3	X	X	X	X	X	X	0	0	1
A3=B3	A2<B2	X	X	X	X	X	0	0	1
A3=B3	A2=B2	A1<B1	X	X	X	X	0	0	1
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	1	0	0	1	0	0
A3=B3	A2=B2	A1=B1	A0=B0	0	1	0	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	0	0	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	1	1	0	0	0	0
A3=B3	A2=B2	A1=B1	A0=B0	0	0	0	1	1	0

Finally we have implemented MC using its basic building blocks. Fig.5 and fig.6 are the schematic and layout of MC.

There are various applications of our design. This design is flexible by which higher order of MC can be implemented.

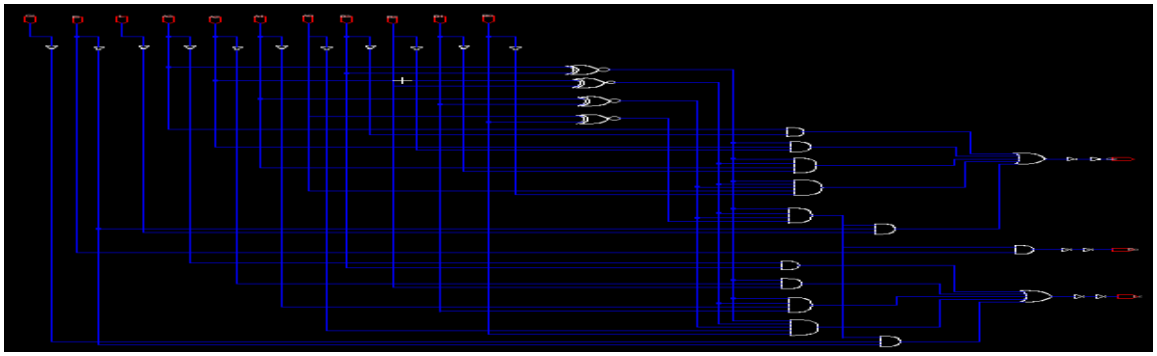


Fig.5 schematic of 4-bit MC (GDI tech)

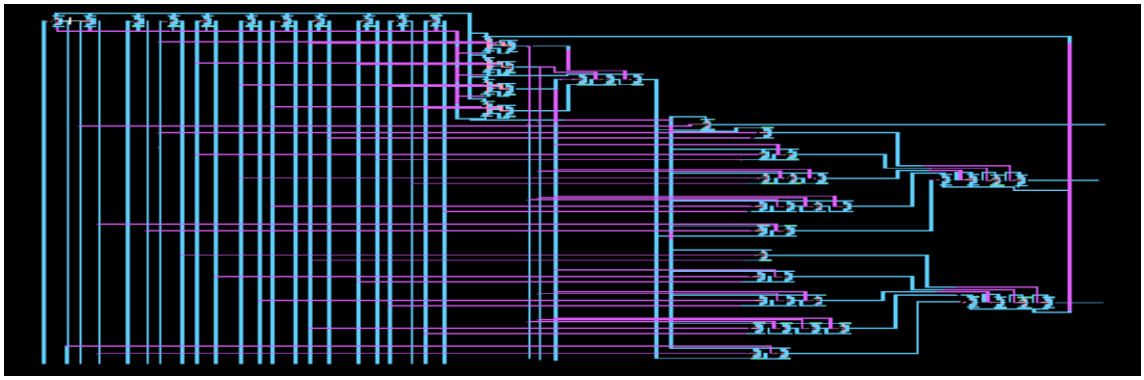


Fig.6 layout of 4-bit MC (GDI tech)

III. Analysis Of Simulation Resutl

(a) Wave form

Functionality of any design can be evaluated by the waveform obtained after the simulation. Here the simulation result of MC has shown in fig.7. Detail of its operation has described in table.2

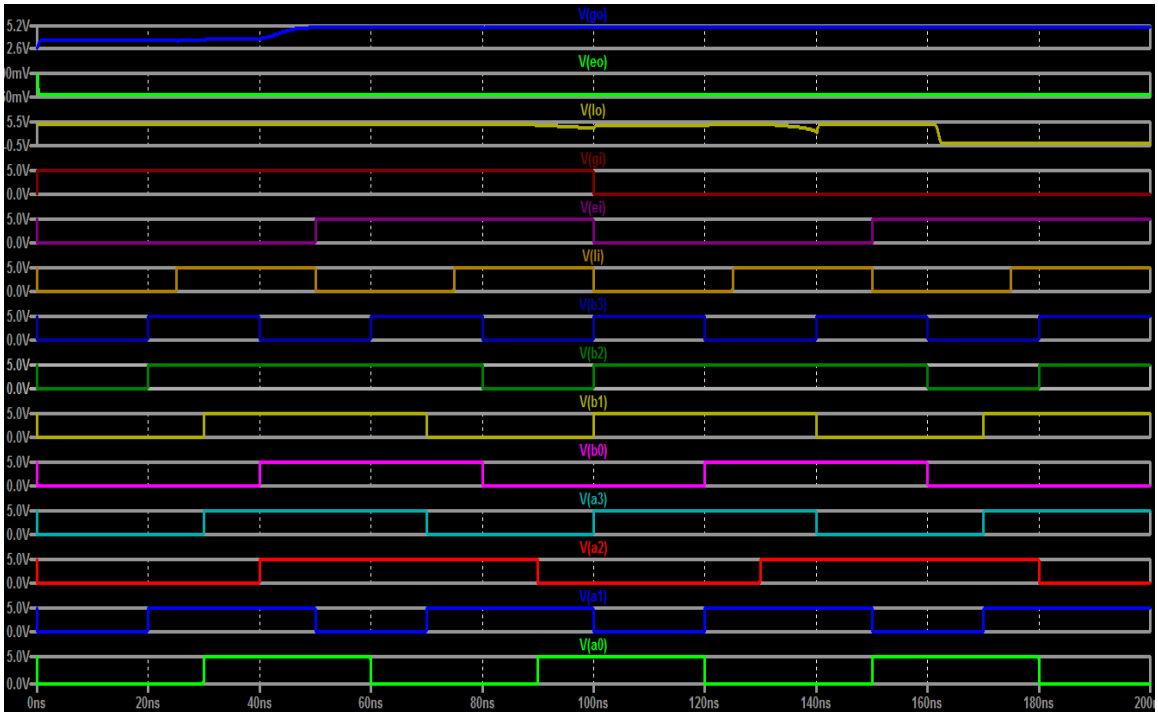


Fig.7 simulation result of 4-bit MC

(b) Spice code

The spice code is the code to provide input signal to design. We have used following spice code to generate above waveform.

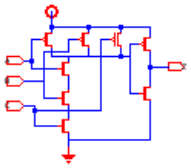
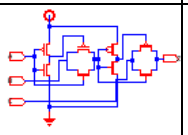
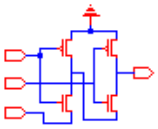
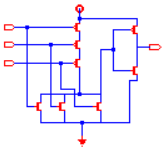
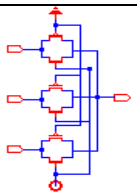
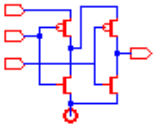
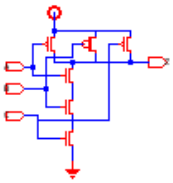
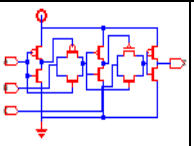
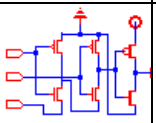
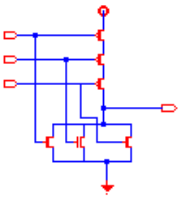
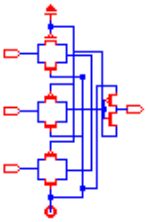
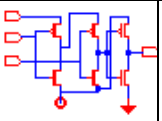
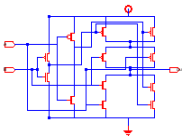
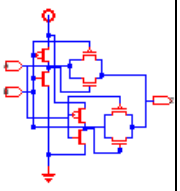
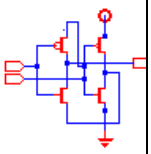
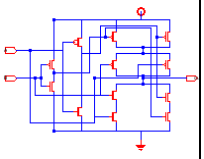
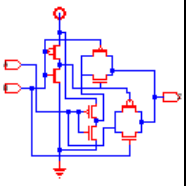
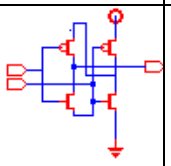
```
V1 VDD 0 DC 5
V2 GND 0 DC 0
.incluce E:\papers\4_BIT_comparator\PROJECT_2017_4bit_mag_comparator\schematic\C5_models.txt
V3 Gi 0 DC 5 PULSE 0 5 0 1ps 1ps 100ns 200ns
V4 Ei 0 DC 5 PULSE 5 0 0 1ps 1ps 50ns 100ns
V6 Li 0 DC 5 PULSE 5 0 0 1ps 1ps 25ns 50ns
V7 A3 0 DC 5 PULSE 5 0 0 1ps 1ps 30ns 70ns
V8 A2 0 DC 5 PULSE 5 0 0 1ps 1ps 40ns 90ns
V9 A1 0 DC 5 PULSE 5 0 0 1ps 1ps 20ns 50ns
V10 A0 0 DC 5 PULSE 5 0 0 1ps 1ps 30ns 60ns
V11 B3 0 DC 5 PULSE 5 0 0 1ps 1ps 20ns 40ns
V12 B2 0 DC 5 PULSE 5 0 0 1ps 1ps 20ns 80ns
V13 B1 0 DC 5 PULSE 5 0 0 1ps 1ps 30ns 70ns
V14 B0 0 DC 5 PULSE 5 0 0 1ps 1ps 40ns 80ns
.tran 1ps 200ns
```

In the spice code **VDD** is assigned a DC value of 5 volt and **GND** the DC value of 0 volt. **C5_models.txt** indicates the model file for NMOS and PMOS transistors. **PULSE** keyword is used to generate train of pulses and **.tran** keyword gives the transient analysis.

IV. Comparision

Today's technology demands to develop various new design techniques in order to reduce the chip area, propagation delay and power consumption. So it is necessary to make comparison against different technologies. Table.3 provides comparison against different technologies where multi-inputs gate s has implemented. This table basically provide idea to develop the design by the use of CMOS, TG and GDI techniques.

Table.3 Transistors usage in multi input Gates by different technologies

SL NO	GATE	TECHNOLOGIES					
		CMOS		TG		GDI	
		SCHEMATIC	TRANSISTORS USAGE	SCHEMATIC	TRANSISTORS USAGE	SCHEMATIC	TRANSISTORS USAGE
1	3-input AND		8		8		4
2	3-input OR		8		6		4
3	3-input NAND		6		10		6
4	3-input NOR		8		8		6
5	2-input XOR		12		8		4
6	2-input XNOR		12		8		4

Our design lastly provides following result whose details have given in table.4. TG tech. Uses 198 transistors whereas GDI tech. uses only 116 transistors to implement our design (MC).

Table.4 Transistors usage and delay of MC

Technology	Transistors Usage	Average Delay(in µs)	Power consumption (µW)
TG	198	56.3	654.2
GDI	116	37.4	455.7

V. Conclusion

Electric VLSI Design System is a high performance EDA tool that provides complete aids in designing the IC layout. It integrates the schematic editor, circuit simulator, schematic driven layout generator, layout editor, layout verification and parasitic extraction. Another advantage to Electric VLSI Design System is that it allows swapping between the designs data with other standard EDA tools in the industry [4] .
GDI tech. reduces 41.4% of chip area, 33.5% of average delay time and also 30.3% of power consumption over TG tech. which has shown in fig.8..

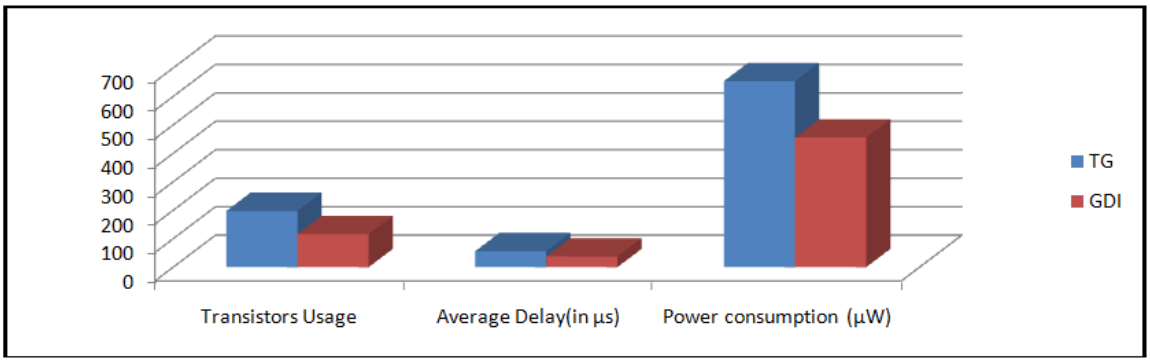


Fig.8 delay and transistors usage in USR using TG & GDI tech

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