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Educational Introduction to CMOS Circuit Design with Texas Instrument ANalyzer (TINA). Applications in Design of Digital CMOS Gates

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Abstract: *TINA software suite applied to the design of CMOS circuits is presented. Various analyses (DC Analysis, Transient, Controlling object analysis, Analysis with initial condition) are presented. The hierarchical design in terms of block-diagram representation of circuits, is illustrated through a design of the CMOS XOR gate. The work is based on a lecture on VLSI design, offered by the author to electrical and electronic engineering students taking a CMOS VLSI design course.*
Keywords *– MOS, CMOS, Digital-Gates, Circuit-Design-Techniques, Hierarchical-Design*

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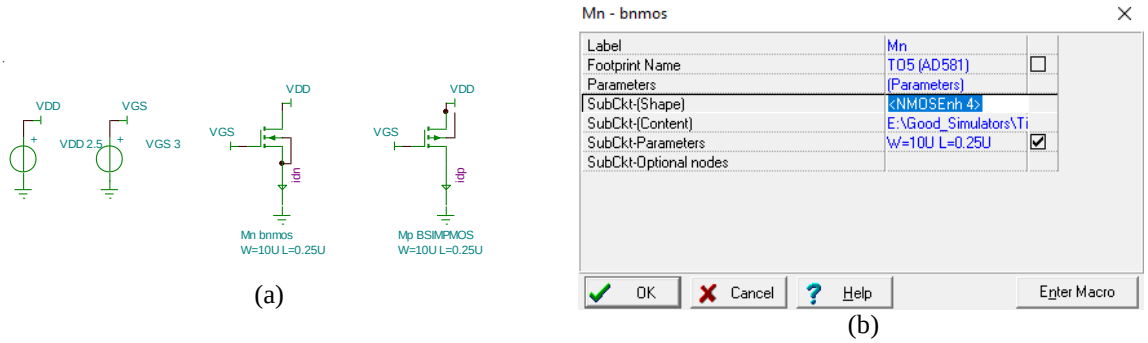
I. Introduction To Tina Capabilites For Mos Device Simulation – Dc Analysis

The purpose of the current article is to present an introduction to the concepts of CMOS circuit design [1,2] using the TINA-pro software [3]. It is based on designing basic digital-gates topologies. This work follows previous publications related to the educational presentation of VLSI design concepts and techniques [4-8]. The topics that will be studied here are specifically related to setting-up nmos and pmos device models using BSIM3 parameters [9] for corresponding circuit simulations of basic digital gates. Devices such as nmos and pmos in a circuit-design, are just symbols, carrying information about the electrical properties of actual devices in terms of systems of equations. The symbols of nmos and pmos are the visual representation of a SPICE description of each device.

TINA software has a dialog window for setting mos-device parameters (models: Symbolic, Schichman – Hodges, SPICE Level 1, 2, 3, S Level-3 (3F5), and BSIM3). Also (and this is the selection in the current article) permits the user to introduce SPICE model decks with technology parameters, as shown in Fig. 1 and Fig. 2. In the current article 0.25 CMOS technology parameters are used.



(a) (b)

Fig. 1. (a). Setting nMOS and pMOS for DC-Analysis. (b). Contents and parameters tab allow the application of changes in the technology model parameters and on the geometrical characteristics respectively.

Figure 1(a) shows the schematic setup for DC analysis of an nmos and a pmos transistor. The use of jumpers (the "TAY" shapes) is utilized in this and all subsequent schematics, in order to present clear designs by using limited number of wires connecting various circuit nodes. Two jumpers with the same name correspond to a wire connecting the specified nodes upon which are placed. Figure 1(b) shows an example of the dialog window popping up with double-clicking on the nmos symbol. Pressing "Enter Macro", a netlist is opened as seen in Fig.2(a). This is the SPICE description of the nmos using BSIM3 modeling equations and 0.25μm technology parameters. Figure 2(b) shows the corresponding SPICE file for the pmos. As seen in these SPICE

descriptions, the BSIM3 model is invoked in TINA using the LEVEL=7 directive. The command PARAMS: W=10u L=0.25 is made accessible though the SubCkt-Parameters in Fig. 1(b), where the user can change the value of the width and length of the device, without having each time opening, changing and saving the netlist.

```
*Berkely-Spice
.SUBCKT  nmos4  D G S B PARAMS: W=10u L=0.25u
M1       D G S B    nmos4    L={L}    W={W}
.MODEL nmos4 NMOS ( LEVEL=7
+TNOM     = 27              TOX      = 5.7E-9
+XJ       = 1E-7            NCH      = 2.3549E17       VTH0     = 0.4365497
+K1       = 0.3915623       K2       = 0.0175145       K3       = 1E-3
+K3B      = 2.6588343       W0       = 1E-7            NLX      = 1.111465E-7
+DVT0W    = 0               DVT1W    = 0               DVT2W    = 0
+DVT0     = -0.0408321      DVT1     = 0.0746768       DVT2     = 0.307109
+U0       = 407.1177485     UA       = 9.442714E-11    UB       = 1.092986E-18
+UC       = 1.63196E-11     VSAT     = 1.365087E5      A0       = 1.3189329
+AGS      = 0.2711719       B0       = 3.291713E-8     B1       = -1E-7
+KETA     = 4.645753E-3     A1       = 0               A2       = 1
+RDSW     = 439.9558234     PRWG     = 0.0345487       PRWB     = -0.0441065
+WR       = 1               WINT     = 1.645705E-9     LINT     = 1.116516E-9
+XL       = 3E-8            XW       = 0               DWG      = -1.494138E-9
+DWB      = 1.459097E-8     VOFF     = -0.1026054      NFACTOR  = 0.1344887
+CIT      = 0               CDSC     = 1.527511E-3     CDSCD    = 0
+CDSCB    = 0               ETA0     = 1.930311E-3     ETAB     = 2.946158E-4
+DSUB     = 0.0214865       PCLM     = 1.3387947       PDIBLC1  = 0.480652
+PDIBLC2  = 9.034986E-3     PDIBLCB  = -1E-3           DROUT    = 0.5593223
+PSCBE1   = 9.843289E9      PSCBE2   = 2.10878E-9      PVAG     = 1.0033136
+DELTA    = 0.01            MOBMOD   = 1               PRT      = 0
+UTE      = -1.5            KT1      = -0.11           KT1L     = 0
+KT2      = 0.022           UA1      = 4.31E-9         UB1      = -7.61E-18
+UC1      = -5.6E-11        AT       = 3.3E4           WL       = 0
+WLN      = 1               WW       = -1.22182E-16    WWN      = 1.2127
+WWL      = 0               LL       = 0               LLN      = 1
+LW       = 0               LWN      = 1               LWL      = 0
+CAPMOD   = 2               XPART    = 0.4             CGDO     = 3.11E-10
+CGSO     = 3.11E-10        CGBO     = 1E-11           CJ       = 1.758521E-3
+PB       = 0.99            MJ       = 0.457547        CJSW     = 4.085057E-10
+PBSW     = 0.8507757       MJSW     = 0.3374073       PVTH0    = 7.147521E-5
+PRDSW    = -67.2161633     PK2      = -1.344599E-3    WKETA    = 3.035972E-3
+LKETA    = -9.0406E-3      LAGS     = -0.3012          )

.ENDS nmos4
```

(a)

```
.SUBCKT BSIMPMOS 1 2 3 4 PARAMS: W=10u L=0.25u
M1 1 2 3 4 PMOS W={W} L={L}
.model PMOS PMOS (Level= 7
+TNOM     = 27              TOX      = 5.7E-9
+XJ       = 1E-7            NCH      = 4.1589E17       VTH0     = -0.6586391
+K1       = 0.5199897       K2       = 0.0357513       K3       = 0
+K3B      = 15.5613889      W0       = 1E-6            NLX      = 1E-9
+DVT0W    = 0               DVT1W    = 0               DVT2W    = 0
+DVT0     = 2.6100181       DVT1     = 0.4363142       DVT2     = -0.042436
+U0       = 196.024903      UA       = 2.767112E-9     UB       = 1.90709E-18
+UC       = 6.166867E-11    VSAT     = 1.975064E5      A0       = 0.2398712
+AGS      = 0.0943234       B0       = 3.21184E-6      B1       = 5E-6
+KETA     = 0.0312217       A1       = 0               A2       = 1
+RDSW     = 997.072701      PRWG     = -0.1916111      PRWB     = -0.495
+WR       = 1               WINT     = 2.527293E-9     LINT     = 1.254514E-8
+XL       = 3E-8            XW       = 0               DWG      = -3.253948E-8
+DWB      = 4.92072E-8      VOFF     = -0.15           NFACTOR  = 1.5460516
+CIT      = 0               CDSC     = 1.413317E-4     CDSCD    = 0
+CDSCB    = 0               ETA0     = 0.7241245       ETAB     = -0.240523
+DSUB     = 1.0813613       PCLM     = 2.0772083       PDIBLC1  = 4.31459E-4
+PDIBLC2  = 0.0252121       PDIBLCB  = -9.960722E-4     DROUT    = 0.0432774
+PSCBE1   = 3.191047E10     PSCBE2   = 1.323218E-8     PVAG     = 0.0420525
+DELTA    = 0.01            MOBMOD   = 1               PRT      = 0
+UTE      = -1.5            KT1      = -0.11           KT1L     = 0
+KT2      = 0.022           UA1      = 4.31E-9         UB1      = -7.61E-18
+UC1      = -5.6E-11        AT       = 3.3E4           WL       = 0
+WLN      = 1               WW       = 0               WWN      = 1
+WWL      = 0               LL       = 0               LLN      = 1
+LW       = 0               LWN      = 1               LWL      = 0
+CAPMOD   = 2               XPART    = 0.4             CGDO     = 2.68E-10
+CGSO     = 2.68E-10        CGBO     = 1E-11           CJ       = 1.902493E-3
+PB       = 0.9810285       MJ       = 0.4644362       CJSW     = 3.142741E-10
+PBSW     = 0.9048624       MJSW     = 0.3304452       PVTH0    = 4.952976E-3
+PRDSW    = 29.8169373      PK2      = 3.383373E-3     WKETA    = -7.913501E-3
+LKETA    = -0.0208318       )
.ENDS
```

(b)

Fig. 2. BSIM3 0.25µm parameters for (a) nMOS and (b) pMOS

In order to simulate the Current-Voltage (IV) characteristics of the two devices, a DC analysis has to be set. Figure 3(a) shows the setup for obtaining the current vs. V_{DS} and Fig. 2(b), the setup for obtaining the current vs. V_{GS}. Figure 3(c) shows the corresponding current vs. V_{DS} plot for the nmos (idn) and the pmos (idp) transistor in log-lin scale. Figure 3(d) shows the corresponding current vs. V_{GS} plot for the nmos (idn) and the pmos (idp). The use of current-arrow symbols idn and idp in the circuit design (shown in Fig. 1(a)) instruct TINA preprocessor to calculate the source-drain current for each voltage-value during DC analysis, resulting in the data seen in Fig. 3.

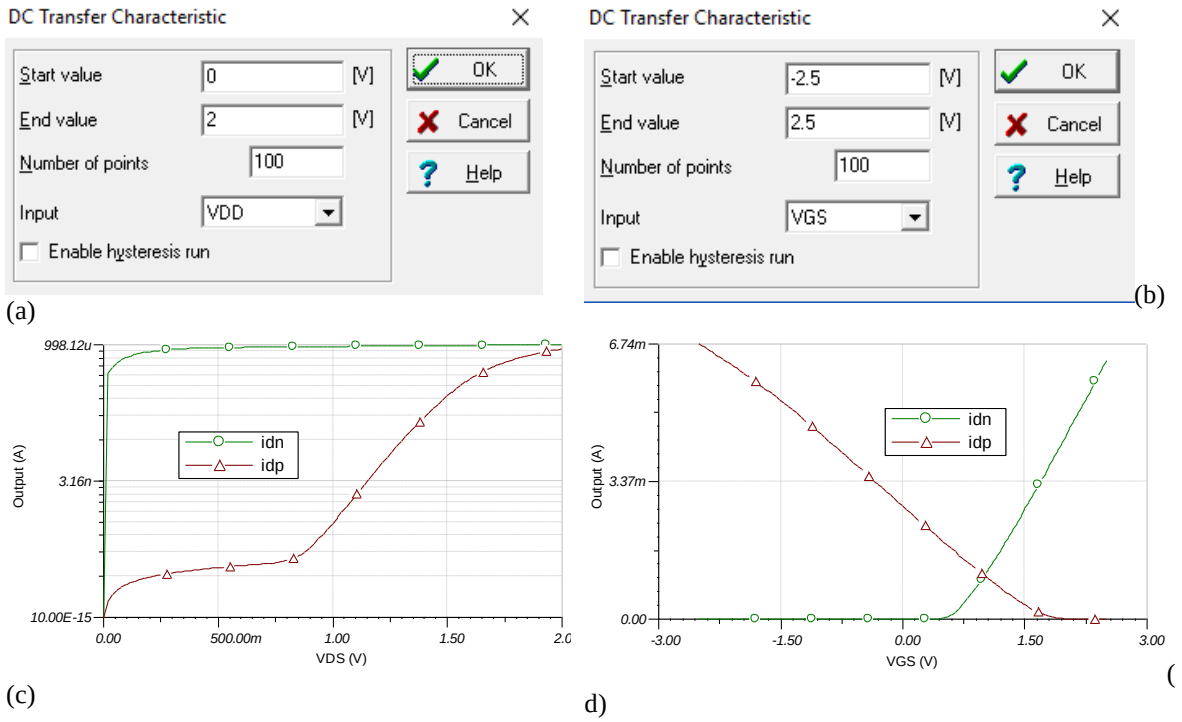


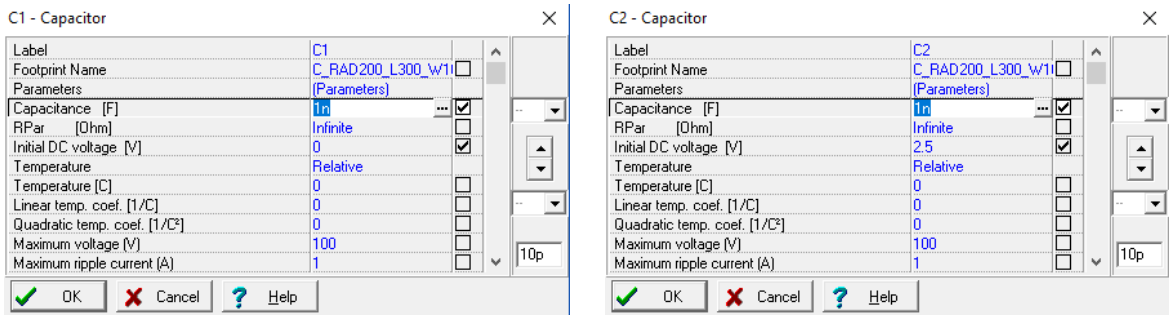
Fig. 3. (a). Setting I vs. V_{DS} DC analysis. (b). Setting I vs. V_{GS} DC analysis. (c). I vs. V_{DS}. (d). I vs. V_{GS}.

II. The Mos As A Switch – Transient Analysis

Having set up and performed the DC analysis of single nmos and pmos devices, the next step is to check their switching properties. Figure 5(a) presents the circuit schematic setup for studying the ability of the devices for reliable capacitor charge and discharge. The capacitor used in each case is either fully discharged or completely charged. Figure 4(a) shows the capacitor's settings-dialog-window, with Initial-DC-Voltage = 0V, and Fig. 4(b) shows the same dialog-window for Initial-DC-Voltage = 2.5V. The initial-capacitor-voltage settings are used in the simulation setup shown in Fig. 5(a). Figure 6 shows the transient analysis window dialog. Note that the "Use initial conditions" setting is selected to take into account the initial DC voltage of the capacitors.

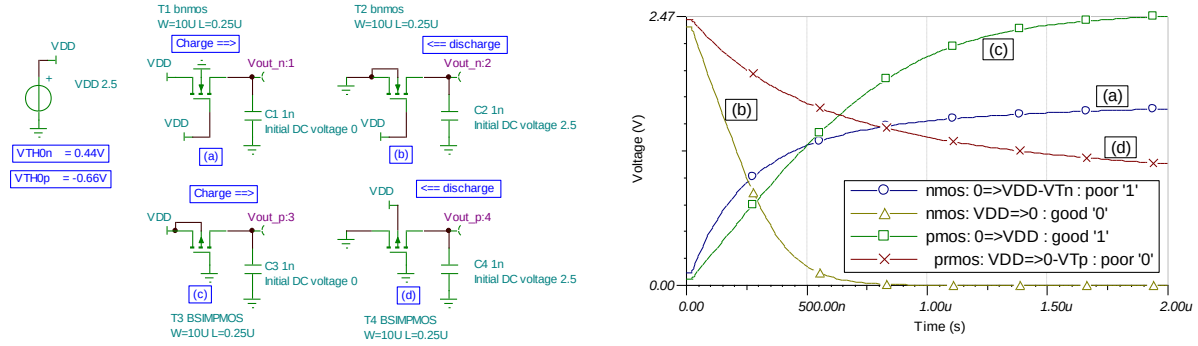
The tests on Fig. 5(a) are as follows: First nmos attempts to charge a discharged capacitor to the V_{DD}. This nmos has V_{DD} on input and V_{DD} on source (Fig. 5(a)-circuit-(a)). Next, an nmos discharges a fully charged capacitor to ground. This nmos has V_{DD} on gate and ground on source (Fig. 5(a)-circuit-(b)). Then, a pmos charges a capacitor to V_{DD}. This pmos has ground on gate and V_{DD} on drain (Fig. 5(a)-circuit-(c)). Finally, a pmos discharges a fully charged capacitor to ground. This pmos has ground on gate and ground on drain (Fig. 5(a)-circuit-(d)).

Figure 5(b) shows the results from the transient analysis. Specifically, the capacitor voltages (Vout_n:1, Vout_n:2, Vout_p:3, Vout_p:4). Take into consideration that nmos and pmos conduct when gate voltage is greater than the threshold V_{tn} and less than V_{tp} respectively. What is seen in the graph are well known facts in CMOS literature [1,2]: (a) the nmos gives a poor "1" i.e., it cannot charge the capacitor up to V_{DD} voltage but only up to V_{DD}-V_{tn}. (b) the nmos gives a good "0" i.e., it can discharge the capacitor down to 0 volts. (c) The pmos gives a good "1" i.e., it can charge the capacitor to V_{DD} volts. (d) The pmos gives a poor "0" i.e., it cannot discharge the charged capacitor down to 0 voltage, but only down in to $|V_{tp}|$.



(a) (b)

Fig. 4. (a) Capacitor with 0V initial DC voltage. (b) Capacitor with 2.5V initial DC voltage.



(a) (b)

Fig. 5. (a). Circuit for checking the switching properties of nMOS and pMOS. (b). Timing analysis results.

Another transient analysis with digital input sources is seen next. Figure 7(a) shows the circuit schematic setup. V_{GS} is a 500kHz clock and V_{DD} is a 1MHz clock. Figure 7(b) shows the currents vs. time. Observe the duality in nmos and pmos function. Also observe that the nmos current (idn) is almost twice compared to a pmos' with the same W/L ratio (idp_w10u). This is due to nmos' approximately twice carrier mobility. To compensate, the W of pmos is set to twice that of nmos' and the resulting current (idp_w20u) is approximately equal to idn. This analysis also presents the practical quality of TINA to perform mixed simulations of digital sources and analog device models on the same circuit schematic.

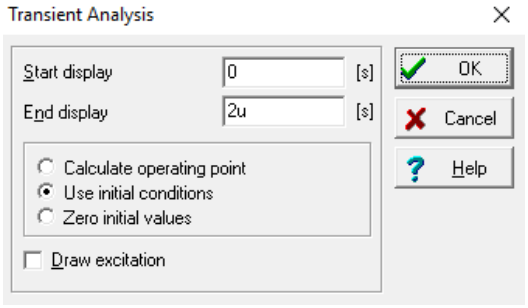
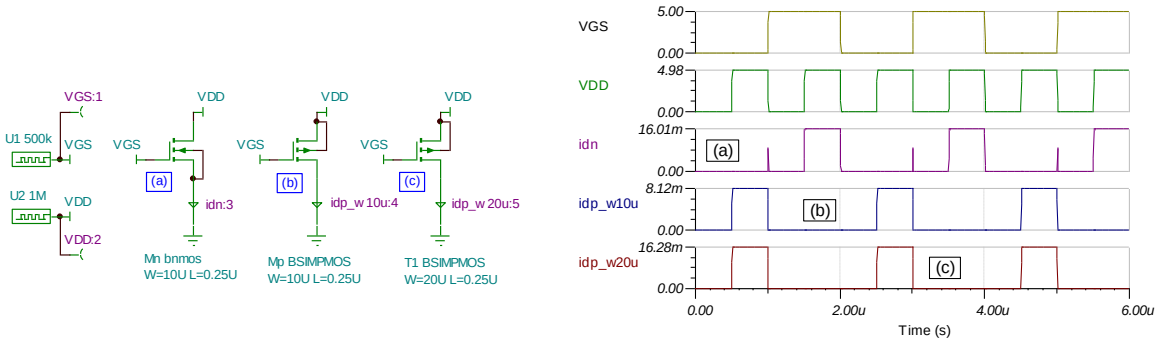


Fig. 6. Transient analysis dialog window.

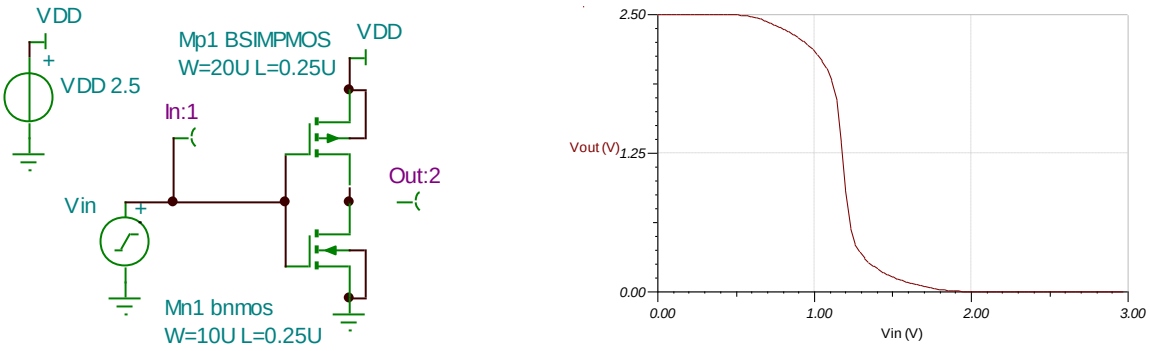


(a) (b)

Fig. 7. (a) Circuit of timing analysis using digital signal source for nmos and pmos with the same width and pmos with double width for comparison. (b) Transient analysis results.

III. 2 Transistor Gates. Inverter And Transmission Gate

The simplest CMOS gate is the inverter and the transmission gate. Both consist of an nmos and a pmos. Their structure is based on using the more reliable of the two devices, depending on the input conditions. For example Fig.8(a) shows a CMOS inverter circuit topology and Fig. 8(b) the corresponding voltage transfer characteristic, showing that the commutation point of the inverter is approximately at 1.2V of input voltage in this case. Figure 9(a) shows the setup circuit for the timing analysis seen in Fig. 9(b), where it is verified the inverting behavior of this gate. The topology of the inverter is such that when the input is "1", only the nmos device is "on", connecting the output to ground, and when the input is "0", only the pmos device is "on", connecting the output to the supply. In each case the strong "0" and the strong "1" is achieved, based on what is discussed in the previous section.

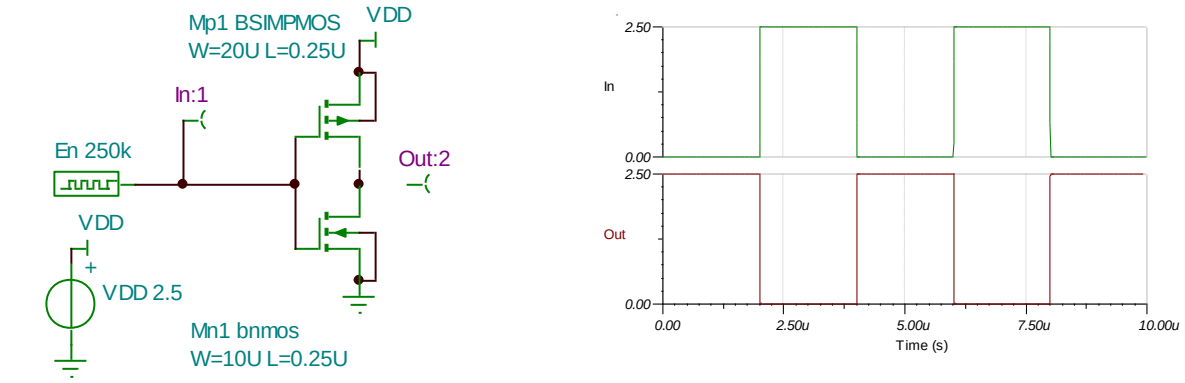


(a) (b)

Fig. 8. (a). CMOS inverter circuit. (b) Voltage transfer characteristic.

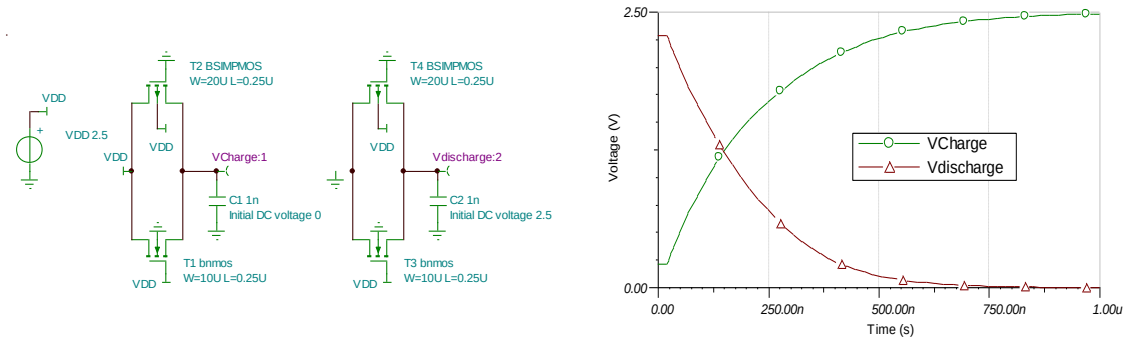
The other simple two-transistor gate is the transmission gate, shown in Figure 10(a). In the first circuit the objective is to observe the capacitance charging, while on the second circuit setup, the objective is to observe the corresponding capacitor discharging. Figure 10(b), shows that in both cases the transmission gate delivers a "good" result, either "1" or "0". Figure 11(a) shows the circuit setup for transient analysis simulation

of the transmission gate. The design is all CMOS based. Figure 11(b) verifies that the transfer of input D to the output Out is achieved under synchronous En=1 and Ep=0 signals, when both nmos and pmos are on.



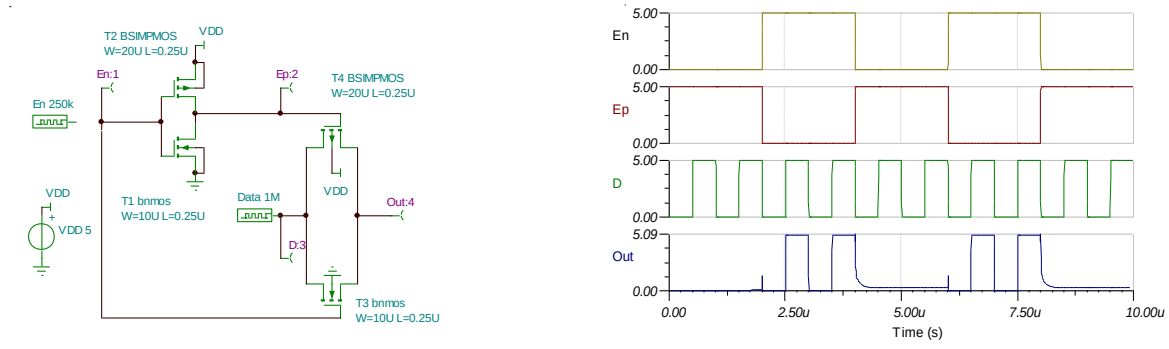
(a) (b)

Fig. 9. (a) CMOS inverter circuit setup for digital timing analysis. (b). In/Out timing analysis.



(a) (b)

Fig. 10. (a). Transmission gate setup for charging and discharging. (b). Timing analysis results.

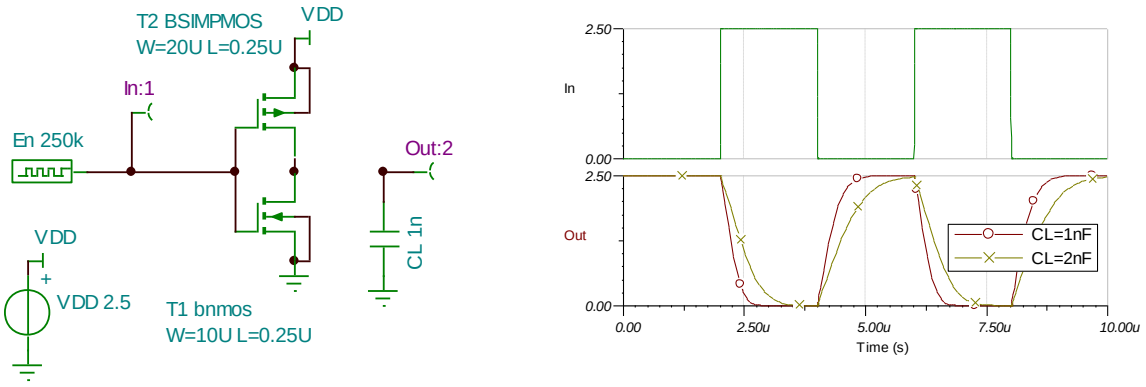


(a) (b)

Fig. 11. (a). Transmission gate circuit setup digital source input. (b). Timing analysis results.

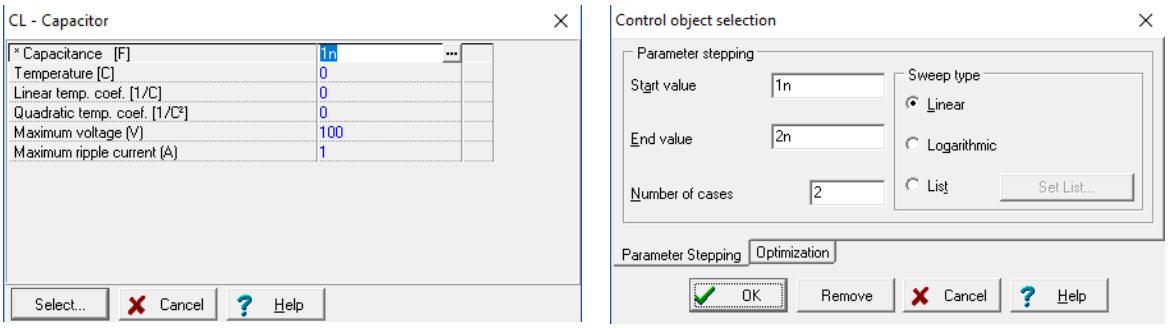
An interesting subject in the literature about inverters is their driving capability in terms of loading capacitances. Figure 12(a) shows a circuit setup for the analysis of this effect. Notice the capacitance CL at the output of the inverter. TINA, through the menu Analysis > Select Controlling Object gives the user the ability to select the capacitance by clicking on it and setting parameter-stepping on the value of the capacitance. Figure 13(a) shows the initial dialog window where, after pressing the "Select" button the parameter-stepping options window is enabled, as in Fig. 13(b). If this selection is no longer required the user has to repeat the process and then select the "Remove" button (Fig. 13(b)). Here the controlling object is the capacitor CL, and the stepping is done on the value of the capacitance starting at 1nF, ending at 2nF, with only these two values (Number of cases

=2). Figure 12(b) shows the result of the timing analysis. It is seen how increasing capacitance leads to longer charging time and thus increases the signal propagation time.



(a) (b)

Fig. 12. (a). CMOS inverter charging an output capacitance. (b). Timing analysis results.



(a) (b)

Fig. 13. (a). Selecting control object. (b). Setting control object selection.

IV. Ring Oscillator

Figure 14 shows the circuit schematic of 5 successive CMOS inverters. Such a circuit is known in literature as a ring oscillator because it produces voltage oscillations in the output node Out, due to the feedback connection. Figure 15 shows the timing analysis for the first 4ns where the onset of oscillations is captured. Using the 'a' and 'b' cursors in the graph window, TINA measures the period of oscillations (353.7ps), so the inverse is the corresponding oscillation frequency. This simple arithmetic calculation can be done in TINA's interpreter as seen in Fig 16, resulting in a frequency of approximately 2.8GHz. Interpreter can be used also for advanced computing if required, as it supports several mathematical functions and programming constructs.

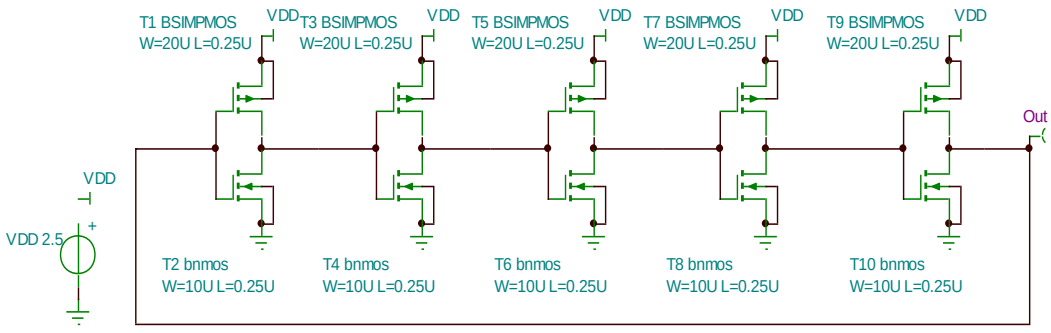


Fig. 14. Ring oscillator with five inverters.

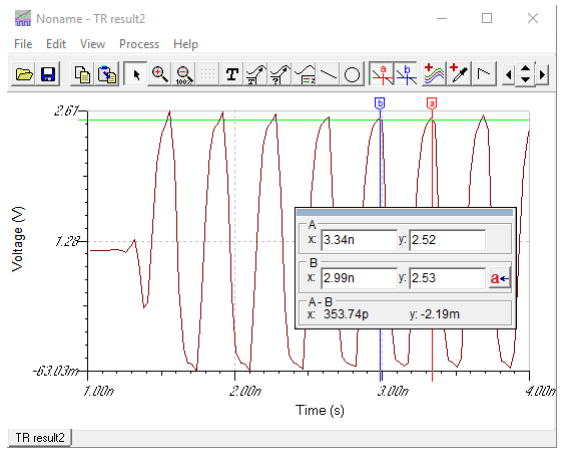


Fig. 15. Output of ring oscillator and metrics in order to determine the frequency of oscillations.

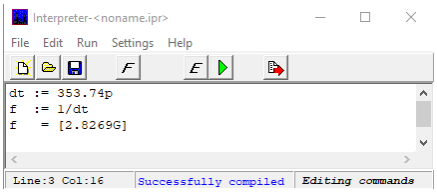
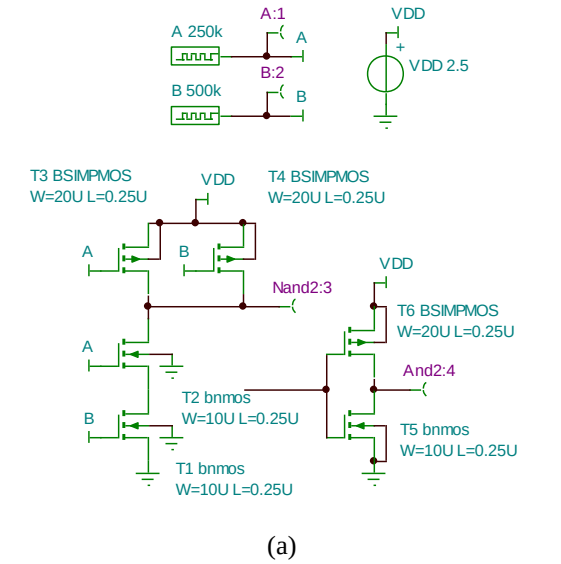


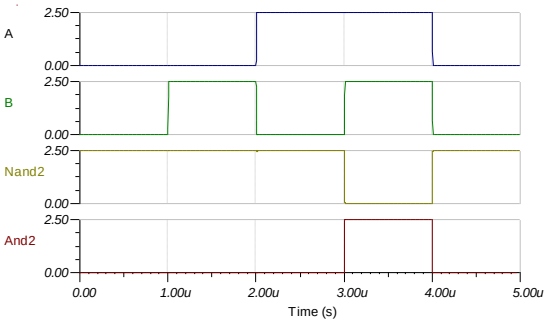
Fig. 16. Screenshot of the TINA's interpreter window used for basic calculations.

V. 2-Input Universal Cmos Gates

The next steps in the design of gates, are the simple two-input universal gates of NAND and NOR, and their corresponding inverted versions of AND and OR respectively. Figure 17(a) shows the CMOS two-input NAND and AND gate and Fig.17(b) the timing analysis that verifies the gate's behavior. Figure 18(a) shows the CMOS two-input NOR and OR gate and Fig. 18(b) the timing analysis that verifies the gate's behavior.

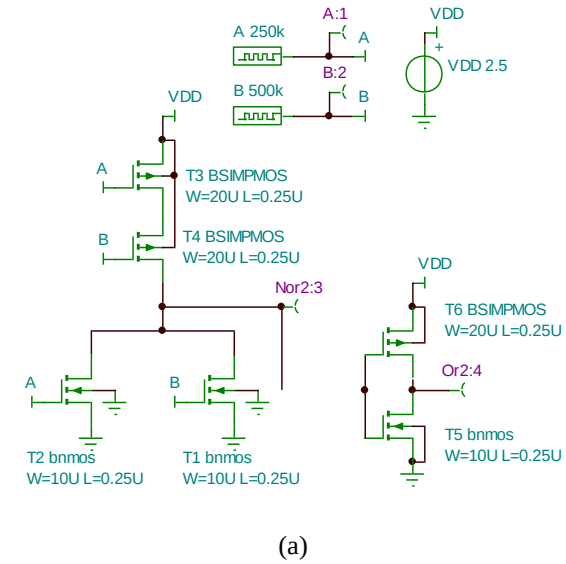


(a)

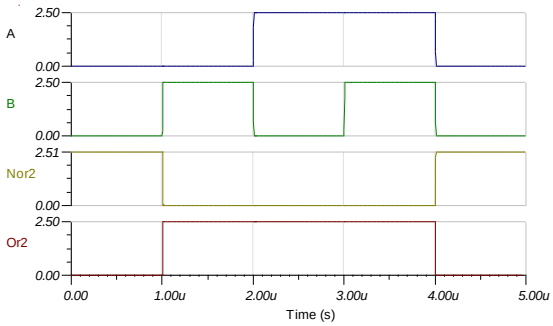


(b)

Fig. 17. (a). CMOS NAND and AND two-input gate. (b). Timing analysis graph.



(a)



(b)

Fig. 18. (a). CMOS NOR and OR two-input gate. (b). Timing analysis graph.

VI. Cmos Xor Gate

The XOR gate is not a universal one, but is used here in order to present the concept of hierarchical design process and the use of block-design units with TINA. Figure 19 shows the CMOS two input XOR gate

structure. The circuit implements in CMOS logic function A'B + AB' (A' = not(A) and B'=not(B)) which is the definition of XOR, using 2 NOT (inverters), 2 AND, 1 OR CMOS gates, a total of 22 transistors.

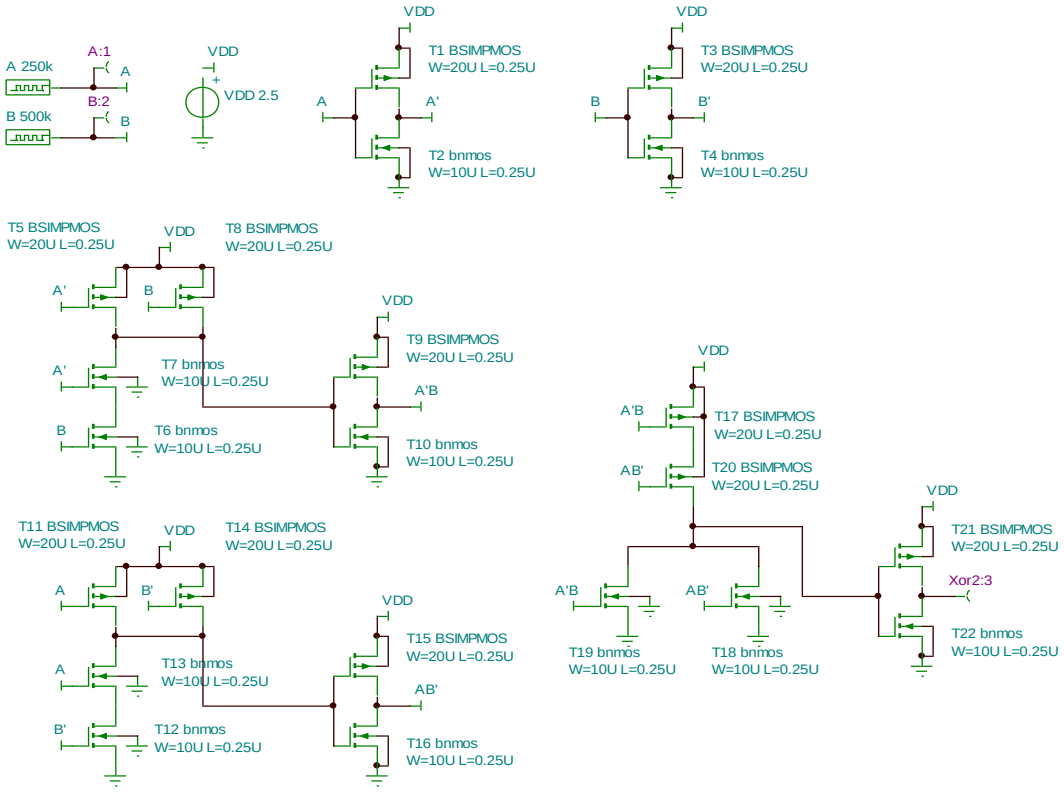


Fig. 19. CMOS XOR two input gate. 22 transistor implementation.

Figure 20 verifies with timing analysis the correct function of the XOR gate. It is advisable, when realizing complex functions using the CMOS principles, to manipulate the circuit structure representation in order to hide a lot of the details and present the overall Boolean character of the circuit. This is achieved using the block-diagram technique.

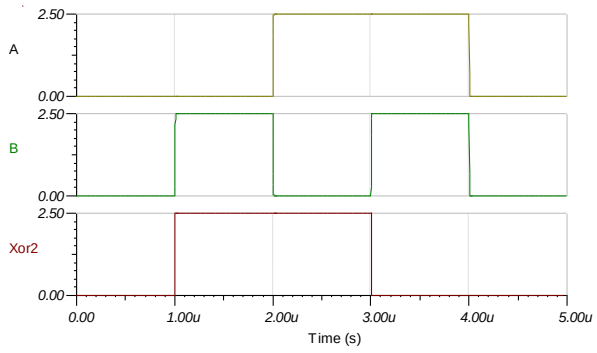


Fig. 20. Timing analysis graph of CMOS XOR two-input gate.

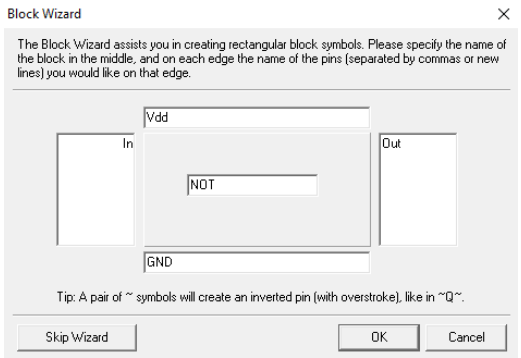


Fig. 21. Insert block dialog window. Input – output pins and block name are imported directly. Several other editing tools exist and made accessible after OK button is pressed.

Invoking from the menu the Insert > Block, the dialog window of Fig. 21 is enabled. The principle is simple: The user enters a name for the block and assign names for the inputs and outputs. In this case a NOT gate is to be created. Once the block diagram is created, with right-clicking on it, and pressing "Enter Macro", the user is "directed" in the "internal structure" of the block, where can place the various circuit components for the corresponding block function.

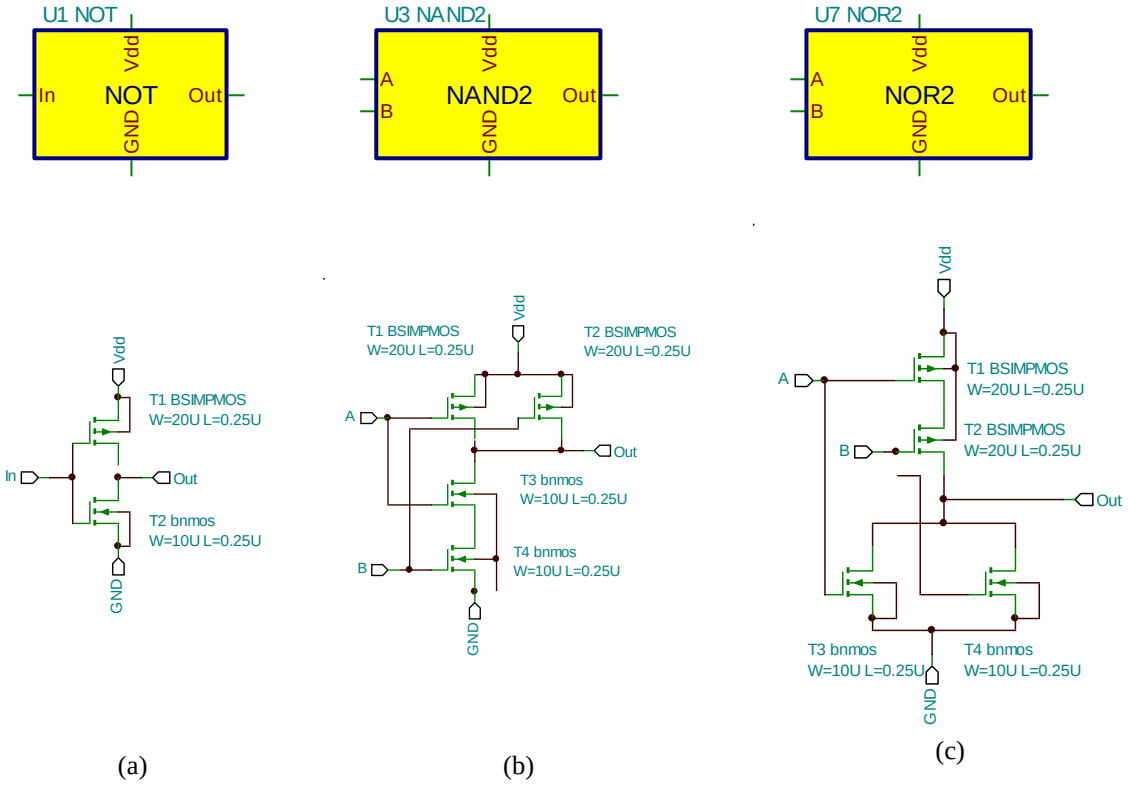


Fig. 22. Block diagram and internal block structure for (a). NOT gate, (b). NAND2 gate, (c). NOR2 gate. Macro pins connect the internal structure of the block to the external connections in the overall circuit.

Figure 22 shows examples of the block icon and the corresponding internal structure of the NOT, NAND, and NOR CMOS gates. Using such block elements (by copy and paste as many times as needed), the XOR gate is redesigned as seen in Fig. 23. This circuit performs the same function as the one of Fig. 19, but it is easier to grasp the Boolean function it realizes. Even this last circuit could be incorporated within a block named XOR with two inputs and one output (Fig. 24), hiding completely the internal workings and leaving only the function name to be seen. Such hierarchical design leads to circuits that are easier to understand and maintain or update.

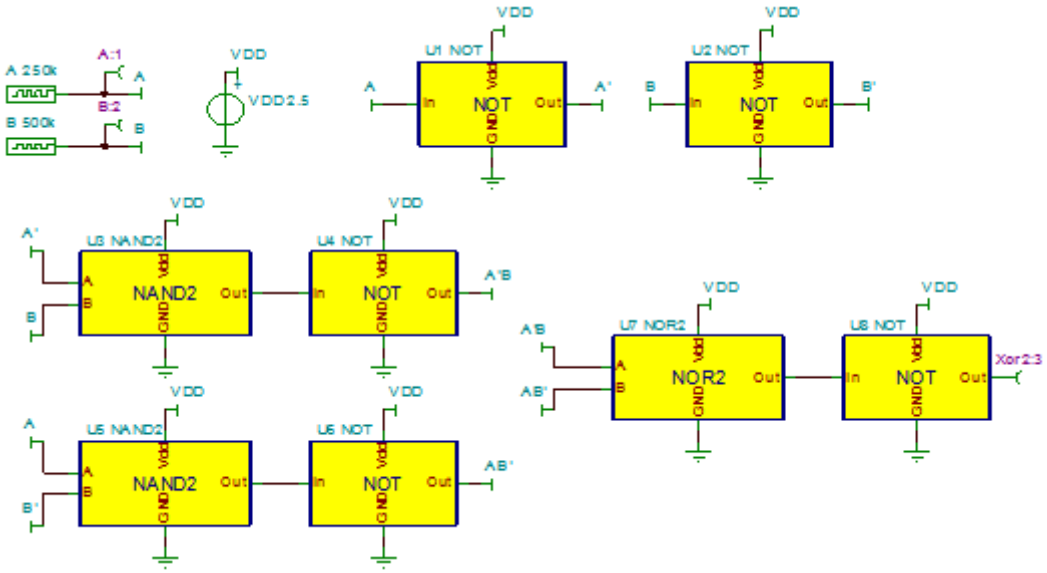
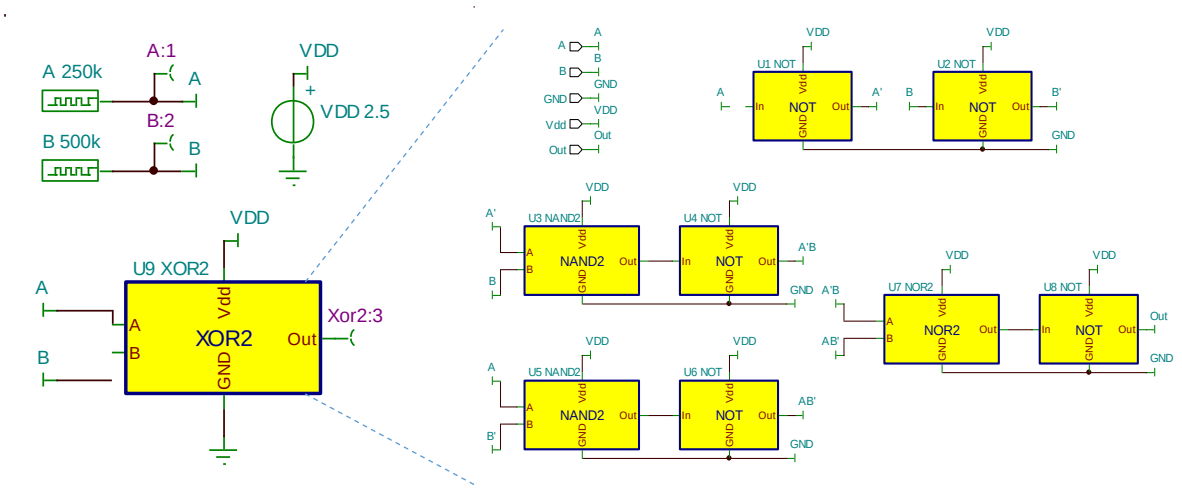


Fig. 23. CMOS XOR2 gate with hierarchical design using block diagrams in order to make the circuit structure easier to grasp.



(a) (b)

Fig. 24. Maximum information hiding in the case of XOR2 (blocks within block).

VII. Conclusion

In the current article an educational review of CMOS design principles was presented using the TINA-Pro software suite. Using nmos and pmos device BSIM3 SPICE files, changing the input file parameters and rerunning the simulations gives the ability to compare between different technology implementations and quantify predictions. Several important details in aiding design, were pointed and various examples were presented featuring various analysis types. The presented material is suitable for fast introducing electrical and electronic engineering students to the CMOS gate design of basic digital gates.

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