IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 9, Issue 4, Ser. I (Jul. - Aug. 2019), PP 18-27
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Design of High Speed and Low Power Domino Logic Circuits for Wide Fan-in gates

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Abstract: *In this brief, a new Comparator based Domino logic design is proposed. The Comparator technique is used to compare the voltages and the Domino logic technique is used to implement the logic function. In the existing system, The different domino logic techniques are designed for wide fan-in gates. The Foot Driven Stack transistor domino logic technique is one of the existing method. This leads to increase in delay . To overcome this problem a Comparator based domino logic is proposed. This Comparator based domino logic is having lower power consumption and low propagation delay than existing domino logic circuits. The backend simulations are achieved by using MENTOR GRAPHICS in 130nm technology and frontend simulations are done by using XILINX.*

Keywords: *Digital circuits, ,High speed domino gate, Low power VLSI circuit, Wide fan-in gates, Comparator based domino logic gate, Mentor graphics,Xilinx.*

Date of Submission: 21-08-2019 Date of Acceptance: 05-09-2019

I. Introduction

Wide fan-in dynamic logic gates are the preferred choice in large memories and high-speed processors due to high speed and smaller area characteristics as compared to static CMOS logic gates [1]. Wide fan-in OR dynamic gates [2] are basic building blocks of modern microprocessors and also employed in the read path of resister files, flash memory, programmable logic arrays, tag comparators, match lines of ternary contents addressable memories, L1 latches, wide De-Mux flip-flop, and Mux flip-flop [3–6] etc. However, in most applications, the wide fan-in dynamic gate is strongly suffered by large leakage current and less Noise Immunity (NI) with low Threshold Voltage (VTH). To overcome these problems, K. Roy et al. [7] proposed a new method in which Pull Down Network (PDN) is designed with NMOS transistors having high V_{TH}. But this high V_{TH} slows down the discharging of the Dynamic Node (DN) through PDN. Further, K. Royet al. [7] proposed another design with PMOS keeper to keep the DN at logic high. An ideal domino gate for wide fan-in is assumed to have low Power Dissipation (PD), and minimum contention current with less area overhead. The output logic of domino gate is characterized by charging and discharging of output node capacitor. The Average power consumption of a domino logic gate is given by the Equation [8]:

$$P_g = P_{short} + P_{switch} + P_{leakage}$$

where P_{short} is the short circuit power consumption due to the shorting of the supply and ground. P_{switch} is the power consumed due to charging and discharging of the load capacitance. $P_{leakage}$ is the power consumed due to the gate and sub threshold leakage current.

To reduce the power consumption in domino logic circuits, several techniques have been proposed in the previous papers[9,10,11]. All of these techniques are modified form of the basic Footerless Domino Logic (FLDL) [7] and Footed Domino Logic(FDL) [7]. In these techniques, additional P and N channel transistors and delay elements are used to reduce power consumption, propagation delay.

II. Different Domino Logic Circuits

The Domino logic circuit is used to speed up the circuit. The Domino logic circuit requires 2N+2 transistors. It requires less area when compared to the static CMOS logic technique because the pull up network requires only one PMOS transistor. For implementing high speed and high performance microprocessors, domino logic is preferred than the other dynamic logic circuits.

2.1 FOOTERLESS DOMINO LOGIC(FLDL):

The first technique designed for domino logic design was Footerless Domino Logic [7] (FLDL) as shown in Fig. 1. In this technique, The domino logic has two phases. The first phase is precharge phase and the other phase is evaluation phase. In the evaluation phase, keeper transistor turns ON and connects the dynamic node to supply. Thus, prevents any undesirable discharge of the dynamic node due to charge sharing problem of Pull-Down Network [12,13].

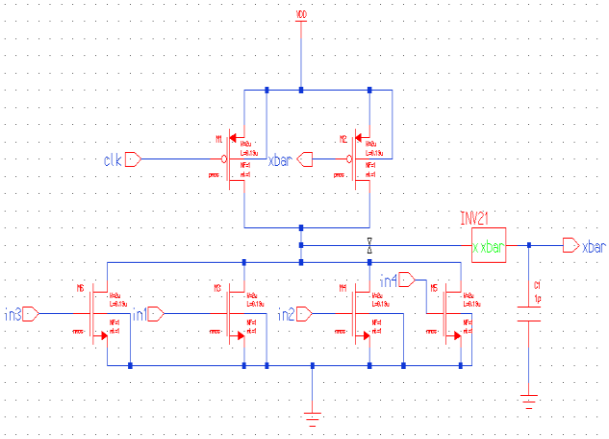


Fig. 1 Footerless Domino Logic

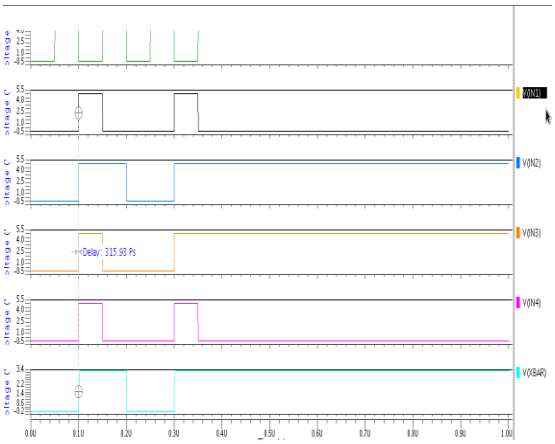


Fig. 2 Waveforms of Footerless Domino Logic

The keeper ratio [7,13] is given by:

$$K = W_{keep} / W_{eval}$$

where W_{keep} is the width of keeper transistor and W_{eval} is the width of evaluation transistors. Therefore, on increasing K, the robustness of the domino circuit increases with the increase in power consumption and propagation delay.

Fig. 2 shows the variation of power consumption in FLDL domino circuit with the increase in the size of the keeper. As the size of keeper increase, power consumption increases due to increased contention between the keeper and evaluation logic.

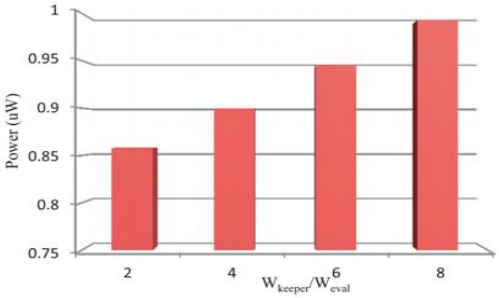


Fig.3 Effect of keeper sizing on power consumption of FLDL domino logic circuit

2.2 FOOTED DOMINO LOGIC(FDL):

The major drawback of FLDL technique is the leakage current through pull down network during the evaluation phase. This can be avoided by inserting a footer transistor N1 in series. But by adding the footer transistor, it introduces the delay therefore reduces the speed of the circuit.

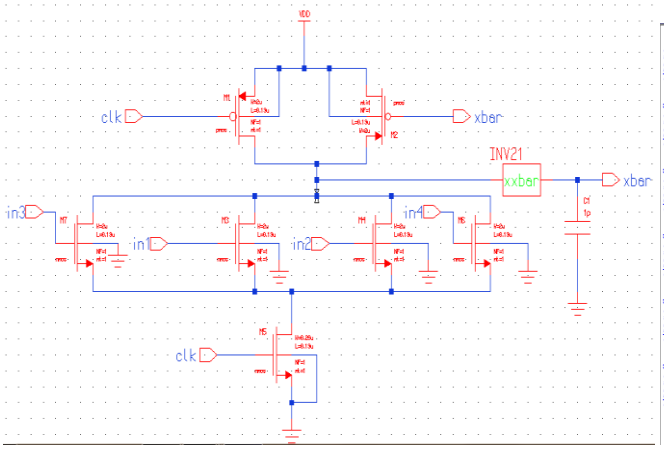


Fig 4. Footed Domino Logic

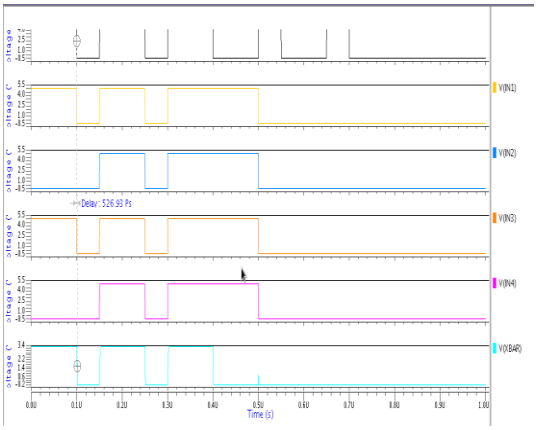


Fig 5. Waveforms of Footed Domino Logic

2.3 CURRENT MIRROR FOOTED DOMINO LOGIC(CMFD):

To reduce the delay, current mirror transistors N2 and N3 are inserted in the FDL logic shown in Fig. 6. These transistors reduce delay but increase discharging current in the circuit. In order to stop discharging of the dynamic node, transistor N4 provides a feedback path from the gate of the current mirror to the output of circuit as shown in Fig. 6.

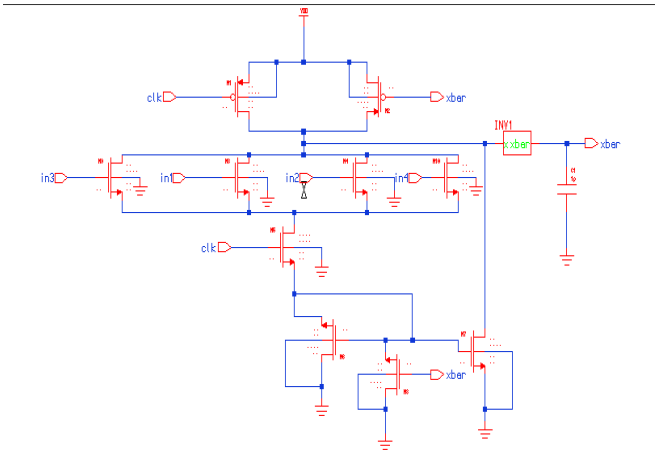


Fig. 6. Current Mirror Footed Domino Logic

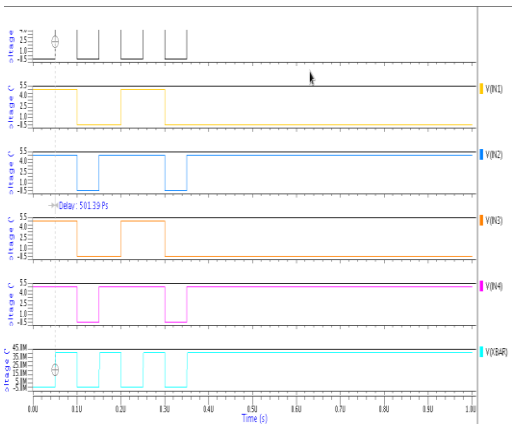


Fig. 7. Waveforms of Current Mirror Footed Domino Logic

2.4 HIGH SPEED CLOCKED DELAY DOMINO LOGIC(HSCD):

In High-Speed Clock Delay (HSCD) [9,10] circuit shown in Fig. 8, transistor N1 is ON at the beginning of precharge mode. Therefore, node N connects to ground through N1. In addition, node GN is at a low voltage that turns off N2. Transistor N1 turns off after a delay equal to delay of two inverters. The voltage at node N biases the transistor in evaluation logic, which decreases leakage current in evaluation logic thus reducing the leakage power consumption. The voltage at node n depends on the size of the footer transistor and evaluation transistors.

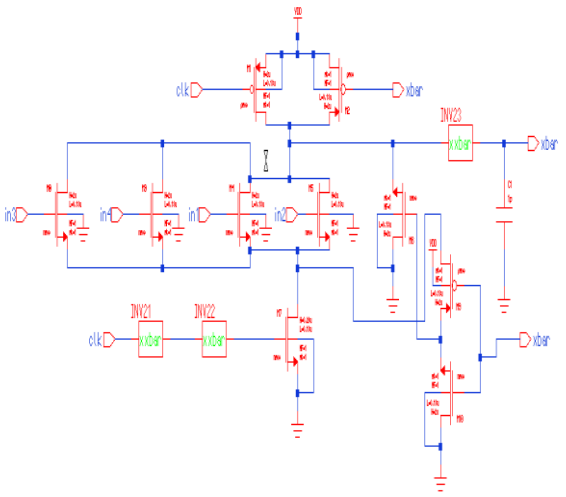


Fig. 8. High Speed Clocked Delay Domino Logic

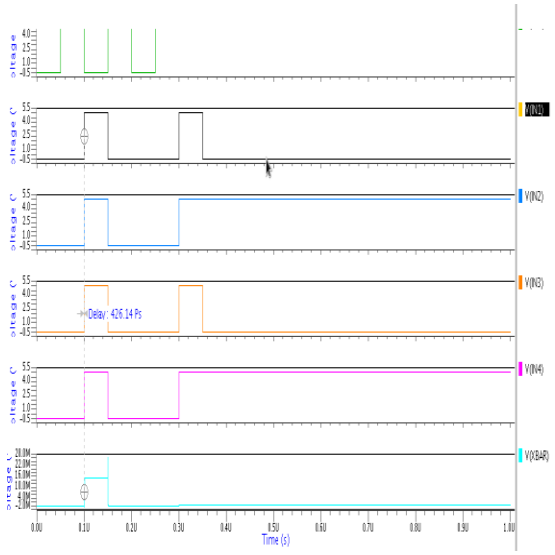


Fig. 9. Waveforms of High Speed Clocked Delay Domino Logic

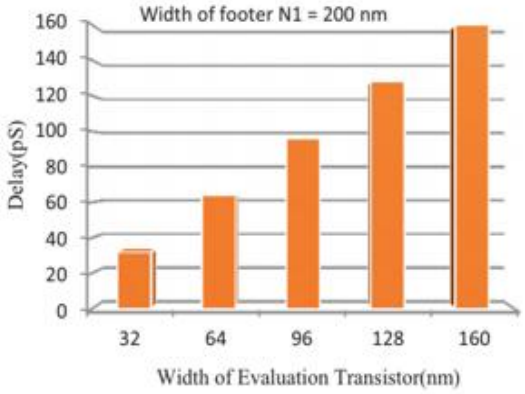


Fig.10 Effect of evaluation transistor width on delay

The voltage at node N decreases with increase in size of N1 and increases with increase in size of evaluation transistors. Fig. 10 shows the effect of variation of evaluation transistor width on delay of the circuit.

2.5 MODIFIED HIGH SPEED CLOCKED DELAY DOMINO LOGIC(MHSCD):

In HSCD technique, an AND gate G and an NMOS transistor are added to increase the speed of evaluation logic. This circuit is modified form of HSCD technique [9]. Therefore, it is termed as Modified HSCD (M-HSCD) shown in Fig. 11. In the evaluation phase, the dynamic node becomes high when one or more inputs are high in the evaluation block. In the AND gate, the a input goes high and the b input goes high and the output of AND gate(G) becomes high after two inverter delays. In this way, the speed of the evaluation logic increases. In the precharge phase, the node N2 is in high impedance state so it causes additional power consumption. This is the major drawback in MHSCD technique.

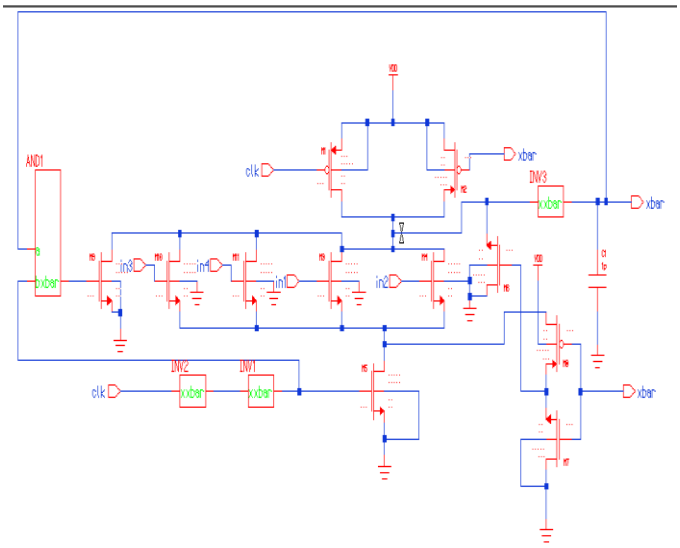


Fig. 11. Modified High Speed Clocked Delay Domino Logic

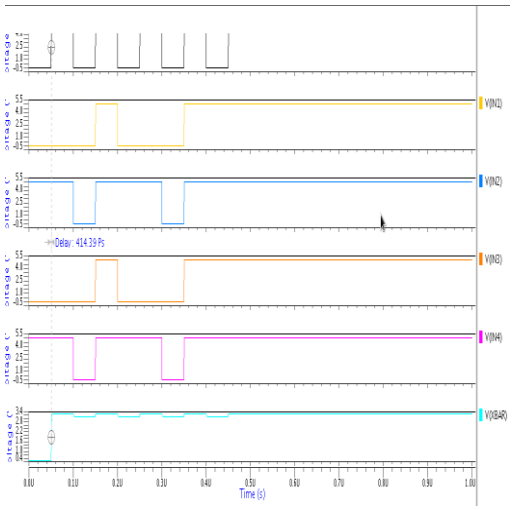
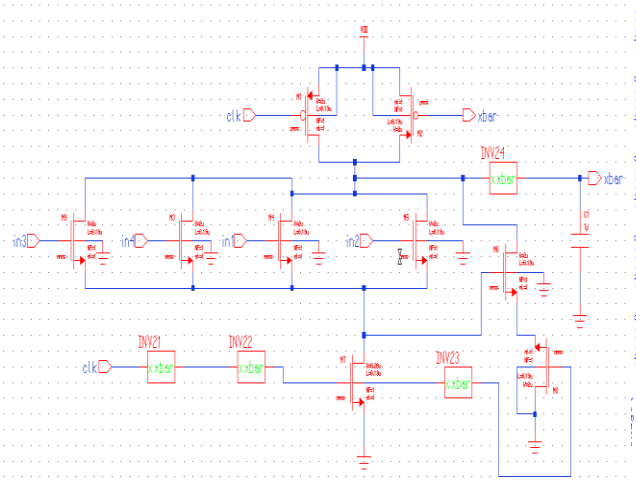


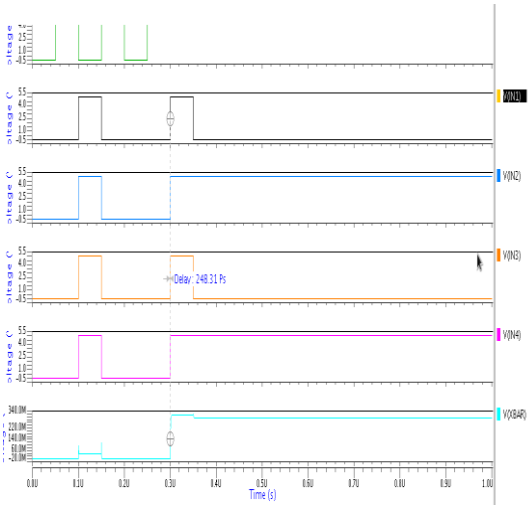
Fig. 12. Waveforms of Modified High Speed Clocked Delay Domino Logic

2.6 CONDITIONAL EVALUATED DOMINO LOGIC(CEDL):

The circuit Fig.13 shows the Conditional evaluated domino logic. The problem encountered in MHSCD technique can be minimized by using CEDL technique by using stacked configuration of NMOS transistors. The CEDL consist of both precharge and evaluation phase. The voltage at node n depends on the size of the footer transistor and the evaluation transistors. The voltage at node N drives the gate of the NMOS(N2) transistor. The maximum delay can be reduced but the power consumption gradually increases this is the major drawback of CEDL technique. The voltage at node N should be kept at minimum value to reduction of power consumption.



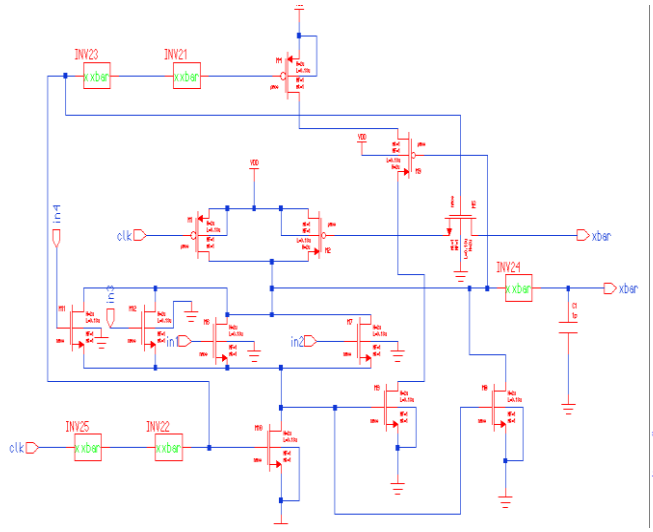
.**Fig. 13** Conditional Evaluated Domino Logic



.**Fig.14.** Waveforms of Conditional Evaluated Domino Logic

2.7 CONDITIONAL STACKED KEEPER DOMINO LOGIC(CSK-DL):

The Fig.15 shows the Conditional stacked keeper domino logic in which voltage at node N is given as a feedback to transistors N2 and N3 for discharging the dynamic node. Here, transistor N2 reduces the voltage at node Q to $V_{DD} - V_{TH}$ that causes an increase in current through the keeper transistor. The transistor N3 plays a critical role to determine the speed of the circuit. In this circuit, when clock goes high in the evaluation phase then the dynamic node discharges to ground.



.**Fig. 15** Conditional Stacked Keeper Domino Logic

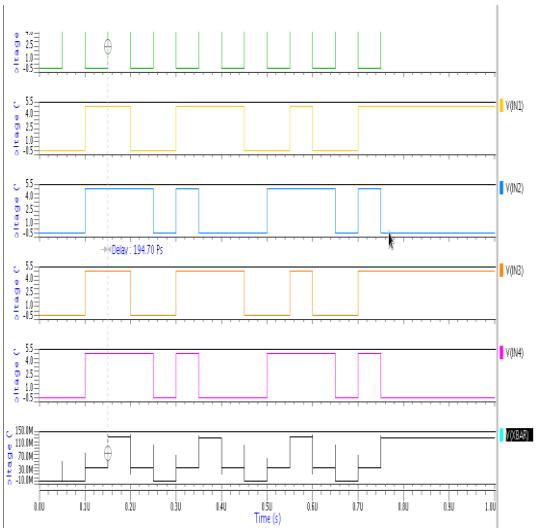


Fig. 16 Waveforms of Conditional Stacked Keeper Domino logic

2.8 FOOT DRIVEN STACK TRANSISTOR DOMINO LOGIC:

This circuit has precharge phase and the evaluation phase. The NMOS transistors N2 and N3 are arranged in stacked configuration. The ON and OFF condition of N2 and N3 transistors depends on voltage at node N. Whenever there is a voltage drop across N1 due to noise pulses, transistor N3 provides stacking effect by making the gate to source voltage of N2 smaller. This will reduce the leakage power of N2 and makes N1 conduct less. In this circuit, When the clock goes low then the dynamic node charges to logic high.

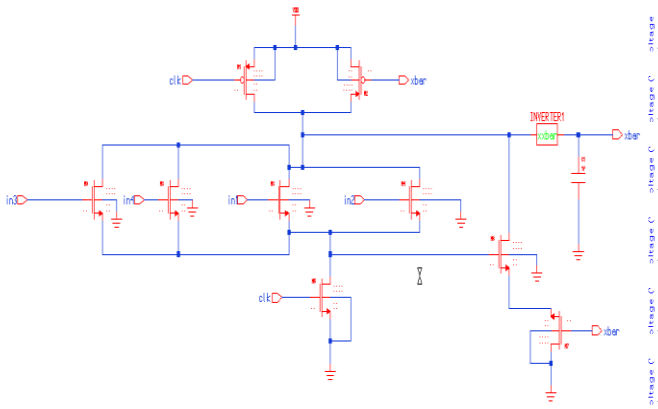


Fig. 17 Foot Driven Stack Transistor Domino Logic

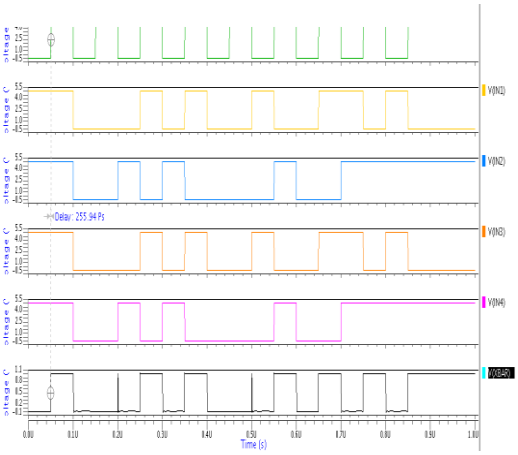


Fig. 18 Waveforms of Foot Driven Stack Transistor Domino Logic

III. System Overview

Here, in this method a new Comparator based domino logic is proposed. In order to reduce the power consumption and delay than the existing domino logic design.

3.1 Comparator based domino logic:

This technique consists of two stages named as DOMINO gate and Voltage Comparator (VC). Domino stage is used to implement wide-OR logic whereas VC is used to compare the two voltages at node A & B. First stage produces the two voltages A & B and these voltages decides the final output from second stage after the charging and discharging of the dynamic node. Mirror is incorporated to re-charge the dynamic node by transferring the current from one branch to another branch.

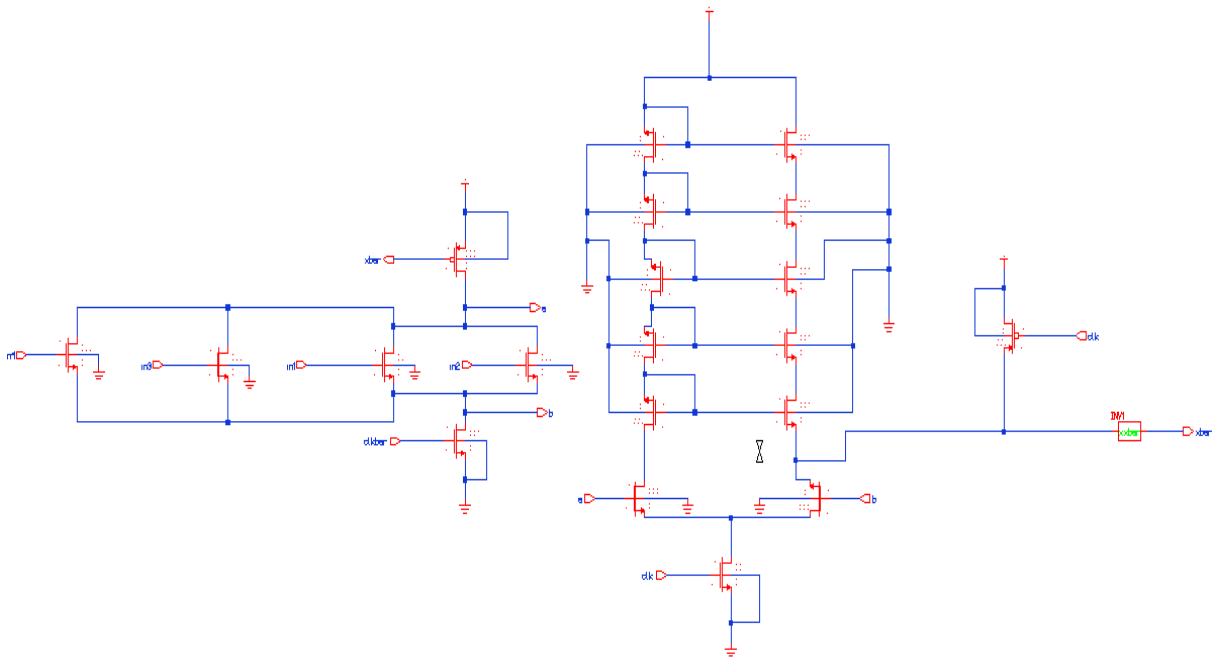


Fig 19. Comparator based domino logic for wide fan-in OR gate

In the proposed gate, as leakage current and capacitance at node A increase with the number of transistors in PDN, PD between node A & B increases. Hence, voltage difference between A & B decreases. Although, a small portion of voltages at node A & B is fed into Voltage Comparator, proposed design will give correct X_{bar} on the basis of voltage difference between A & B. Therefore, Differential pair is used to obtain the true logic at output and to reduce Power dissipation.

In simple current mirror, total current cannot be transferred due to channel length modulation (CLM). In order to overcome the effect of CLM, a cascade current mirror is used. As the transistors are stacked in the mirror, the threshold voltage of NMOS increases. As a result, leakage current decreases which reduces the power dissipation. Mirror is used to provide the high speed and reduction in leakage current by transistor stacking. Thus, the gate size ratio of right arm to left arm is defined as mirror ratio (M).

$$M = M_2/M_1$$

Mirror ratio also decreases with the number of transistors increase in stacking. Hence, the size of each transistor in the mirror should be low such that mirror ratio can be high and increment in area is also minimal. In the proposed designed, M1 and M2 will be controlled by the voltage at node A and B because of which DN will be controlled in EP and finally X_{bar} will be decided. This DOMINO logic technique for wide fan-in gates consists two phases same as dynamic logic circuit.

PRECHARGE PHASE:

The comparator based domino logic circuit consists of precharge transistor and keeper transistor in the pull up network (PUN) .The pull down network consists evaluation logic block in which the number of NMOS transistors are connected in parallel or in series manner according to the inputs. In the Precharge phase, all PDN transistors are in cut-off condition, transistor M_{dis} is OFF, Mp2 and transistor M_{footer} are ON at low Clock (CLK) voltage (CLK = '0' and CLK= '1') and low inputs. Hence, DN gets charge due to which inverter makes the X_{bar} low which turns ON the transistor Mp1 and start to charge node A. If any charge shares from node A by sub-threshold leakage, transistor M_{footer} is ON to maintain the zero voltage at node B. In this condition, there is no conduction path between DN and ground through transistor M2 due to which node DN is charged upto VDD to be logic '1' and also node A is charged upto VDD to be logic '1' and node B is discharged down to ground level to be logic '0'.

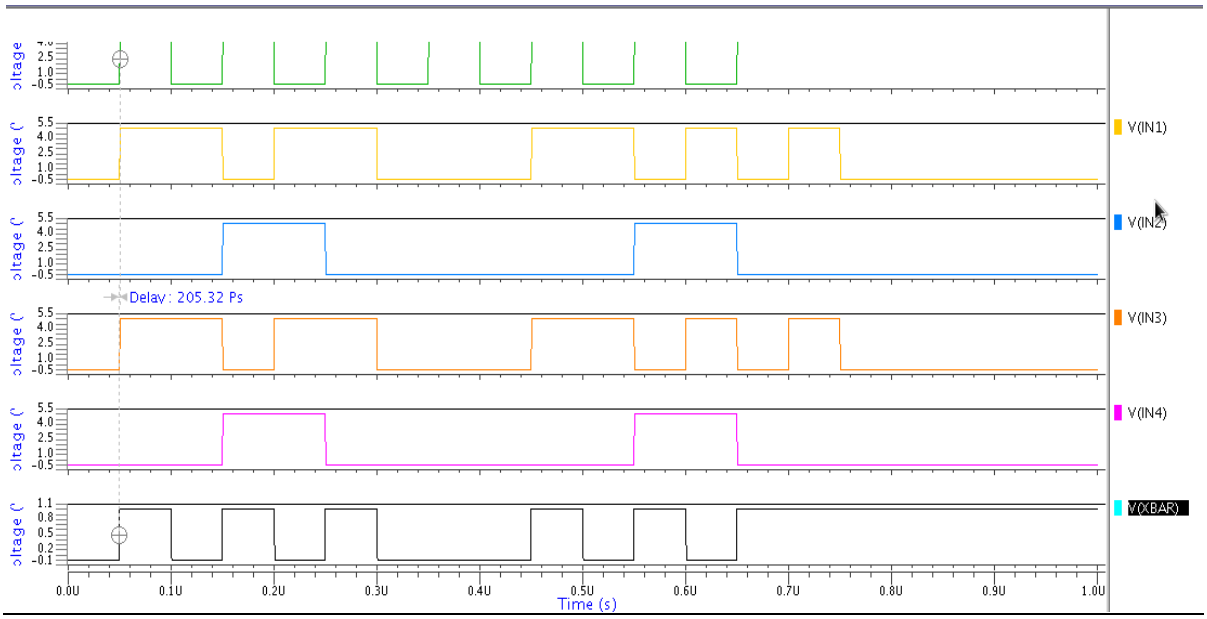


Fig 20. Waveforms of Comparator based domino logic for wide fan-in OR gate

EVALUATION PHASE:

The evaluation phase, at clk= '0' or clk_{bar} = '1',Mp2 and M_{footer} are in cut-off mode which turn OFF the transistor M_{footer} in order to maintain the voltage at node B. From PP to the starting of EP transistor Mp1 remains ON, after which it may remain ON or switched to OFF depending on input. Now, PDN, where NMOS transistors are connected in series, comes into action. All inputs of transistors of pull down network may be either high or low, or some may be high and rest at low logic. Now, two conditions can be considered; first one in which all inputs of signifies high voltage at node A. Only a small portion of this voltage will be shared with node B due to sub threshold leakage current. Hence, this small voltage is not capable of switching ON the transistor M2. Therefore, DN remains ON and in this situation left arm of mirror acts as keeper which keeps the dynamic node at high logic due to which X_{bar} remains at low logic which remains the transistor Mp1 ON. Now, the second condition in which at least one input must be at high logic, NMOS in pull down network will be ON and start to conduct. Thus one or more than one conduction path exists between node A & node B due to which voltage sharing is possible. The voltage at node B increases whereas voltage difference between node A & node B reduces. Therefore, M1 and M2 both turn ON and a conduction path exists between DN and ground because of which DN starts to reduce through transistor M2 and M_{dis}. Thus dynamic node switches to low logic and inverter switches the output at high logic due to which transistor Mp1 becomes OFF.

IV. Simulation Results

TABLE 1: Comparison of various domino topologies based on power, delay for a 2-input OR gate

Topology	Average power(µw)	Propagation delay(PS)
FLDL	0.030	568.7
FDL	0.015	520.5
CMFD	0.060	312.2
HSCD	0.032	418.1
MHSCD	0.040	417.1
CEDL	0.155	217.4
CSK-DL	0.163	197.3
FDS-DL	0.002	263.1
PROPOSED CIRCUIT	0.001	200.3

TABLE 2: Comparison of various domino topologies based on power, delay for a 4-input OR gate

Topology	Average power(µw)	Propagation delay(PS)
FLDL	0.060	316.0
FDL	0.018	526.9
CMFD	0.051	501.3
HSCD	0.036	426.1
MHSCD	0.045	414.1
CEDL	0.233	248.3
CSK-DL	0.242	194.7

FDS-DL	0.003	255.9
PROPOSED CIRCUIT	0.0015	205.3

TABLE 3: Comparison of various domino topologies based on power, delay for a 8-input OR gate

Topology	Average power(µw)	Propagation delay(PS)
FLDL	0.113	278.3
FDL	0.017	556.3
CMFD	0.052	521.8
HSCD	0.038	468.3
MHSCD	0.063	414.0
CEDL	0.366	301.3
CSK-DL	0.375	192.65
FDS-DL	0.0035	268.88
PROPOSED CIRCUIT	0.0010	200.09

TABLE 4: Comparison of various domino topologies based on power, delay for a 16-input OR gate

Topology	Average power(µw)	Propagation delay(PS)
FLDL	0.241	304.0
FDL	0.023	970.1
CMFD	0.055	557.8
HSCD	0.040	546.3
MHSCD	0.065	554.0
CEDL	0.593	185.61
CSK-DL	0.602	143.08
FDS-DL	0.003	249.24
PROPOSED CIRCUIT	0.0015	201.33

Xilinx results:

Comparator based domino logic for wide fan-in OR gate:

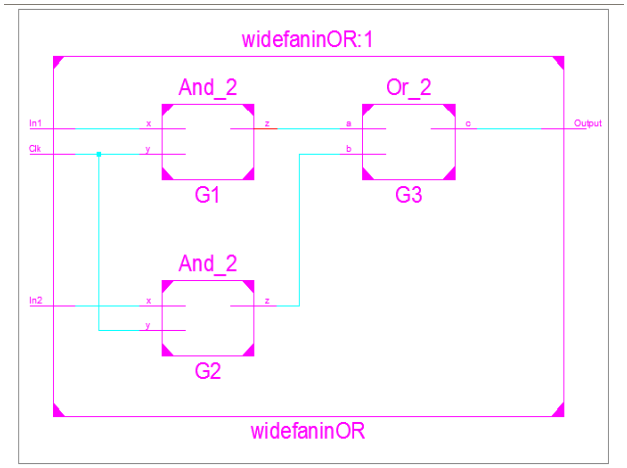


Fig 21.RTL schematic

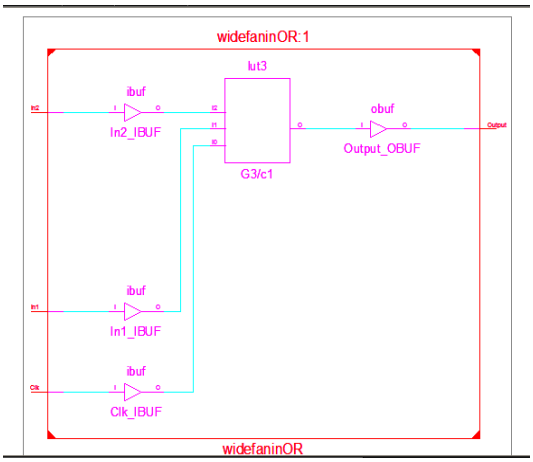


Fig 22. Technology view

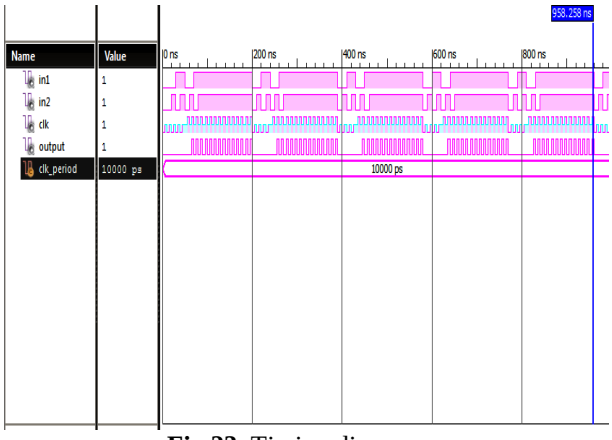


Fig 23. Timing diagram

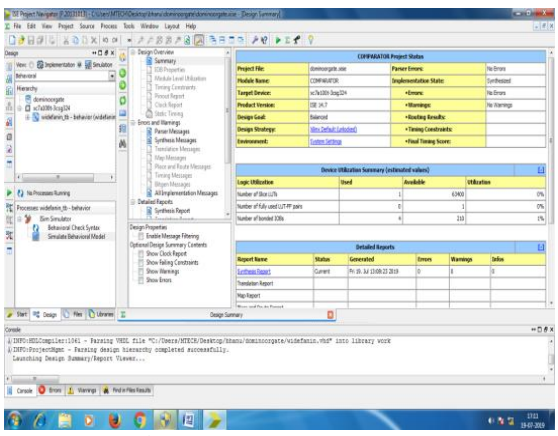


Fig 24. Summary report

V. Conclusion and Future scope

In this brief, The work is to design a new method that is comparator based domino logic technique for wide fan-in gates is designed to resolve trade-off among power consumption and propagation delay . This creates difficulty to design a new domino circuit for low threshold voltage. In contrast, the proposed gate reduces the power and delay. Wide fan-in gates are basic building microprocessors and also employed in read path of register files, flash memory etc., The different domino logic techniques is compared to the proposed technique. So, when compared to the existing foot driven stack transistor domino logic technique, the comparator based domino logic technique reduces the power consumption and propagation delay. Hence, the proposed comparator technique is more efficient in terms of power and delay.

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Kosuri Bhavani " Design of High Speed and Low Power Domino Logic Circuits For Wide Fan-in gates" IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) , vol. 9, no. 4, 2019, pp. 18-27.